Semiconductor Circuit Design

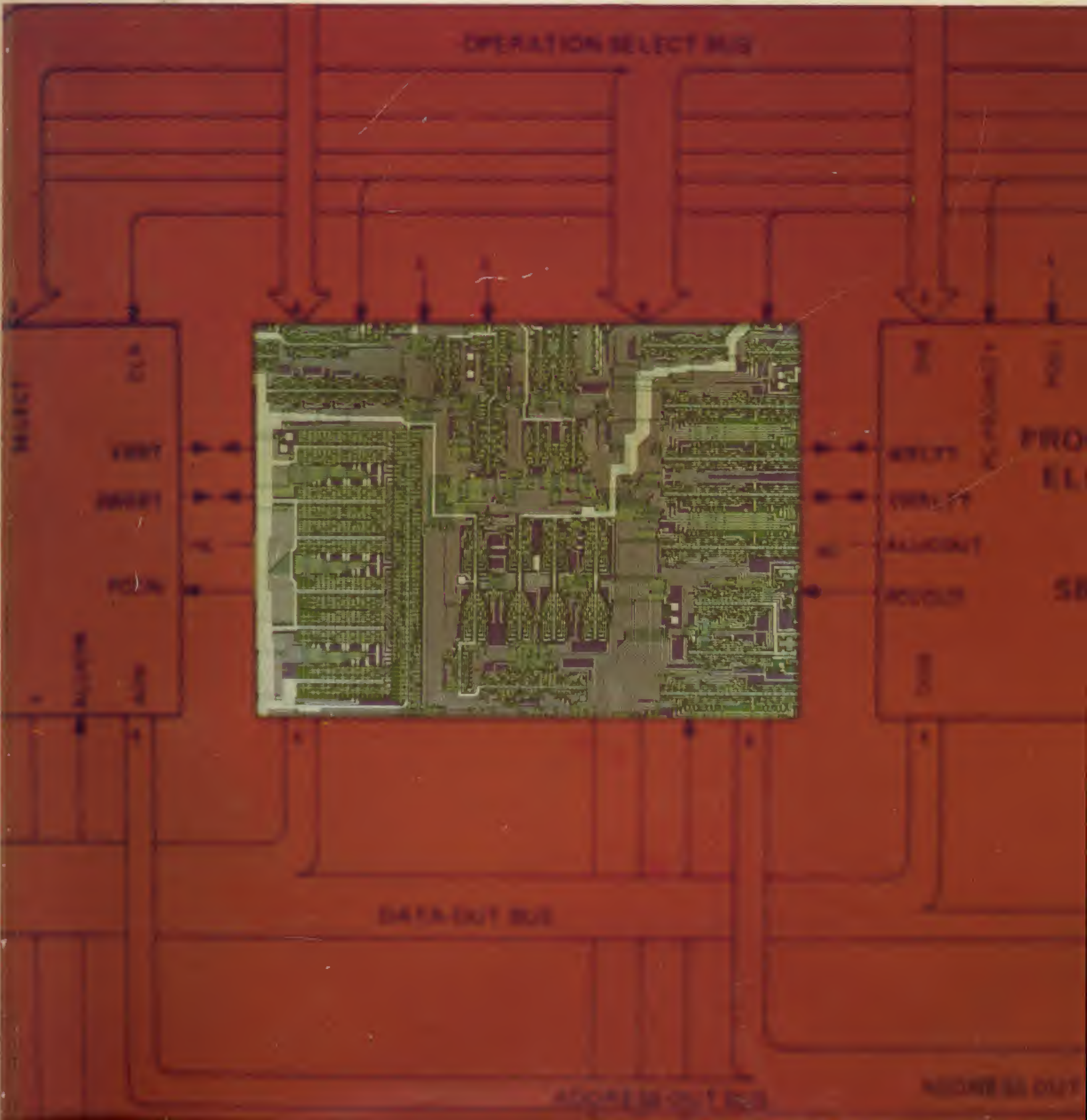
Vol. IV

Texas
Instruments
Limited

Semiconductor Circuit Design

Vol. IV

Edited by: Bryan Norris, Manager, Applications Laboratory, Texas Instruments Limited


OPERATION SELECT BUS
DATA OUT BUS
ADDRESS OUT BUS

Semiconductor Circuit Design

Bryan Norris, Texas Instruments Ltd.

This is the fourth in a series of text books published by Texas Instruments Ltd to enable the reader to keep up to date with the latest developments in circuit design using semiconductors. The majority of material in this volume has been written by members of the Texas Instruments Applications Laboratory in Bedford. The series of text books is edited by Bryan Norris who has been manager of the Bedford Application Laboratory since 1967 and has a wide experience in all areas of circuit design. This latest volume is divided into two sections which deal broadly with Power Control and Digital Processing Techniques. In each section are chapters covering operational data and a wide range of applications for devices such as Power Transistors, Rectifiers, Triacs, Programmable Unijunction Transistors, Numeric Displays and complex Bipolar and MOS I.C.s. There are also chapters on I^2L technology and I.C. Microprocessors.

In common with the other books in the series this volume is intended to be of use both to the moderately advanced student and the designers in industry who can apply the circuits as they stand or adapt them to a specific need.

The authors contributing to this volume include:

DAVID A. BONHAM
JUREK BUDEK
HOWARD COOK
STEVEN CRAFT
PETER VAN CUYLENBURG
PAUL GRÜNENFELDER
MICK MAYTUM
BOB PARSONS
JOHN READ
KEN SALMON
PETER WILSON

ISBN 0 904047 03 2

Semiconductor Circuit Design

Vol. IV

Ex-Libris
Arthur Missira
MCMXCVII

Semiconductor Circuit Design

Vol. IV

Edited by: Bryan Norris
Manager, Applications Laboratory,
Texas Instruments Limited

TEXAS INSTRUMENTS
LIMITED
MANTON LANE · BEDFORD · ENGLAND

Copyright 1975 by Texas Instruments Limited

All Rights Reserved

This publication, or parts thereof, may not be reproduced in any form without the permission of the publishers, Texas Instruments Ltd. Texas Instruments reserve the rights to make changes at any time in order to improve design and supply the best product possible. Information contained in this publication is believed to be accurate and reliable. However, responsibility is assumed neither for its use nor for any infringement of patent or rights of others which may result from its use. No licence is granted by implication or otherwise under any patent or patent right of Texas Instruments or others.

ISBN 0 904047 03 2

1st Edition May 1975
2nd Impression September 1975
3rd Impression January 1977

Printed in Great Britain by Morrison and Gibb Ltd, London and Edinburgh. Artwork produced by Newnorth Artwork Ltd, Bedford.

Preface

The aims of this series of Semiconductor Circuit Design books are to provide up to date information on a broad range of semiconductors, and to give straightforward examples of how the devices may be used in practice. All the chapters have therefore been written by practising professional engineers with these aims in view.

The arrangement of sections differs from proceding volumes in that, instead of grouping the chapters by device types, I have sectioned the book into two broad application areas, namely Power Control and Digital Processing Techniques.

In the first section there are three chapters which examine Rectifiers, High Voltage Power Transistors and Programmable Unijunction Transistors respectively. The following two chapters describe circuits in which these devices are employed, and the section is completed by chapters on touch control and phychedelic lights control.

The Digital Processing section opens with one chapter defining and grouping microprocessors and microcomputers and explaining the use of two specific types, and a second describing how, by using Schottky T.T.L. I.C.s, a fast microcomputer may be produced. The succeeding chapters are concerned with peripheral devices and circuits, e.g. Programmable Read Only Memories, T.T.L. Random Access Memories, Universal Asychronous Receiver/Transmitter, Binary and Decimal Rate Multipliers, Priority Encoders and Numerical Displays. The final chapter describes the evolution, fabrication and applications of a new technology, Integrated Injection Logic (I^2L).

I should again like to express my thanks to all the contributing authors, and also the editor of Practical Wireless, Lionel Howes, for permission to use material originally written for that magazine, on which Chapter VII is based.

BRYAN NORRIS

Applications Manager
Texas Instruments Limited
April 1975

Contents

SECTION 1. POWER CONTROL

Page

Chapter I USE OF RECTIFIERS 1
Single Phase Rectifier Circuits.. 1
Three Phase Rectifier Circuits.. 13
Three Phase Power System 14
References 22

Chapter II USE OF HIGH VOLTAGE SWITCHING TRANSISTORS 23
Construction 23
Effect on Parameters 24
A Circuit Operation 25
Transistor Ratings 27
Switching Requirements 28
Control of Base Current 29
Measurement Parameters 29
Measuring Systems 29
Measurement Procedure 30
Device Dissipation 31
Analysis of Waveforms 32
Transient Analysis 33
References 34

Chapter III PROGRAMMABLE UNIJUNCTION TRANSISTORS.. 35
Device Characteristics 35
Definition of Parameters 39
Applications 39
Reference 46

Chapter IV INVERTER/CONVERTER SYSTEMS 47
Single Ended Self Oscillating Circuits 47
Single Ended Driven Circuits 50
Push-Pull Self Oscillation Circuits 55
Push-Pull Driven Circuits 57
References 64
Acknowledgement 64

Page

Chapter V SWITCHING MODE POWER SUPPLIES 65
Cascaded Approach 65
Design Example (Single Power Device Approach) 68
References 75
Appendix 76

Chapter VI TOUCH SWITCH POWER CONTROL 79
Using Field Effect Transistors 79
Using Integrated Circuits 82
References 90
Acknowledgement 90

Chapter VII PSYCHEDELIC LIGHTS CONTROL 91
Circuit Description 91
Interconnection 94
Lamp Dimming 98
References 100

SECTION 2. DIGITAL PROCESSING TECHNIQUES

Page

Chapter VIII MICROPROCESSORS 103
Micro-Computer Concepts 103
Micro-Processors 104
A 4-Bit Slice Microprocessor Element 107
One Chip Microcomputers 116
References 123

Chapter IX A SCHOTTKY T.T.L. MICROCOMPUTER 125
A Fast Microcomputer 125
The SN74S281 4-Bit Accumulator 131

Chapter X USE OF PROGRAMMABLE READ ONLY MEMORIES 139
System Timing Generation 139
Information Checking 140
High Speed Character Generators 142
References 145

Chapter XI REFERENCE MARK GENERATOR FOR AUTOMATED EQUIPMENT .. 147
Operation 147
Circuits 147
References 151

Chapter XII A UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER 153
Operation 154
Supplementary Circuits 159
Applications 162
References 165
Acknowledgements 165

Chapter XIII BINARY AND DECIMAL RATE MULTIPLIERS 167
Description 167
Arithmetic Operations 171
Mathematical Operations 176
Practical Consideration 178
References 180
Appendix I 181
Appendix II 182

		Page
Chapter XIV	PERIPHERAL CIRCUITS	183
	Priority Encoders	183
	Keyboard Encoders	185
	Digital to Analogue Converters	186
	Precision Triangular Function Generator	188
	Reference	189
Chapter XV	DISPLAY AND COUNTING CIRCUITS	191
	Construction	191
	Description	191
	Applications	196
	References	204
	Acknowledgement	204
Chapter XVI	INTEGRATED INJECTION LOGIC	205
	Evolution of the I.I.L. Gate	205
	Fabrication	206
	Design	208
	Power Supplies	210
	Applications	211
	References	211
	Index	213
	Contents of Semiconductor Circuit Design Volume I	218
	Contents of Semiconductor Circuit Design Volume II	219
	Contents of Semiconductor Circuit Design Volume III	220

SECTION 1.

POWER CONTROL

I USE OF RECTIFIERS

by

Jurek Budek and Mick Maytum

Silicon rectifiers/diodes have uses in many electronic and electrical engineering applications. These include power supplies, inverters and converters, amplifiers, servo systems, modulators and demodulators, d.c. restoration, d.c. stabilization and arc suppression. The advantages of silicon devices are their small size and weight, their long-term reliability under adverse conditions of vibration and shock, a high efficiency and their independence of external excitation. A diode/rectifier may be regarded as a non-linear resistive device possessing low electrical resistance, ideally zero, in the forward direction and high resistance, ideally infinite, in the reverse direction. Overall silicon devices approach more closely to the ideal than any other rectifying device.[1]

In the basic half-wave circuit, consisting of a rectifier in series with a single-phase a.c. source and a resistive load, the rectifier functions as a synchronized switch. It allows current to flow each time the source has one particular polarity and interrupts current when the source polarity reverses, so that the load current flows in half-cycle pulses. This pulsating current is unsuitable for most purposes but can be 'smoothed', or made to flow more uniformly, by:

(*a*) passing the current through a filter
(*b*) increasing the number of phases
(*c*) increasing the number of cycles of operation (i.e. half-wave to full-wave circuit).

For most low and medium power applications, where the source is a single phase a.c. supply, the rectified current is smoothed by a filter consisting of one or more reactive elements. The amount of ripple that can be tolerated governs the complexity of the filter which may be either:

(*a*) a capacitor-input filter, which presents a shunt capacitance to the rectifier output, or
(*b*) a choke-input filter, which presents a series inductance to the rectifier output.

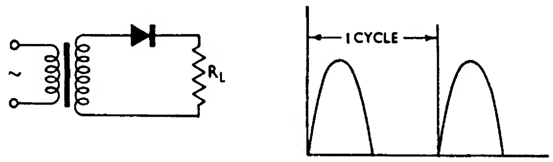
In certain applications, such as lightweight power supply units for airborne equipment, three phase circuits are commonly used as the output requires very little filtering and the higher efficiency and good power factor of the three-phase circuit also reduce the weight of the unit.

For high power rectification, where large currents are involved, the filter components tend to be bulky and expensive and here also it is more convenient to increase the number of phases and dispense with the filter entirely, e.g. 24 phases for the power supplies of electro-chemical equipment. The most common applications for large high voltage (h.v.) power supplies are radar, radio transmitters, travelling wave tubes, microwave, inductive and dielectric heating. The circuit most frequently used for these supplies is the three phase bridge. The design information given in the last part of this chapter, therefore, is for a three phase bridge, together with efficiency and power factor calculation.

SINGLE-PHASE RECTIFIER CIRCUITS

Half-Wave Circuit

This circuit (Figure 1) is simple, uses only one rectifier and does not need an intermediate transformer for some applications. Its use is restricted to low output powers since its efficiency is low and the output voltage has a large low-frequency ripple, which makes smoothing more difficult. In addition, if a transformer is used, d.c. magnetization of the core occurs.



(a) BASIC CIRCUIT (b) OUTPUT WAVEFORM

FIGURE 1. Half-Wave Circuit

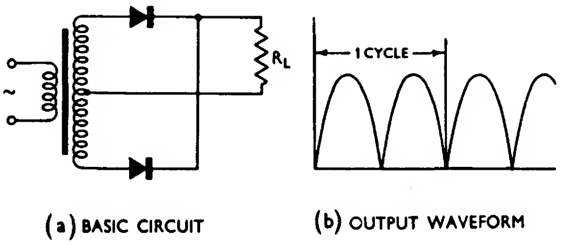
Full-Wave Circuits

The two main types of full-wave circuits are:

(*a*) the centre-tapped transformer circuit
(*b*) the bridge circuit

A transformer with a centre-tapped secondary winding can be used with the bridge circuit when a three-wire d.c. supply is required. These circuits are used for the larger output powers since they are more efficient than the half-wave circuit, give a smaller ripple voltage at twice the supply frequency, and produce only negligible d.c. magnetization in the core of the transformer.

The Centre-Tap Transformer (Bi-Phase) Circuit: As shown in Figure 2 this consists of two half-wave circuits operating in push-pull on alternate half-cycles, the single-phase supply being effectively split into two phases.



(a) BASIC CIRCUIT (b) OUTPUT WAVEFORM

FIGURE 2. *Centre-Tap (Bi-Phase) Circuit*

The Bridge Circuit: Where higher d.c. output voltages are required the bridge circuit (Figure 3) has several distinct advantages over the centre-tap circuit. For a device of a given inverse voltage rating the d.c. output voltage obtainable using the bridge circuit is twice that using the centre-tap circuit. The bridge circuit allows the use of transformers without the complication of a centre-tapped secondary winding. This is particularly advantageous at high voltages as the number of turns in the secondary of the bridge circuit transformer is half that of the centre-tapped secondary for a given output, or at high frequencies where the number of turns is very low or an odd number. The current flows continuously in the secondary of the bridge circuit transformer and only half the time in each half of the winding of the centre-tapped transformer. Hence the transformer for the bridge circuit has a higher utilization of the winding space. These factors lead to a simpler and smaller transformer for the bridge circuit and in certain cases one may not even be required.

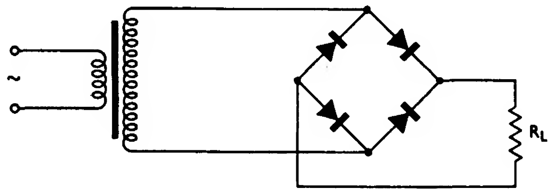


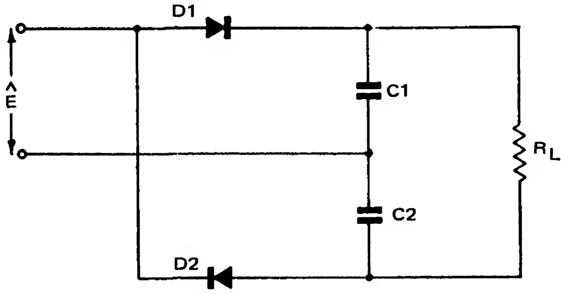
FIGURE 3. *Single-Phase Bridge Circuit*

The Centre-Tapped Bridge Circuit: The use of a centre-tapped transformer secondary in the bridge circuit is a convenient means of splitting the output voltage for applications such as audio, operational, differential amplifiers, etc. In this case there is still no d.c. saturation of the transformer core, even when only one-half of the output is loaded. The output should not be followed by a single capacitor filter as the alternating current can flow through the unloaded input capacitor to the load and upset the balance when only half the output is loaded. Both 'half' voltage and full voltage contain the same percentage ripple at twice the supply frequency. The ripple in the halves of the output is in anti-phase and the effect is to cancel in the equipment it feeds, which may allow some reduction in smoothing components.

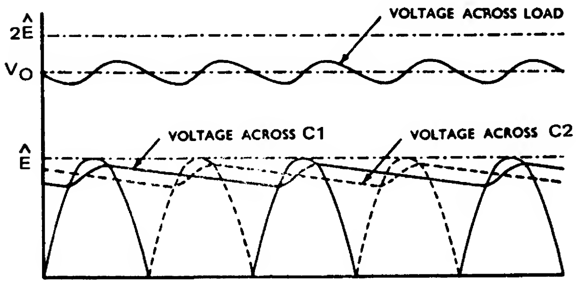
Voltage Multiplier Circuits[2]

These circuits utilize the principle of charging capacitors in parallel from the a.c. input and adding the voltages across them in series to obtain d.c. output voltages higher than the source voltage. With these circuits filtering must necessarily be of the capacitor-input type.

Voltage Doublers: Conventional and cascade circuits are considered together for ease of comparison. In the conventional circuit (Figure 4) the capacitors C1 and C2 are

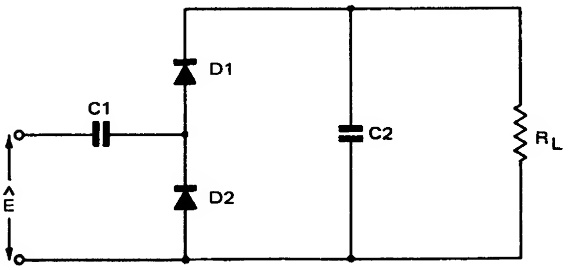


(a) BASIC CIRCUIT

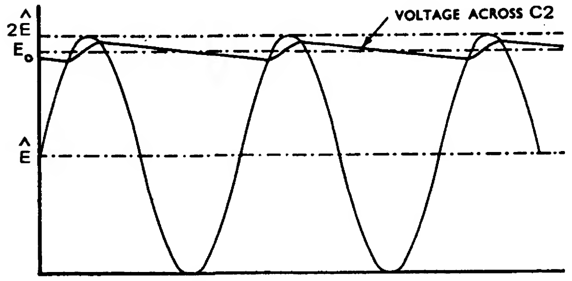


(b) OUTPUT WAVEFORM

FIGURE 4. *'Conventional' Voltage Doubler*



(a) BASIC CIRCUIT



(b) OUTPUT WAVEFORM

FIGURE 5. *'Cascade' Voltage Doubler*

each charged, during alternate half-cycles, to the peak value of the alternating input voltage, thus giving an output of twice the a.c. peak voltage.

In the cascade circuit (Figure 5) capacitor C1 is charged to the peak value of the a.c. input voltage through diode D2 in one half-cycle and in the other half-cycle it discharges in series with the a.c. source through diode D1 to charge capacitor C2 to twice the a.c. peak voltage.

The 'conventional' circuit has the slightly better regulation and since the ripple frequency is twice the supply frequency filtering is easier, the percentage ripple being about the same in both cases. In addition, both capacitors are rated at the a.c. peak voltage, whereas capacitor C2 in the 'cascade' circuit has to be rated at twice this figure. With both circuits the peak inverse voltage across each device is twice the a.c. peak. The 'cascade' circuit, however, has the advantage of a common input and output terminal and, therefore, permits combination of units to give higher order voltage multiplications. The regulation of both circuits is poor so that only small load currents can be drawn. A typical output characteristic for the conventional circuit is given in Figure 6 and the same curve is approximately correct for a practical cascade circuit in which the value of ωCR_L is greater than 10.

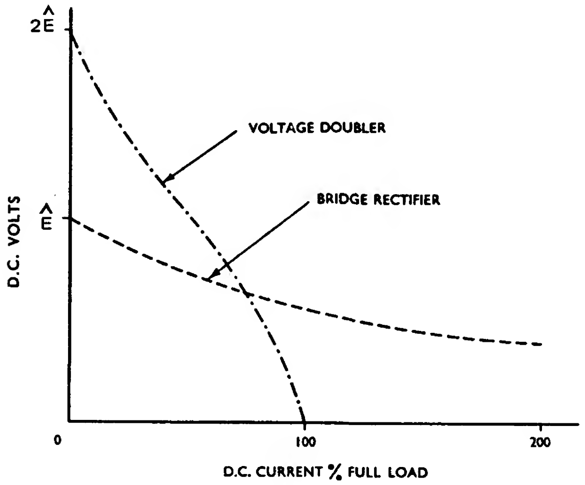


FIGURE 6. Output Characteristics of some Single-Phase Circuits

The Bridge Voltage Doubler circuit, as shown in Figure 7, is a combination of the conventional voltage doubler and the bridge rectifier circuit. Although often shown in literature, as the only function of the extra diodes, D3 and D4, is to prevent voltage reversal on the output capacitors due to, say, an output short circuit, this circuit is very little used in practice.

Voltage Triplers: The circuit, shown in Figure 8, adds the output of a cascade voltage doubler and a half-wave rectifier in series to give an output voltage three times the a.c. peak. Capacitors C1 and C3 are rated at the a.c. peak voltage and C2 at twice this figure, the peak inverse voltage (p.i.v.) across each rectifier being twice the a.c. peak.

In pulse circuits the a.c. waveform is unsymmetrical resulting, say, in the positive excursion of the waveform being orders of magnitude greater than the negative excursion. Thus there is very little difference between full voltage doubling and simple half-wave rectification of the positive peak. When applied to voltage multipliers this means that twice the number of stages is required to produce slightly more than three times the positive peak. This has resulted in the 'loose' terminology of the name 'voltage tripler' being applied to five or six stages of voltage multiplication, e.g. in colour television.

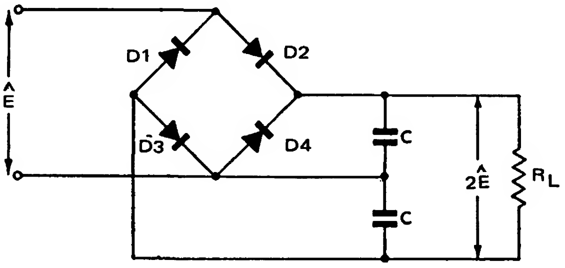


FIGURE 7. Bridge Voltage Doubler

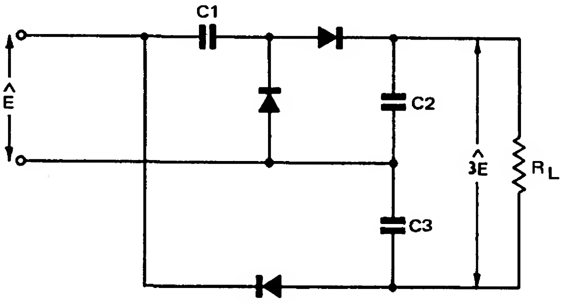
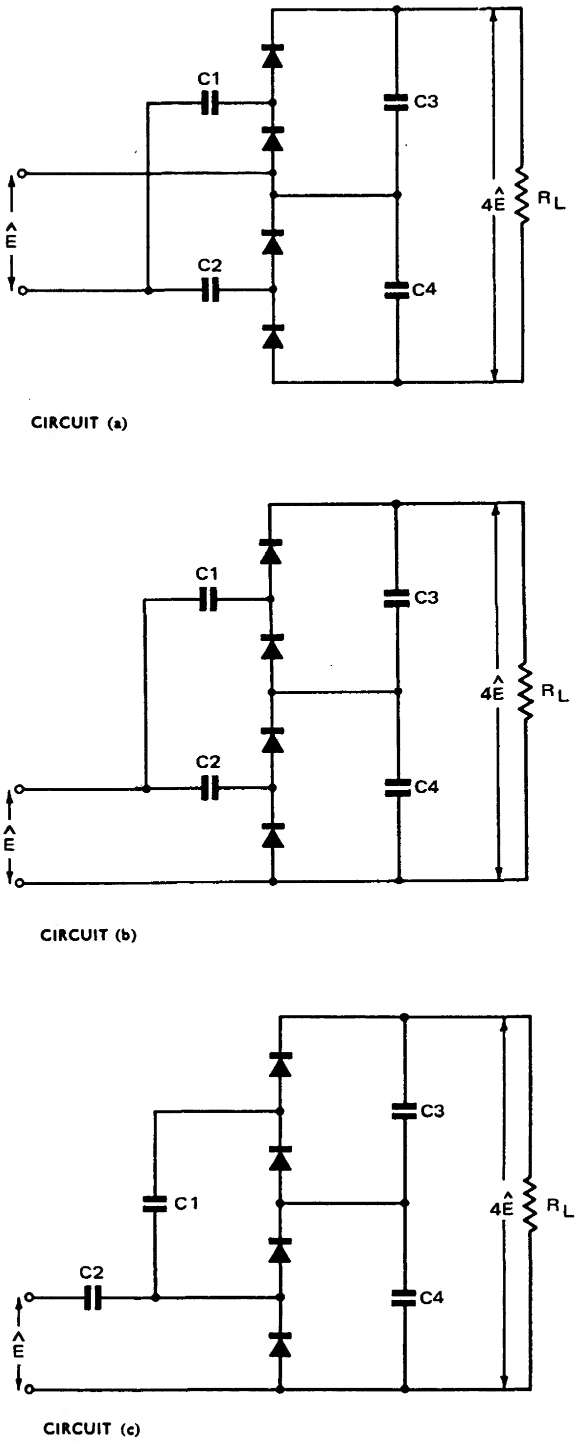


FIGURE 8. Voltage Tripler

Voltage Quadruplers: Three alternative circuits are shown in Figure 9. Circuit (*a*) is a symmetrical arrangement with capacitors C3 and C4 rated at twice the a.c. peak voltage. Circuits (*b*) and (*c*) have a common input and output terminal and, therefore, can be extended for further voltage multiplication. In circuit (*b*) capacitor C1 is rated at three times the a.c. peak voltage and C3 and C4 at twice the a.c. peak, while capacitors C1, C3 and C4 are rated at twice the a.c. peak in circuit (*c*). However, the input capacitor C2 in the latter circuit has to have twice the capacitance of that in (*b*). The peak inverse voltage across each device in all these circuits is equal to twice the peak voltage.

n-Stage Voltage Multiplication (Cockcroft-Walton Circuit): The voltage quadrupler circuit (*c*) can be further extended as shown in Figure 10 to obtain higher d.c. voltages. The voltage ratings of all 'ladder' capacitors and devices are twice the a.c. peak throughout but the capacitance values have to be graded as shown for an optimum design. However in practice the designer will usually opt for the same value of capacitor throughout to minimize the number of components required, stored, etc. The value of C will be the same as that for the cascade voltage doubler, which is the basic unit for this circuit. The value of the load resistance for this basic unit should be taken as $\frac{1}{n}$th the value of the load resistance for the voltage multiplier chain, where 'n' is the number of cascade units in the chain.



CIRCUIT (a)

CIRCUIT (b)

CIRCUIT (c)

FIGURE 9. Voltage Quadrupler Circuits

Capacitor-Input Filter^3

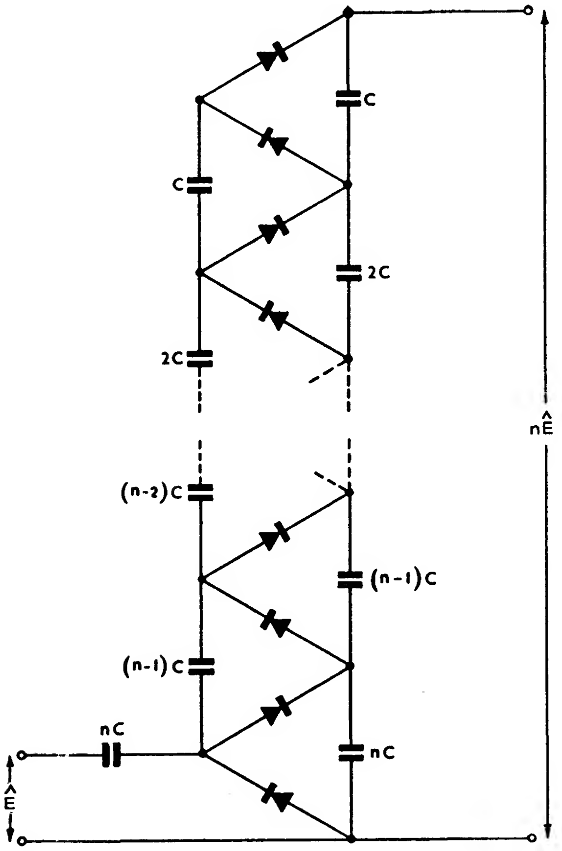


FIGURE 10. n-Stage Voltage Multiplication Circuit

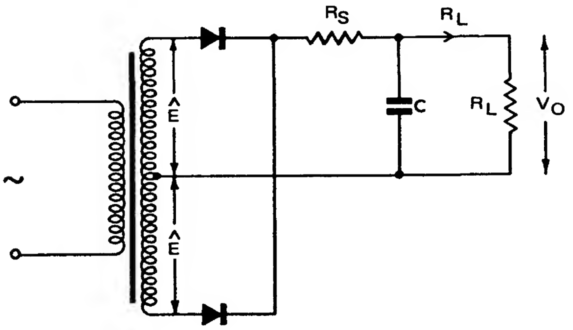


FIGURE 11. Capacitor-Input Filter with Centre-Tap Circuit

Circuit Configuration: To illustrate the behaviour of capacitor-input circuits the full wave centre-tap circuit is used with a reservoir capacitor C across the resistive load R_L, as shown in Figure 11. The total source resistance through which the capacitor charging current flows is represented by R_S; this includes the resistance of one-half of the secondary winding, the reflected, primary resistance, the forward resistance of the devices and any series added resistance. The action of the circuit is demonstrated by the waveforms of Figure 12. The capacitor C acts as a reservoir. As the secondary voltage approaches peak value and exceeds the voltage across capacitor C one of the diodes conducts, charging the capacitor almost to the a.c. peak voltage. This charging period is only a small part of the cycle and during the rest of the cycle capacitor C discharges through load resistance R_L, the voltage across it falling almost linearly. The values of the peak current through the rectifiers, $\hat{I}$, and the d.c. output voltage, V_O, depend in a complex manner on the following factors:

- (*a*) The load resistance R_L
- (*b*) The filter capacitor C
- (*c*) The leakage reactance of the transformer.
- (*d*) The source resistance R_S

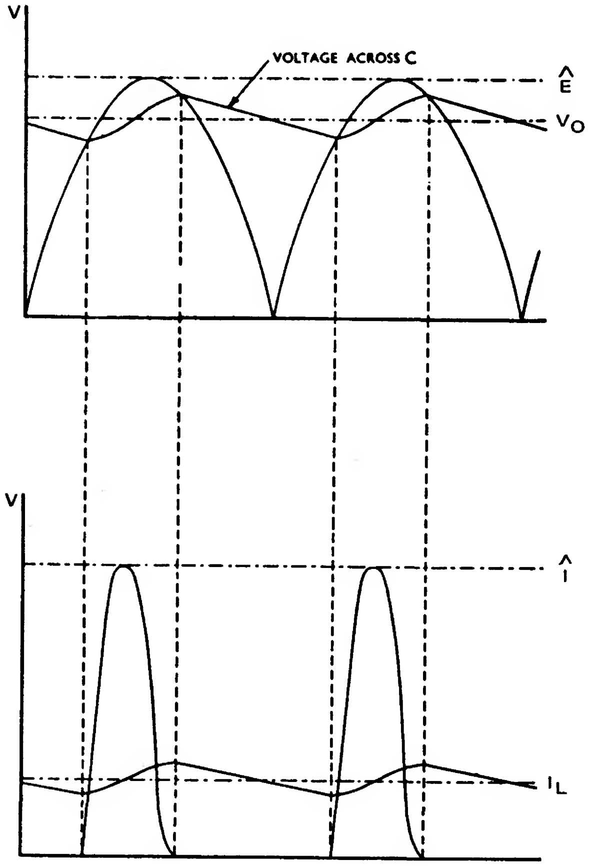


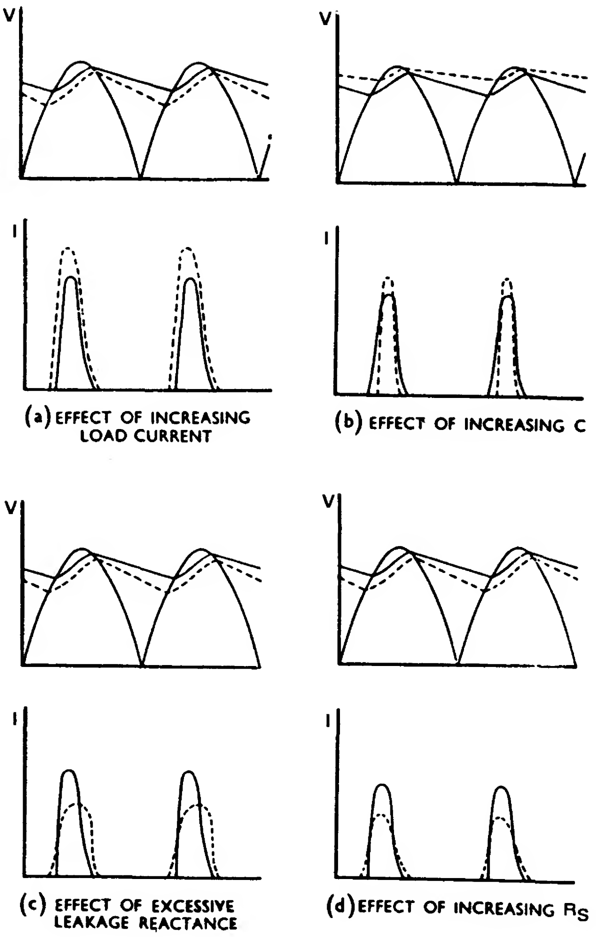
FIGURE 12. Waveforms for Capacitor Input Filter Circuit

The effects of these on the charging current waveforms are illustrated in Figure 13.

In a particular power supply problem the d.c. output voltage, load current and ripple content conditions required are usually known. The circuit design meeting these requirements must also ensure that the rectifier units are not operated under conditions in excess of the ratings quoted by the manufacturer. The major ratings are:

- (i) Peak inverse voltage, p.i.v.
- (ii) Average rectified forward current, I_O.
- (iii) Recurrent peak forward current, $\hat{I}$
- (iv) Surge current at switch-on, I_S.

The worst forward current condition occurs at switch-on when a large initial charging current flows through the device to the input capacitor. At the instant of switching on the a.c. supply the capacitor charging current is equal to the instantaneous secondary voltage divided by the total source resistance, R_S and therefore has a maximum possible value $\hat{E}/R_S$. In the majority of circuits the time constant CR_S is small compared with the half-cycle period of the a.c. supply, so that the charging current falls very rapidly to a value much lower than that at switch-on. If the time constant is large compared with the half-cycle period the charging current alternately in each device will be approximately a half-sine wave pulse of peak value less than $\hat{E}/R_S$, and will be repeated in successive alternate half-cycles with exponentially decreasing amplitude. The surge current in the recurrent peak current may have to be limited by the addition of extra resistance in the charging path at the cost of efficiency and regulation. This is particularly relevant in the case of the modern switching mode inverter which operates directly from the bridge rectified supply by using high voltage transistors to provide a.c. mains regulation.



(a) EFFECT OF INCREASING LOAD CURRENT

(b) EFFECT OF INCREASING C

(c) EFFECT OF EXCESSIVE LEAKAGE REACTANCE

(d) EFFECT OF INCREASING R_S

FIGURE 13. Effect of Various Parameters on the Waveforms

The calculations involved in the design are simplified by the series of curves derived by O. H. Schade[4] for the half-wave, full-wave and voltage doubler circuits. They define:

(*a*) the percentage ripple content of the output voltage, as given in Figure 14.
N.B. This is expressed as an r.m.s. value of the waveform and the total peak to peak value is approximately $\sqrt{12}$ times this.

(*b*) the ratio of d.c. output voltage to peak input voltage. Figure 15 is for half-wave, Figure 16 for full-wave and Figure 17 for voltage doubler circuits.

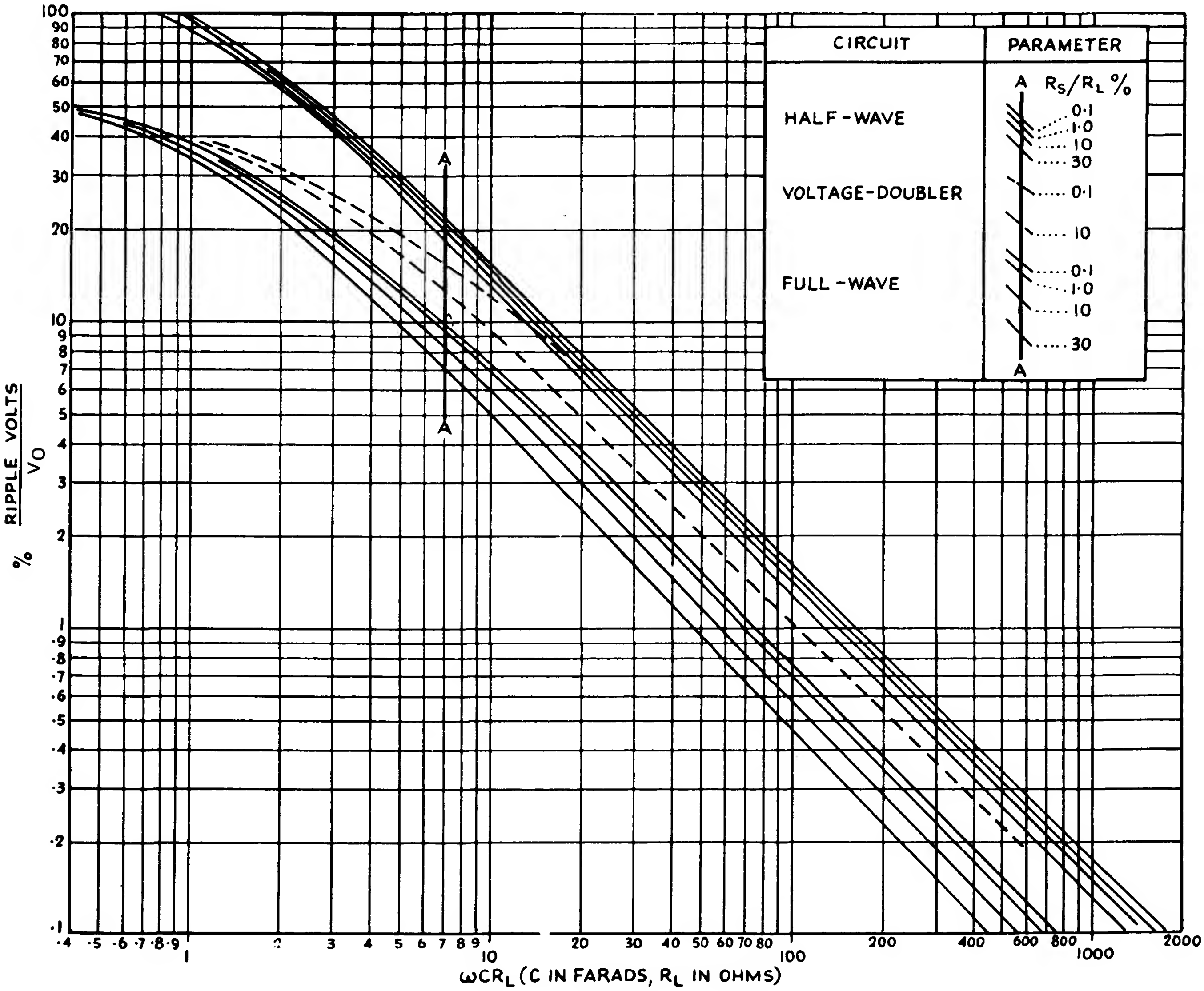
(*c*) the ratio of peak to average current per rectifier, Figure 18.

They are drawn for a range of supply frequencies, capacitances, and load and source resistances.

It can be seen that R_S affects the performance of the circuit considerably. The forward resistance of silicon rectifiers is extremely small and, since it is normally a negligible part of the total source resistance, a value corresponding to the voltage drop at the mean forward current can be assumed. The total value of R_S must be sufficient to restrict peak rectifier resistance leads to loss of efficiency and poor regulation due to the voltage drop across it. The minimum value of filter capacitance C is determined by the maximum ripple content and the load resistance. In addition, if good regulation is required the value of ωCR_L should lie to the right of the upper bend of the curves in Figures 15 to 17. However, when a large capacitance is needed to achieve this, excessive peak currents are incurred, imposing an additional limit on the maximum current which can be drawn.

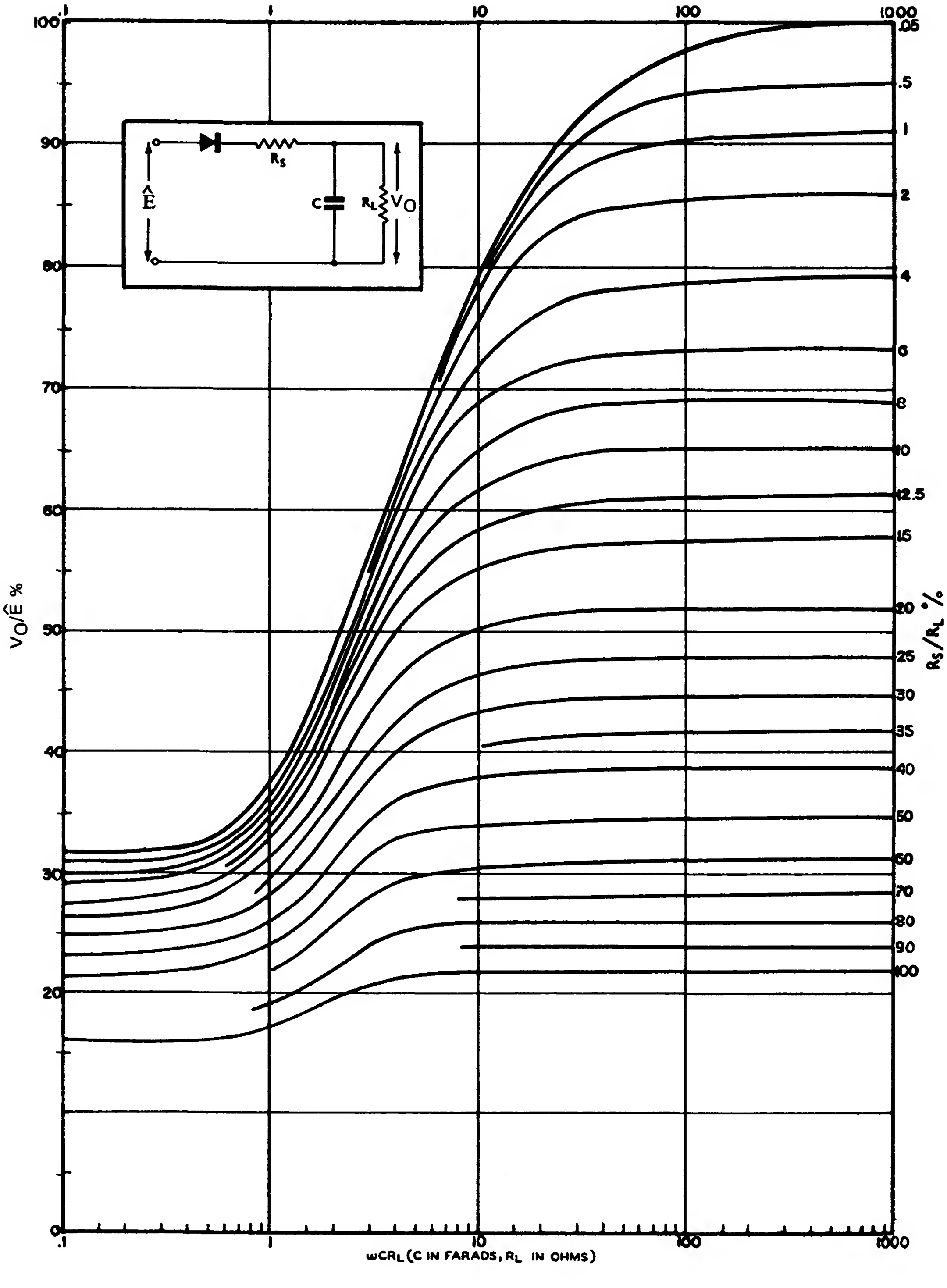
The effect of transformer leakage reactance is to decrease the peak currents through the rectifiers, as shown in Figure 13(c), and for low powers is small. However for large powers it must be taken into account as discussed later.

In a typical circuit R_S is of the order of 6% of R_L and the ripple voltage about 5% of the mean d.c. output. Under these conditions the relationships given in Table 1 are approximately correct for a sinusoidal input voltage. They give an indication of the performance of capacitor input circuits, but since peak current conditions are critical it is necessary in the design of particular circuits to adopt the detailed analysis illustrated by the examples. The

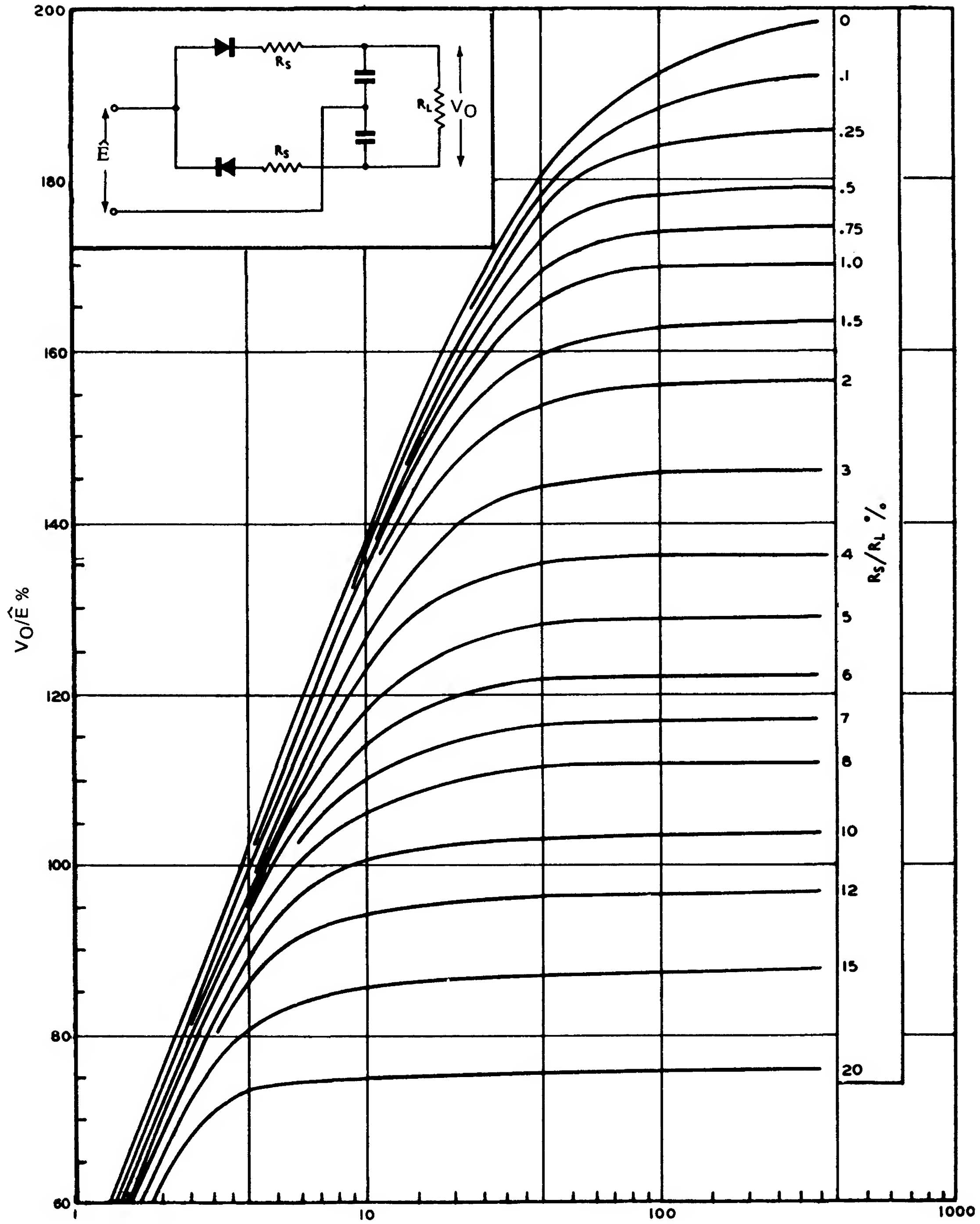


* *FIGURE 14. Root-Mean-Square Ripple Voltage for Capacitor-Input Circuits*

* (By permission from O. H. Schade, Proc. I.R.E., July 1943,)



* FIGURE 15. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Half-Wave Capacitor-Input Circuits.



* *FIGURE 17. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Capacitor-Input Voltage Doubler Circuits.*

current ratios I_L/I_O in the table indicate a typical derating to allow for the peak currents through the rectifiers, I_O being the maximum average forward current which each rectifier can pass into a resistive load. A further derating of this value is required (I_{av}) when capacitative smoothing is used, to account for the high peak currents.

Table 1. Typical Voltage & Current Relationships

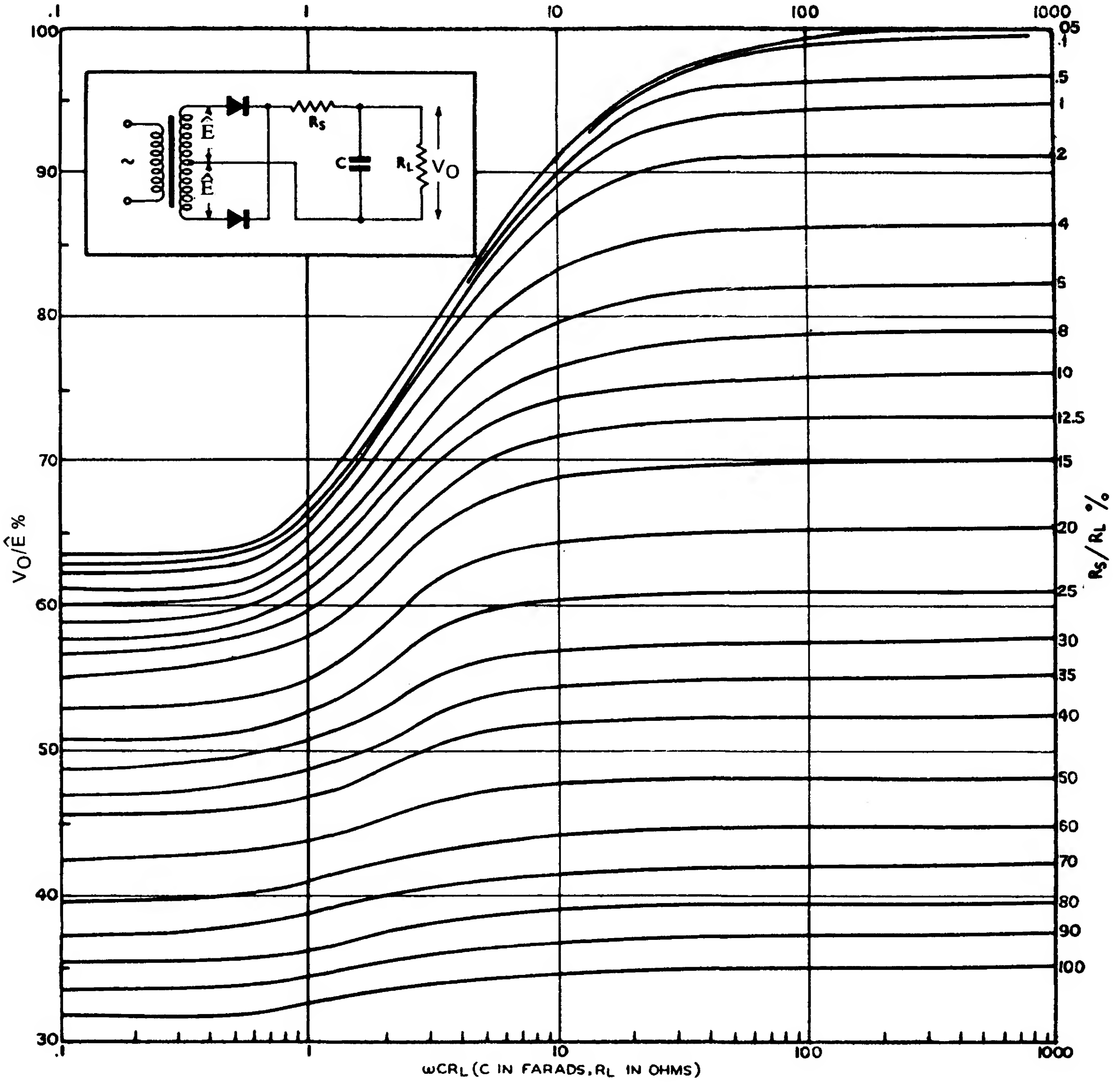
	Half-wave	Centre-Tap	Bridge	Voltage Doubler
V_O/E_{rms}	1.2	1.2	1.2	2
P.i.v./E_{rms}	2.8	2.8	1.4	2.8
I_L/I_O	0.8	1.6	1.6	0.8

Practical Example: Consider the mains power supply for the Stereo Texan Amplifier, of Figure 12, page 165 of Semiconductor Circuit Volume II. The required specification is:

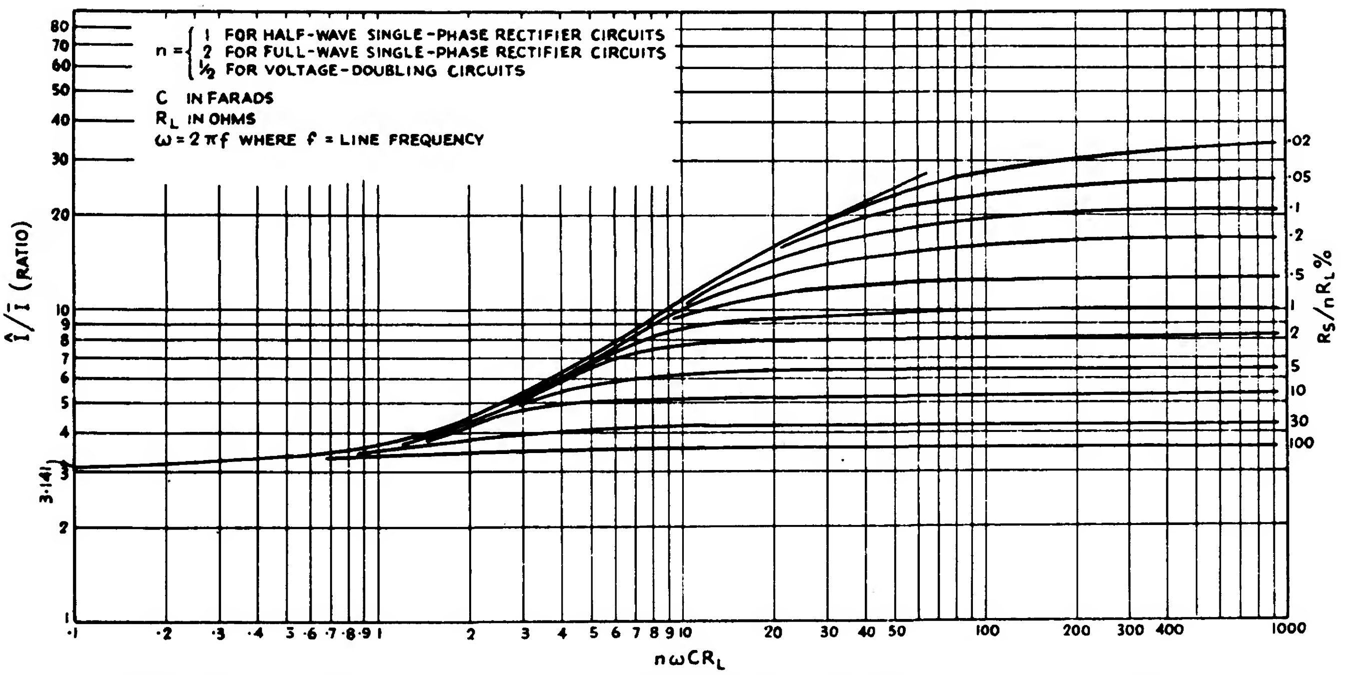
No load output voltage, V_O, = ±32V
(Determined by the output transistor voltage ratings)

Minimum output voltage, V = ±17V,
when both channels driven at 16W into 8Ω.

Peak to peak ripple voltage under these conditions,
E_R, = 5%.



* *FIGURE 16. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Full-Wave Capacitor-Input Circuits.*



* *FIGURE 18. Relation of Peak Current to Average Current per Rectifier in Capacitor-Input Circuits.*

The circuit chosen is a complex compromise between cost, bulk, efficiency and regulation. Under normal music conditions, over 20W are available on each channel. Continuous sinewave drive conditions represent a heavy current demand on the power supply and results in the supply rail falling to approximately 17V (although 16W is available from both channels under these conditions). This relatively poor regulation provides excellent short circuit protection for the amplifiers it feeds.

The circuit is analysed as two opposite polarity biphase rectifier circuits:

The peak no load transformer winding voltage, E, is given by

$$\hat{E} = \hat{V}_o + \check{V}_F$$

where V_F is the diode forward drop at low currents (≏0:6V).

Therefore $\hat{E} = 32 + 0{\cdot}6 = 32{\cdot}6\text{V}$.

$E_{r.m.s.} = 32{\cdot}6/2^{\frac{1}{2}} = 23\text{V}$ (No load)

The twin output power of 16W sinewave into 8Ω is equivalent to a single load of 32W into 4Ω. The average power supply current I_L for this is

$$I_L = (32/4)^{\frac{1}{2}}\ 2^{\frac{1}{2}}/\pi = 4/\pi$$

$$= 1{\cdot}27\text{A}$$

The effective power supply load R_L on each rail is

$$R_L = V_o/I_L = 17/1{\cdot}27$$

$$= 13{\cdot}4\Omega$$

As neither the effective rectifier source resistance, R_S, or the value of the reservoir capacitor C1 are known, some iteration is required. The large fall in output voltage with loading shows $R_S/R_L\%$ to be high, say 40%. Using this value and recognising the 5% peak to peak ripple rating corresponds approximately to $5/12^{\frac{1}{2}} = 1{\cdot}5\%$ r.m.s. ripple, Figure 14 shows a ωCR_L factor of 30 is required to achieve this.

Therefore $C1 = 30/2.\pi.100.\ 13{\cdot}4 = 3{,}600\mu\text{F}$.

The average to peak to peak ratio is given by

$(\check{E}_o + \hat{V}_F)/(\hat{E}_o + \check{V}_F)$ where $\hat{V}_F$ is the diode forward drop at high currents (≏1V).

i.e. $(17 + 1)/(32 + 0{\cdot}6) = 0{\cdot}49$ i.e. 49%.

This from Figure 16 with this ratio 49% and $\omega CR_L = 30$

$$R_S/R_L = 48\%.$$

Therefore $R_S = 13{\cdot}2 \times 0{\cdot}48$

$$= 6{\cdot}4$$

The average current I_{av} per diode will be

$$I_L/2 \text{ or } 1{\cdot}27/2 = 0{\cdot}63\text{A}$$

Figure 18 shows an I/I_{av} value of 4, hence

$$I = 0{\cdot}63 \times 4 = 2{\cdot}5\text{A}.$$

The maximum rectifier surge current, I_S will be

$$E/R_S = 32{\cdot}6/6{\cdot}4 = 5A$$

and the working p.i.v. will be $2\hat{E}$ or 65V.

These ratings can be adequately met by a 1N4002 diode.

Thus the specification arrived at is:

Diodes 1N4002
Reservoir Capacitors 3,500μF at 40V
Effective Source Resistance $R_S = 6{\cdot}4\Omega$.
$E_{r.m.s.}$ 23V – 0 – 23V No load.

If the power supply performance was of a highly critical nature the above working would be modified to account for component, loading and mains supply tolerances.

Check

The transformer specified for the amplifier is a Gardeners SL20 and a sample of one of these had the following characteristics. (Design values in brackets.)

$R_P = 147\Omega$
$R_S = 1{\cdot}9\Omega$/winding ($R_S = 6{\cdot}4\Omega$)
No load rectified voltage 33V (32V)
Maximum load rectified voltage = 18V (17V)
Percentage ripple at maximum load = 1·45V peak or 8% (5%)
Rectifier repetitive peak current = 3·2A (2·5A)

Practical and design performance figures differ mainly due to the rectifier source resistance being slightly lower than the design value at,

$$2 \times 142/([33 + 0{\cdot}63]/245 \times 2\tfrac{1}{2})^2 + 1{\cdot}9$$

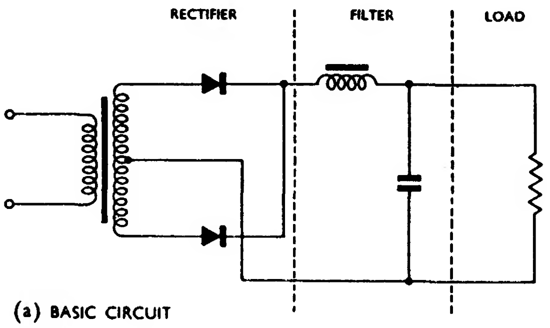
$$= 3{\cdot}1 + 1{\cdot}9$$
$$= 5\Omega$$

Note the effective referred primary resistance must be doubled to account for the currents of both the positive and negative rail rectifiers.

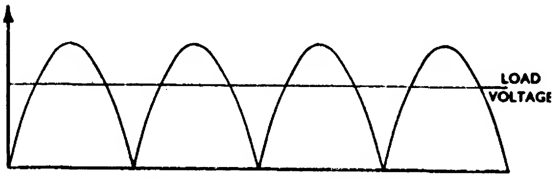
Choke Input Filter

In smaller equipments choke input filters are nowadays too costly and bulky to be employed. Their main application is therefore in industrial systems where large amounts of power are involved.

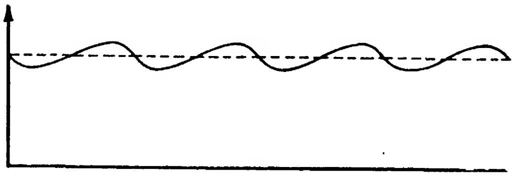
Choke-input circuits are shown in Figures 19 and 20. In the ideal situation when the choke has infinite reactance and zero resistance the load current is constant and all the ripple voltage is developed across the choke. The current is transferred instantly from one rectifier to another each time the supply voltage passes through zero. In Figures 19 and 20, the broken waveforms refer to the case of infinite inductance and the solid curves to finite inductance. The choke inductance must be above that value which just causes the pulsating current from the rectifiers to become continuous and consequently prevents the current in the filter from falling to zero in any part of the cycle. This value is known as the 'Critical Inductance'. When the inductance is less than the critical value the circuit behaves as a capacitor-input circuit. In practice an inductance double the critical value, known as the 'Optimum Inductance', is used. The effectiveness of the choke depends on the time constant L/R_L, so that the value of critical inductance varies inversely as the load current. Hence as the minimum load current decreases the value of choke inductance required increases. In view of this a 'swinging choke' can be used to advantage. With this type of choke the inductance decreases with increase of d.c.



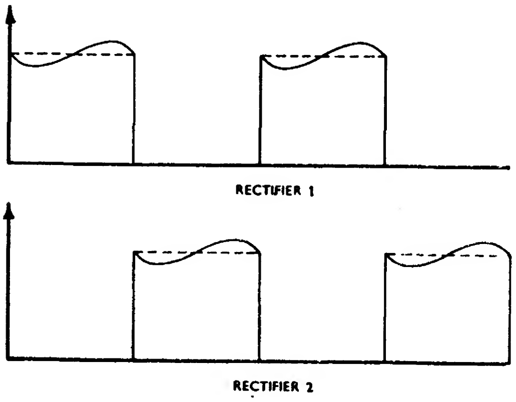
(a) BASIC CIRCUIT



(b) RECTIFIER OUTPUT VOLTAGE



(c) CURRENT IN INDUCTANCE



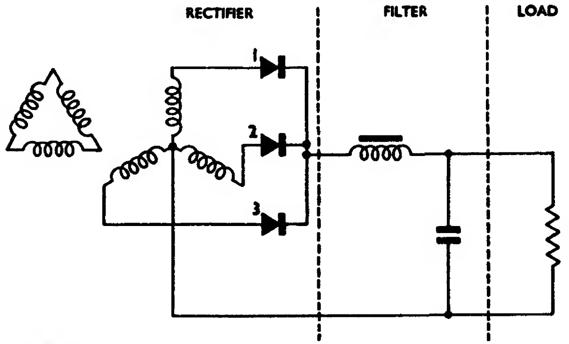
(d) CURRENTS IN INDIVIDUAL RECTIFIERS

FIGURE 19. Choke-Input Filter with Centre-Tap Circuit

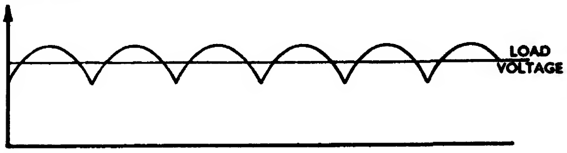
current, due to saturation of the core. Its value at low currents can be much larger than that of a constant inductance choke (such as is required in additional filter sections) of the same dimensions. The decrease of choke inductance as load current increases is not inconvenient since the critical inductance also decreases at high load currents. Usually the choke is designed to have the optimum inductance at minimum load current, so that filtering is effective over the entire current range. If the load current is decreased below the normal minimum it eventually reaches a value at which the critical inductance becomes equal to that of the choke used. This value is known as the critical load current, I_C, for the choke (see Figure 21) At load currents less than this the circuit behaves as a capacitor-input filter circuit. When such small load currents are required the deterioration in regulation can be avoided by connecting a 'bleeder' resistance permanently across the load to prevent the current through the choke from falling below the critical value.

The ratio of peak current per rectifier to load current depends on the type of circuit and the choke inductance. In the ideal case each rectifier passes the entire load current for part of each cycle, except in the three-phase double star circuit where each carries only half the load current. For a critical inductance choke the peak current is twice the load current.

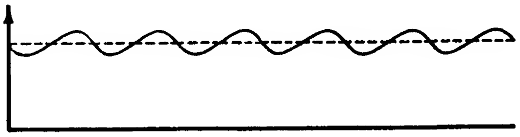
The waveforms of Figures 19 and 20 neglect the effect of transformer leakage reactance which prevents instantaneous transfer of current from one rectifier to another. In practice the waveforms are modified as described later in the three-phase bridge design.



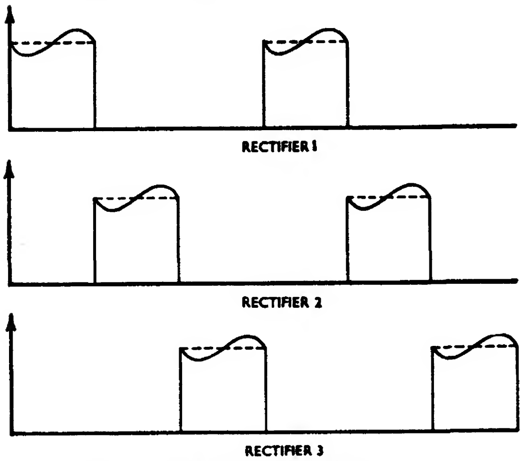
(a) BASIC CIRCUIT



(b) RECTIFIER OUTPUT VOLTAGE



(c) CURRENT IN INDUCTANCE



(d) CURRENTS IN INDIVIDUAL RECTIFIERS

FIGURE 20. Choke-Input Filter with Three-Phase Half-Wave Circuit

Additional Filter Sections

When the ripple voltage must be reduced to an extremely low value which cannot be achieved with a single section, it used to be the practice to use further CR or LC filter sections. Nowadays this function has been replaced by switching mode regulators unless very large power is involved. In addition switching mode regulators can accommodate very large ripple percentages which permit economies in the size of the reservoir capacitor and the transformer.

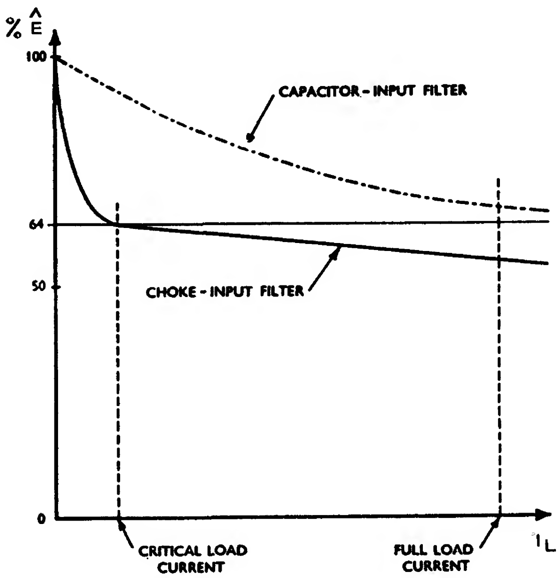


FIGURE 21. Output Characteristics of Input-Filters

THREE-PHASE RECTIFIER CIRCUITS

Half-Wave Circuit

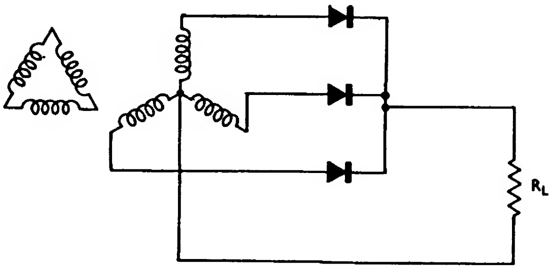
This is the simplest of the three-phase circuits (Figure 22) using the minimum number of devices. It consists essentially of three single-phase half-wave circuits, each device carrying the current for one-third of the cycle. The obvious advantages of using a three-phase a.c. supply are higher efficiency and lower ripple content, which is at three times the supply frequency. In addition, if the transformer windings for all three phases are suitably arranged, i.e. in 'zig-zag' connection, on the same core no d.c. magnetization of the core will be produced. This circuit is used for comparatively low power outputs at voltages less than half the rated p.i.v. of the devices.

Centre-Tap Circuit

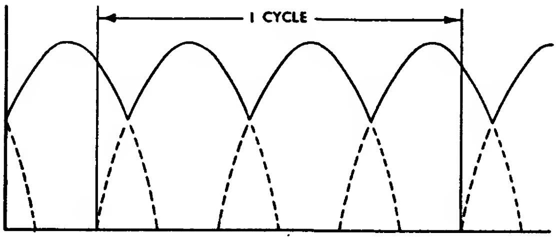
This circuit, known as a 'diametric' connection and shown in Figure 23, may be regarded as two three-phase half-wave circuits displaced in phase by 60° and operating in parallel. The current in each rectifier flows for one-sixth of a cycle, giving a smoother output with a ripple frequency six times that of the supply. The efficiency is higher than that of the three-phase half-wave circuit and this circuit is used for larger powers at voltages less than half the rated p.i.v. of the devices. As all the devices have a common connection the 'packaging' of the power supply unit is simplified.

Double Star Circuit

This circuit (Figure 24) differs from the previous one by the introduction of an interphase reactor between the two half-wave circuits. This reactor enables the two circuits to operate independently so that each rectifier conducts for one-third of the cycle instead of one-sixth. The peak current through each rectifier is reduced to half that in the previous case because at any instant there are two rectifiers carrying current. This reduces the current rating required for each rectifier but the p.i.v. across them is twice the peak phase voltage. The circuit has applications similar to the previous one where the reduction in the cost of the rectifiers due to their lower current ratings would more than offset the cost of the interphase reactor. For the lower voltage, heavy current circuit this arrangement is the most efficient as the rectifier losses consist of the single rectifier loss and not two in series as in the following bridge circuit.

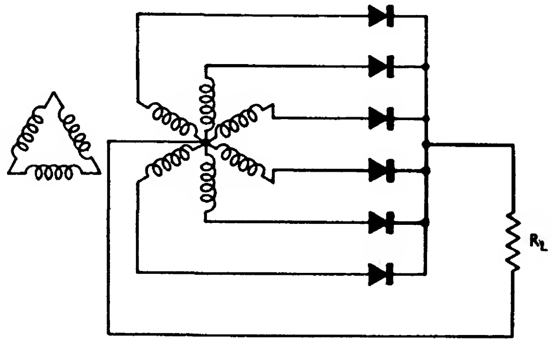


(a) BASIC CIRCUIT

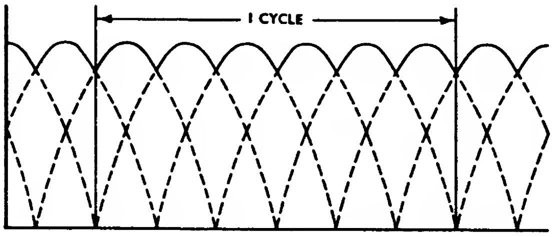


(b) OUTPUT WAVEFORM

FIGURE 22. Three-Phase Half-Wave Circuit



(a) BASIC CIRCUIT



(b) OUTPUT WAVEFORM

FIGURE 23. Three-Phase Centre-Tap Circuit

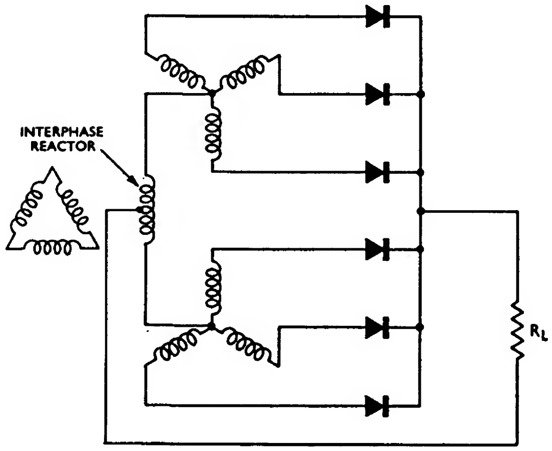


FIGURE 24. Three-Phase Double Star Circuit

Bridge Circuit

In this circuit (Figure 25) full-wave rectification is obtained from each phase. At any instant, excluding a short circuit condition, two rectifiers conduct simultaneously and in series in the sequence AF–FB–BD–DC–CE–EA giving six peaks per cycle in the output. This is one of the circuits most frequently used with semiconductor devices. It has the high efficiency and low ripple content of the previous circuits but requires a smaller transformer and no interphase reactor. The transformer secondary may be either star or delta wound as no neutral point is required. It is used for higher output voltages, as the p.i.v. across each rectifier is half that in the centre-tap circuit and the a.c. voltage required for a given d.c. output is the lowest of any circuit discussed.

Centre-Tapped Bridge Circuit

When a three-wire d.c. output is required, a three-phase bridge circuit can be used with a centre-tap on a star-connected transformer secondary winding. When current is drawn from only one-half of the output the circuit operates as a three-phase half-wave circuit. The ripple content is then higher than when both halves are in use and it is at three times the supply frequency.

Voltage Doublers

Figure 26 shows the three-phase version of the conventional single-phase voltage doubler. It can be used for larger output powers than the single-phase circuit and has a regulation similar to that of the single-phase bridge doubler.

The three-phase bridge voltage doubler (Figure 27) has improved regulation characteristics and can be used to provide much larger currents. The output voltage, even on overload, never falls below that of the three-phase bridge rectifier as the comparative regulation curves of Figure 28 show. The percentage voltage ripple of these circuits is much smaller than that of the single-phase circuits.

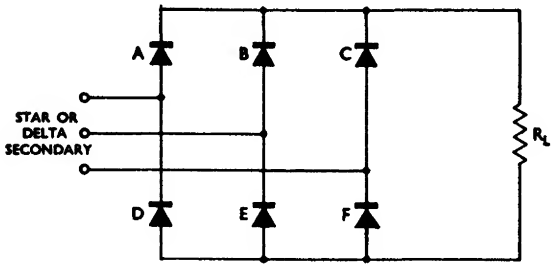


FIGURE 25. Three-Phase Bridge Circuit

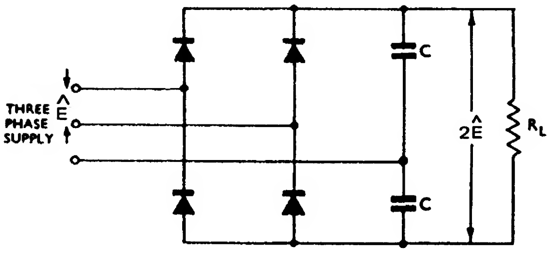


FIGURE 26. Three-Phase Voltage Doubler

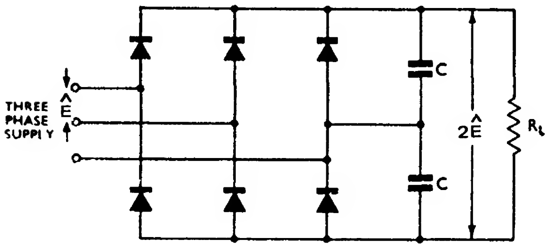


FIGURE 27. Three-Phase Bridge Doubler

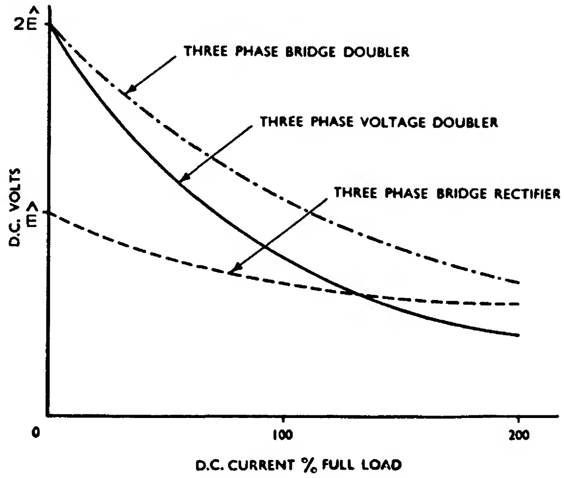


FIGURE 28. Output Characteristics of Some Three-Phase Circuits

THREE-PHASE POWER SYSTEM

The introduction of silicon rectifiers gave rise to new ideas in designing high voltage, h.v., power equipments. H.v. silicon rectifier stacks offer the advantages of long life, small size, reliability and low operating costs when compared with thermionic valves. Furthermore, there is no need for the warming up period and heating transformer associated with thermionic valves. The silicon devices used in h.v. assemblies incorporate their own inherent reverse voltage limiting protection. They are of a non-destructive avalanche breakdown type, so that additional protection against excessive voltage transients is not required in the majority of cases. The stacks may be encapsulated in epoxy resin thus giving a rigid construction suitable for mounting either on insulation or metal plates or brackets. For larger powers the stacks can be connected in series or parallel.

Series Operation of Avalanche Rectifiers

When connected in series controlled avalanche rectifiers require no shunting resistors to ensure an equal reverse voltage distribution across each element because of their ability to work satisfactorily in the avalanche region. Figure 29 shows two rectifiers connected in series. For a given reverse voltage supply equal to $V_a + V_b{}'$ the voltage swing across devices a and b will be as shown in Figure 29. Any increase in reverse voltage will cause an increase in the reverse current and $V_b{}'$ will increase until the avalanche voltage V_b is reached. Providing that the total voltage applied to both diodes in series is less than the sum of the two avalanche voltages, i.e. $(V_a + V_b)$ the value of reverse current I_R will remain low well within the rating of the devices.

Conventional rectifiers need shunting resistors for steady stage voltage sharing and also capacitors for transient voltage sharing. As avalanche rectifiers have an inherent capability of absorbing reverse power, there is no need for shunting capacitors. In a normal design there will be sufficient reverse power capability existing in diodes connected in series to cope with any transients generated by switching 'on' and 'off' of most of their equipment transformers.

Manufacturers' data sheets provide information on the reverse power rating. The voltage transient energy can be evaluated from the magnetic energy stored in the transformer core. A simple comparison of these quantities will allow the suitability of the devices to be checked.

Parallel Operation of High Voltage Stacks

When running h.v. stacks in parallel two points must be considered: load sharing at the nominal load and load sharing during fault conditions. Typical forward voltage characteristics are shown in Figure 30. The slopes of the minimum and maximum curves are approximate only. (In fact, they curve slightly so that an increase of current does increase the forward voltage drop.) If two diodes are connected in parallel, one having a maximum and the other a minimum forward voltage drop, V_F, Figure 30 shows that at 1.0V forward drop, one diode will take 10A and the other only 6.5A. This unbalance will increase at lower currents, i.e. at 0.8V across two diodes connected in parallel, one diode will take 5A, but the other only 2.5A. Paralleling up strings of diodes will lessen the unbalance; the greater the number of diodes in series, the less inequality.

Several tests were carried out on three strings of devices connected in series. Each string consisted of 20 avalanche diodes, type 1AS029. Table 2 gives a summary of the results. The current measured is the peak current of a 50Hz half sine wave. 'Percentage above mean' figures were obtained from the formula:

$$(B - M)100/M \quad \%$$

where B is the highest current of a string, and M is the total current divided by 3, i.e. ideally shared current per string.

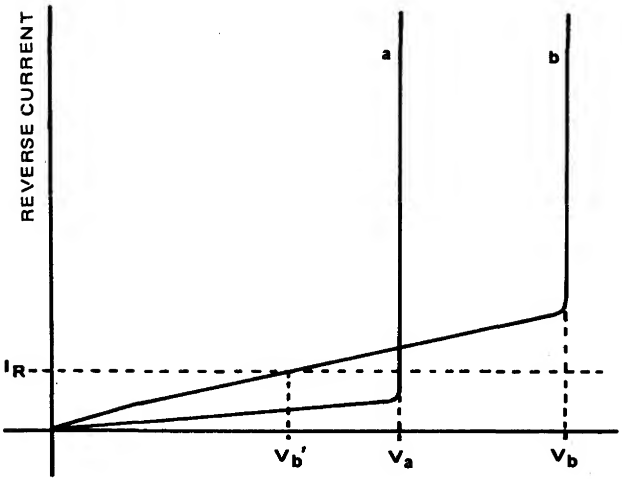


FIGURE 29. Waveforms Across Two Rectifiers in Series

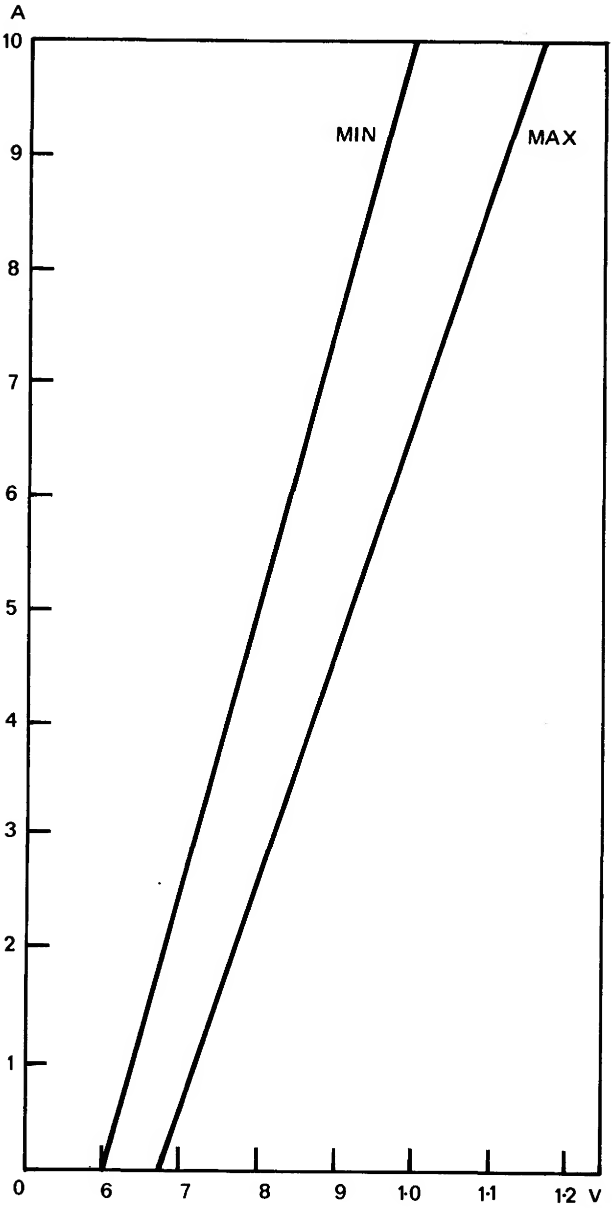


FIGURE 30. Typical Forward Voltage Characteristics

The experienced designer should allow for the possibility of diode failure. To assess the effects of this situation, Table 2 shows, therefore, load sharing between strings with one string having one or two diodes short circuited, i.e. 5% or 10% loss of diodes in one string. Some sort of external forced load sharing must be then introduced to prevent unbalance between strings becoming unacceptable, i.e. exceeding the device rating. An 0.8Ω series resistor, connected with each string gives a satisfactory result for this particular example. As guidance, a series resistor, R_S, which will dissipate 10% of the diode losses, should be used with each string of diodes. For example, a 1AS029 diode is rated at 1.5A average with a typical forward voltage drop 0.87V. Total power dissipation in a 20 diode string will be 20 x 0.87 x 1.5 = 26W. The series resistor then will be $R_S = 2.6/1.5^2 = 1.15\Omega$; Resistor R_S compensates for the unbalance caused by the loss of 10% of diodes in one string. For less than 10 diodes in series, the value of the series resistor should be increased. To illustrate an unbalance between various strings some current traces were recorded and are shown in Figure 31. The effect of an 0.8Ω series resistor is quite noticeable.

Table 2

Total	'a'	'b'	'c'	Percentage above mean	Remarks
14.5	5	4.5	5	2.1	
36.5	12.5	11.5	12.5	2.9	
69.5	23.5	22.5	23.5	1.7	
83.9	28.7	27.6	27.6	3.1	
124.2	41.4	41.4	41.4	0	
142.5	47.5	47.5	47.5	0	
162	54	54	54	0	
21	8.5	6.0	6.5	21.5	One diode is short circuited in string 'a'
59.5	22.5	18.0	19.0	12.5	
89.7	32.5	28.6	28.6	8.3	
123.7	43.7	40	40	6.1	
135.0	50	47.5	47.5	3.6	
18.5	6.5	6.0	6.0	4.8	One diode is short circuited in string 'a' and 0.8Ω resistors are added to each string
39	13.5	12.5	13.0	3.8	
63.5	21.5	21.0	21.0	2.4	
86	30	28.5	27.5	4.3	
107	36	36	35	1.4	
145	48.8	48.7	47.5	1.1	
22	10.5	5.5	6.0	44	Two diodes are short circuited in string 'a'
55	22.5	16.0	16.5	20.3	
77	31.0	22.5	23.5	20.0	
107	41.0	32.5	33.5	15.4	
141	52.4	43.6	45	11.6	
16	6.5	4.5	5	21.4	Two diodes are short circuited in string 'a' and 0.8Ω resistors are added to each string
39.5	14.0	12.5	13.0	6.6	
62	21.5	20.5	20	4.1	
74.5	26.0	25.0	23.5	5.3	
119.5	41.0	40.0	38.5	3.1	
147.5	50	50	47.5	1.8	

Three Phase Bridge Design

Theory:[5] One of the most common connections for h.v. power conversion is a three phase bridge (see Figure 32) where the transformer and silicon rectifiers capabilities are fully utilised. The following design information is based on what is known as the 'Infinite Reactance Theory'. It assumes that each pulse of current is rectangular in form as though a reactance of infinite value is in the d.c. output circuit. It shows good correlation with practical results in polyphase rectifier circuits, but is less accurate in single phase circuits because of an increasing departure from the assumed idealised waveform.

High power circuits, employing semiconductors, invariably use a certain amount of reactance to provide fault current limitation. In most cases the reactance values vary between 5% and 10%. The voltage drop, caused by the reactance, cannot be ignored and must be taken into account for accurate circuit design. As the current waveforms in rectifier circuits are not therefore sinusoidal it would be rather difficult to establish the correct voltage loss due to the presence of reactance. 'Infinite Reactance Theory' offers a solution to this problem. An overlap angle present in rectifier circuits and proportional to the a.c. reactance causes a reduction in d.c. voltage output which can be calculated, see Figure 33. The voltage drop occurs only during the period of overlap and it is this feature which is the main difference between this method and the orthodox design calculations. In the latter the a.c. reactance is neglected as it is considered to be too small to make any appreciable difference, or calculated as an a.c. input drop.

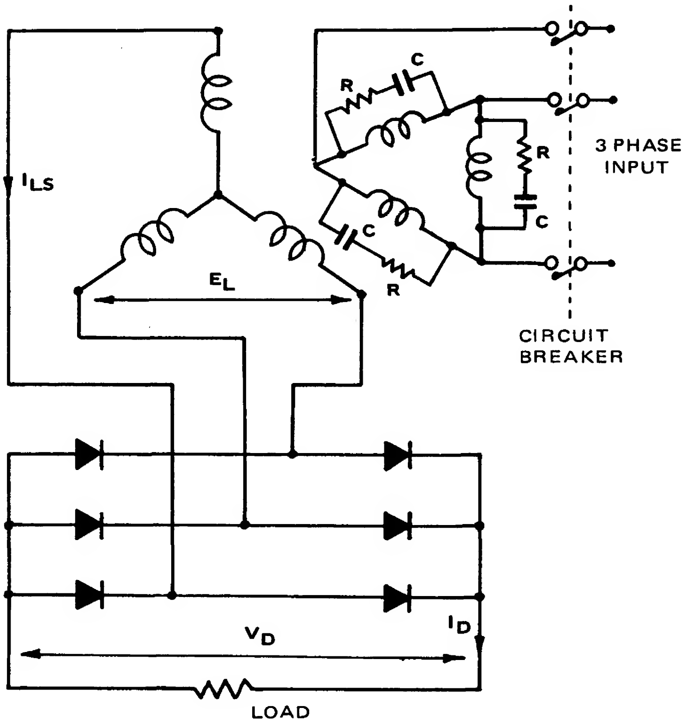
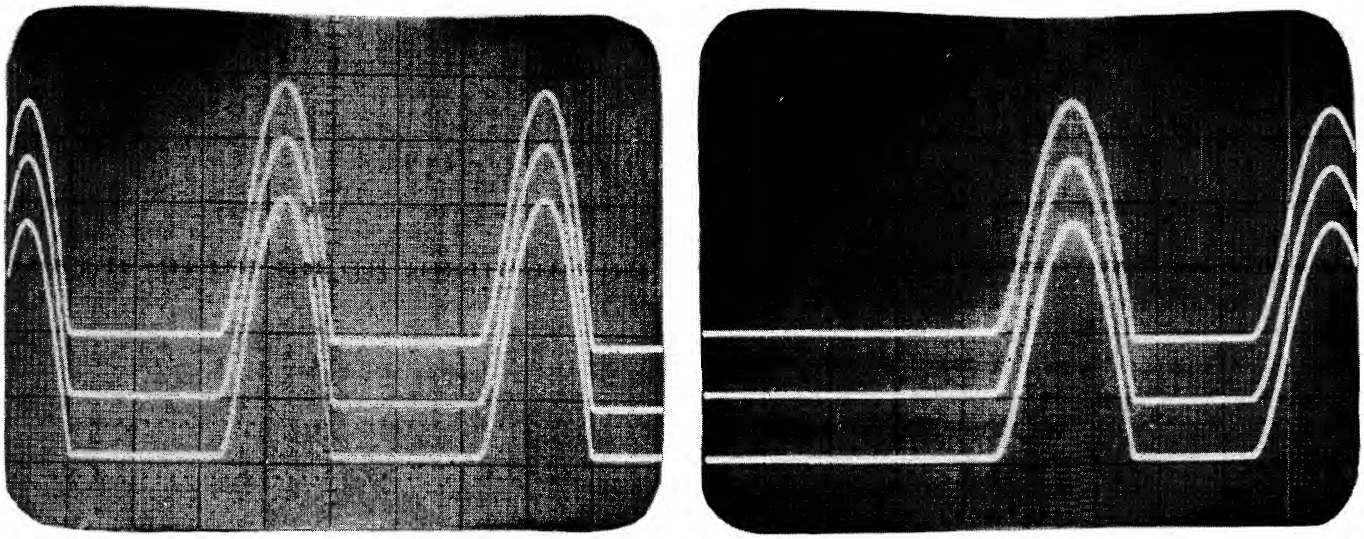
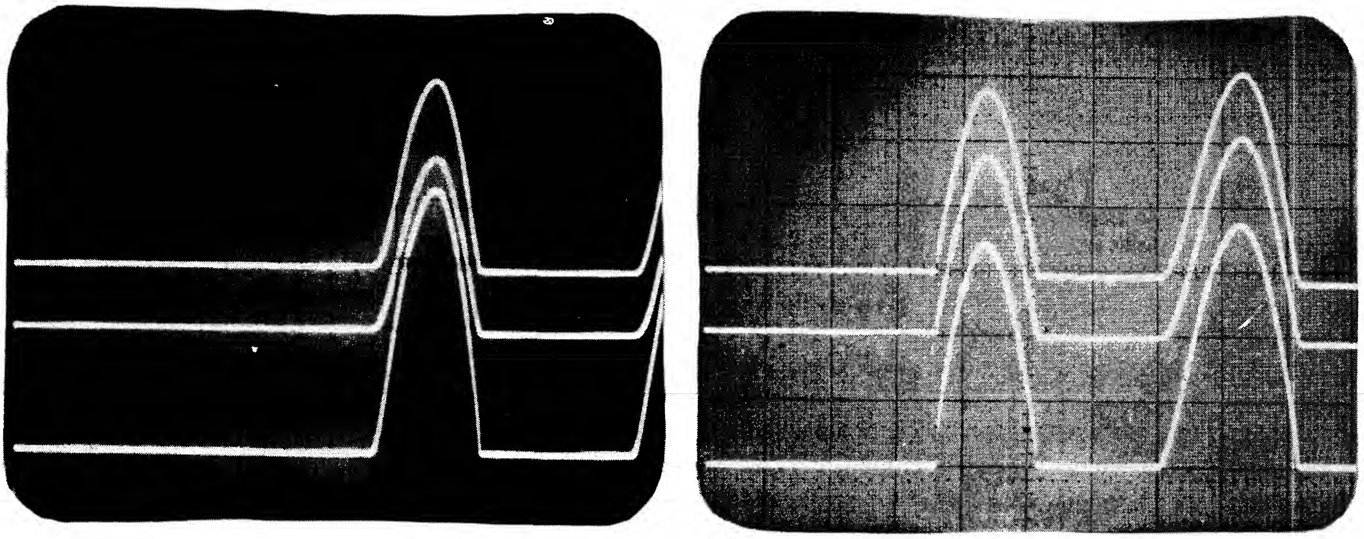


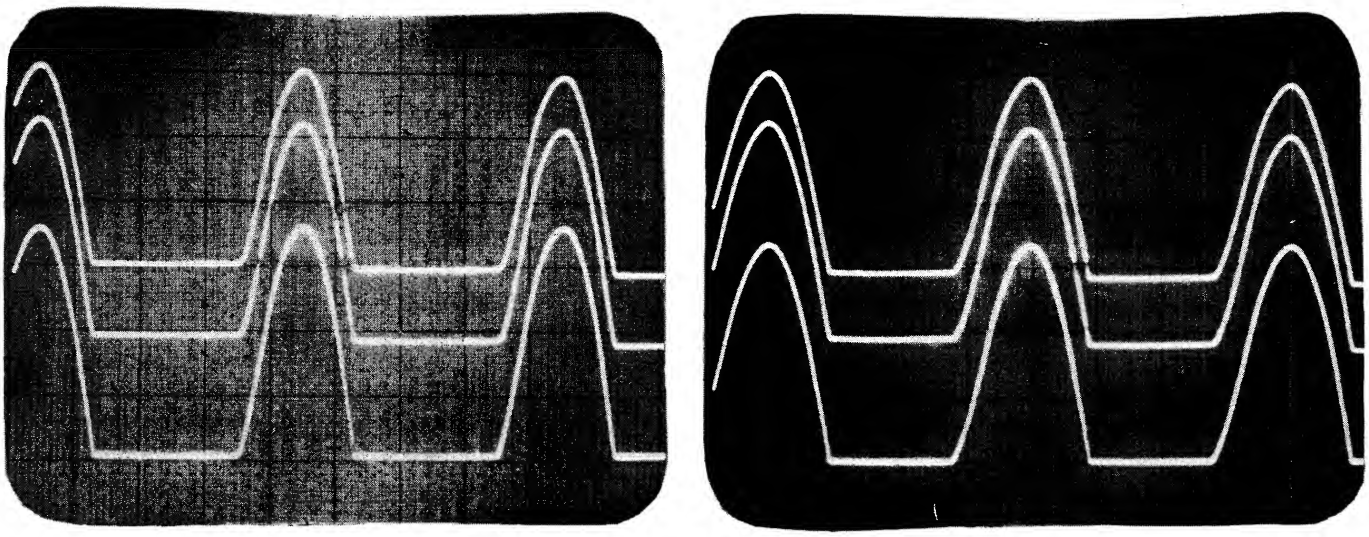
FIGURE 32.



(a) LOW CURRENT 5A/cm ↑ (b) HIGH CURRENT 12.5A/cm ↑



(c) LOW CURRENT 2 DIODES SHORT CIRCUITED 5A/cm ↑ (d) 2 DIODES SHORT CIRCUITED 12.5A/cm ↑



(e) 2 DIODES SHORT CIRCUITED + 0.8Ω RESISTOR 5A/cm ↑ (f) 2 DIODES SHORT CIRCUITED + 0.8Ω RESISTOR 12.5A/cm ↑

FIGURE 31. Waveforms of Fault Current Through 20 Diode H. V. Stacks

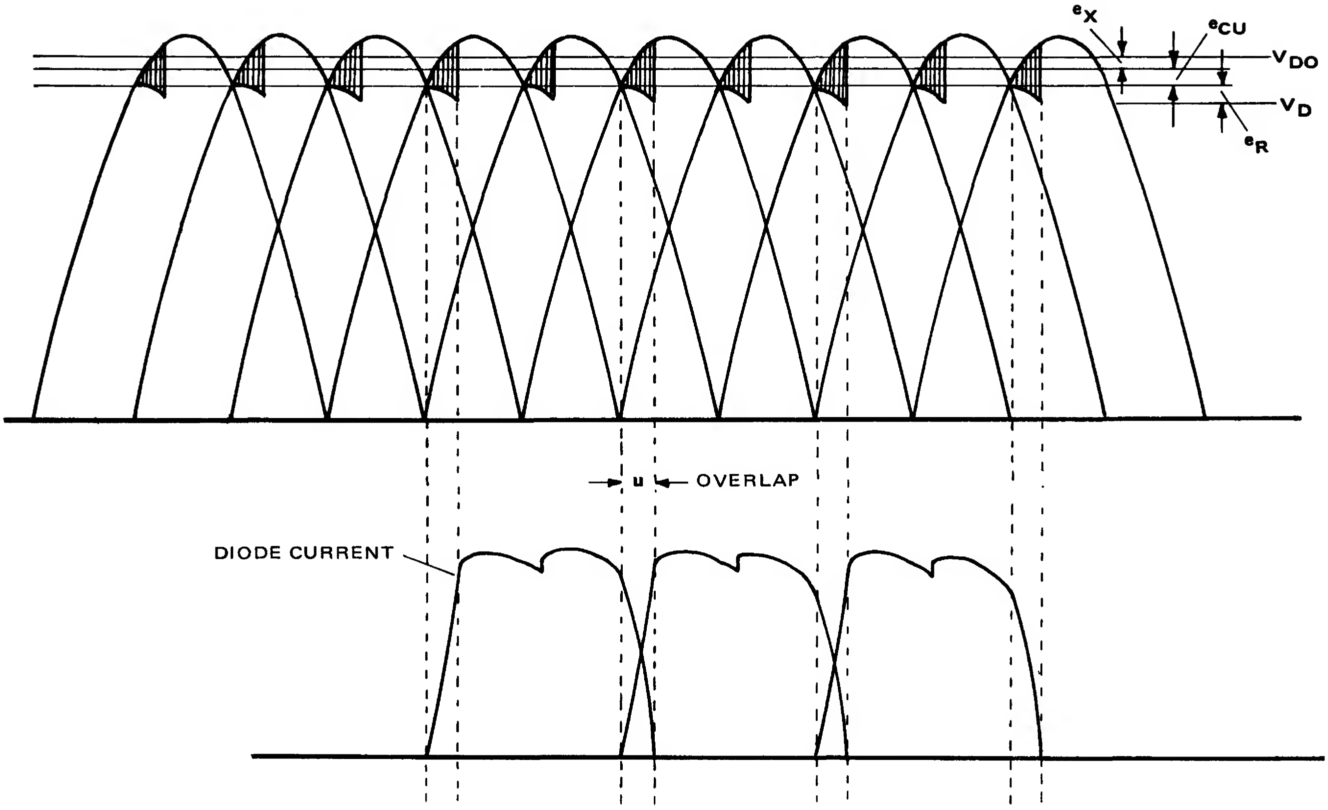


FIGURE 33. Current and Voltage Waveforms

The following equation must be satisfied:

$$V_{DO} = V_D + e_X + e_R + e_{CU} \qquad (1)$$

where

V_{DO} = Theoretical no load d.c. voltage

V_D = Full load d.c. voltage

e_X = D.c. reactive voltage drop (during commutation) due to the presence of transformer leakage reactance and supply reactance.

e_R = D.c. voltage drop (total) in the rectifiers.

e_{CU} = D.c. voltage drop due to the presence of resistance in the circuit, including copper loss

Now

$$e_X = (X_T + X_S).\,V_{DO}/200 \quad . . . . . . \quad (2)$$

where X_T = percentage transformer reactance referred to the primary kVA

$$e_{CU} = \text{total circuit power loss due to resistance}/I_D \quad . . . . \quad (3)$$

where I_D = D.c. current in amps at full load.

From equation (1) and (2) V_{DO} can be determined.

$$V_{DO} = (V_D + e_R + e_{CU})/[1 - (X_T + X_S)/200] \qquad (4)$$

$$E_{LO} = V_{DO}/1{\cdot}35 \quad . . . . \quad (5)$$

where E_{LO} = Secondary r.m.s. voltage between lines at no load.

$$I_{LS} = I_D \times 2^{1/2}/3^{1/2} \quad . . . . \quad (6)$$

where I_{LS} = rectifier transformer secondary r.m.s. line current

Primary transformer rating = secondary transformer rating = $1{\cdot}05 \times I_D \times V_{DO}/1000$ kVA . . . . (7)

The Fault Current:[6] This has been assumed to be limited only by the leakage reactance of the transformer and supply. When switching on to a fault condition, it can be observed that the first pulse of the current is larger than that of the steady state short circuit. This is due to the asymmetry (asymmetrical pulse) caused by the presence of a reactance. The amplitude of the asymmetrical pulse depends on the ratio R/X of the system and can be established from Figure 34. It can also be seen from Figure 34 that the maximum asymmetrical pulse can be double the peak value of steady state short circuit current for an a.c. infinite reactance system. For practical purposes, account must be taken of an asymmetrical pulse when dealing with

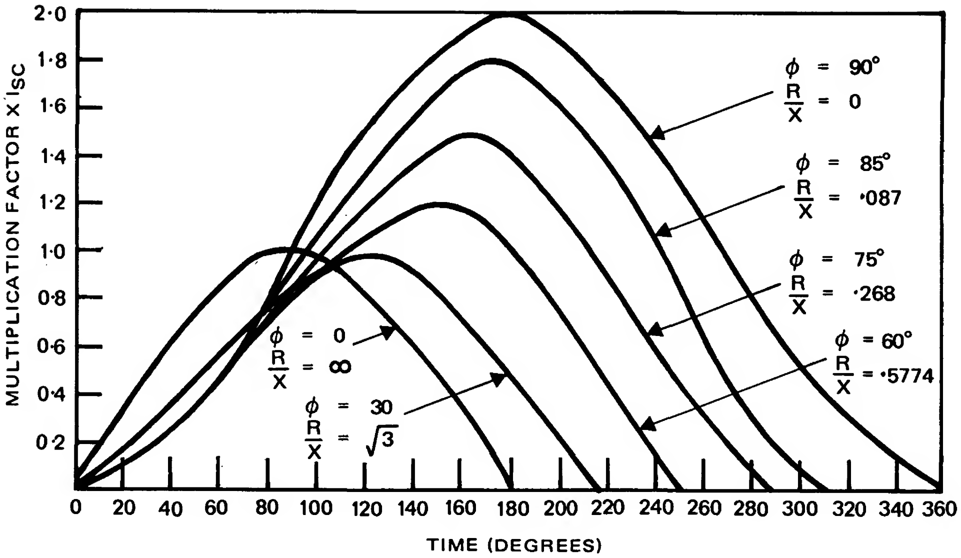


FIGURE 34. First Pulse Current Waveform

up to, for instance, only 3 or 4 pulses. In longer periods the steady state pulses will swamp the effect of the asymmetrical pulse.

$$I_{SC} = I_D \times 200/3^{½}(X_T + X_S) \; . \; . \; . \; . \; . \; . \quad (8)$$

where I_{SC} is short circuit peak current

Efficiency: The accepted way of calculating efficiency in larger equipments is by a summation of losses.

$$\text{Efficiency} = \eta$$
$$= [1 - \text{losses}/(\text{power output} + \text{losses})]\ 100\% \quad (9)$$

In calculating the efficiency the losses of the transformer, rectifier and auxiliaries should be included. The losses in the rectifier diodes will depend upon the overall load current and will be equal to:

$$P_R = I_D \times 2 \times V_F \times n \; . \; . \; . \; . \; . \; . \; . \; . \; . \quad (10)$$

where

P_R = total rectifier losses in the three phase bridge

V_F = forward voltage drop across one diode at current, I_D

n = number of diodes connected in series

Power Factor: For practical purposes the only important value of the power factor of the current drawn from the supply is the power factor of the fundamental or cos ϕ], where ϕ is the angle by which the fundamental component of current lags the supply voltage. It is this value that will be measured by instruments. The total power factor is the product of the displacement factor (due to the fundamental) and of the distortion factor (due to the harmonics), the latter being of theoretical interest only. The evaluation of the power factor depends upon the following relationship:

$$\cos u = 1 - 2e_X/V_{DO} \; . \; . \; . \; . \; . \; . \; . \; . \; . \quad (11)$$

$$\tan \phi_1 = (u - \sin u.\cos u)/\sin^2 u \quad . \; . \; . \; . \; . \quad (12)$$

where u is the angle of overlap (see Figure 33). From the value of tan ϕ_1, cos ϕ_1 can be obtained and by applying this to the curves of Figure 35 for varying amounts of percentage magnetising current, the power factor of the

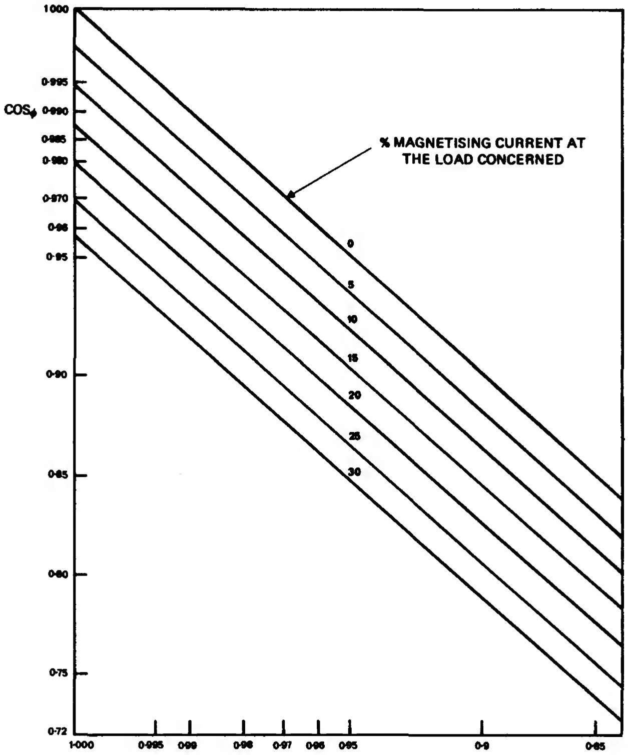


FIGURE 35. Effect of Magnetising Current on Cos ϕ

fundamental cos ϕ can be established. The magnetising current taken represents a percentage of the full load primary current. If, therefore, the power factor is to be calculated for any other load current, it must be remembered that the magnetising current percentage must now be based on the new primary current. For example, if the full load magnetising current is taken as 5%, the magnetising current percentage at half the primary current would become 10%. In the case of e_X, the d.c. reactive volt drop, this will be directly proportional to I_D, the output current.

Protection: To ensure the satisfactory operation of equipment using semiconductor devices the problem of protection against possible excessive voltage transients and excessive currents must be solved. Earlier, the capabilities of avalanche diodes to absorb large powers in the reverse direction was discussed. Therefore, for normal applications of h.v. stacks, there is no need for further steps to be taken. However, in some cases, when frequent switching is taking place, e.g. induction or dielectric heating, a simple CR network, connected across the primary windings of the transformer will help to suppress excessive voltage transients. Recommended values for voltage transients suppression are shown below and connections are given in Figure 32.

$$C = 350\, I_M/E_P \quad \mu F \quad \ldots\ldots\ldots (13)$$
$$R = 100/C \quad \Omega \quad \ldots\ldots\ldots (14)$$

assuming a 50Hz supply
where I_M is the magnetizing current in amps.
and E_P is the primary supply line voltage.

Surge currents are easier to evaluate than voltage transients and they can be controlled by a circuit design as described in the fault current paragraph. By choosing the correct value of transformer leakage reactance, the peak fault current can be kept below a safe value for the devices. Circuit breakers, contactors and fuses are normally used to protect semiconductor equipments against overloads and short circuits. Contactors, not having fault breaking capabilities, are normally backed up by fuses. Circuit breakers, however, do not require fuses. In order to withstand an inrush current to a transformer, the fuses in the input side of the transformer are usually rated at twice or three times the nominal current. Therefore, protection against the d.c. faults becomes more difficult. On the other hand, the fuses on the secondary side of the transformer may be rated very near to the full load current. This is not always convenient, especially for h.v. equipments, as the fuses become rather expensive. When fuses or breakers are adapted for the protection of silicon devices, correct discrimination can be achieved by keeping below the rectifier overload curve at every point by either fuse or breaker characteristics. A knowledge of $i^2.t$ (let through energy) values is very useful in cases when a fault current is expected to be interrupted within ten milliseconds. In this time interval, the i^2t can be assumed to be approximately constant. A simple comparison of the rectifiers i^2t with total fuse i^2t will give the rating of the fuse needed.

Practical Example

Rectifier Transformer Requirements: Rectifier power equipments to deliver 10A at 12kV, i.e. 120kW for an induction heating load.

$I_D = 10A$
$V_D = 12kV$

Let us assume $X_T = 7\%$ and $X_S = 1\%$.

From equation (8) $\quad I_{SC} = 10 \times 200/3^{1/2} \times 8 = 145A$

Assuming the copper loss = 2%, i.e. 2 x 120/100 = 2·4kW

The ratio of the percentage of equivalent resistance due to the copper losses to the total percentage reactance (i.e. 2/8 = 0·25) gives the multification factor for obtaining peak asymmetrical current from Figure 34 which here is 1·5. Therefore, the peak asymmetrical current is 145 x 1·5 = 218A.

Connecting 3 x 1·5A H.V. stacks in parallel will give, including a 10% unbalance, 218 x 1·1/3 = 80A per stack, which is well within the surge rating of a 1AS029 avalanche rectifier.

It is now necessary to find the theoretical no load d.c. voltage, V_{DO}. Considering a stack consisting of 20 avalanche diodes connected in series with, say, 1.0V drop per diode,

$$e_R = 2 \times 20 \times 1 = 40V$$

$$e_{CU} = 2400/10 = 240V \qquad \text{from equation (3)}$$

$$\therefore V_{DO} = (12{,}000 + 40 + 240)/[1 - (7+1)/200] \qquad \text{from equation (4)}$$
$$= 12800V$$

Check:

$$e_X = (7 + 1) \times 12800/200 = 512V \qquad \text{from equation (2)}$$

$$\therefore V_{DO} = 12000 + 512 + 40 + 240 = 12792, \text{ i.e. } 12800 \qquad \text{from equation (1)}$$

Note that the d.c. reactive voltage drop $e_X = 512V$ which cannot be ignored when designing rectifier equipments.

Now other transformer details can be found.

$$E_{LO} = 12{,}800/1{\cdot}35 = 9{,}500V \qquad \text{From equation (5)}$$

$$I_{LS} = 10 \times 2^{1/2}/3^{1/2} = 8{\cdot}2A \qquad \text{From equation (6)}$$

Rating of the transformer = 1·05 x 10 x 12,800/1000
= 134·4kVA $\quad$ From equation (7)

Check

Rating of the transformer is also $= 3^{1/2} \times E_{LO} \times I_{LS}/1000\text{kVA}$

$= 3^{1/2} \times 9{,}5000 \times 8{\cdot}2/1000$

$= 135\text{kVA}$

The specification for the transformer can now be written

Connections:	delta/star
Primary supply	440V, 3 phase, 50Hz
Secondary open circuit	
Line voltage	9500V
Secondary full load current	8·2A rms
Leakage reactance	7%
Assumed copper losses	2·4kW
Ambient temperature	30°C

Figure 36 shows the d.c. voltage regulation of the equipment.,

H.V. Stacks: There are two points for consideration in selecting rectifiers, i.e. the voltage and current ratings. The maximum peak voltage expected from the transformer is $9500 \times 2^{1/2} \times 1{\cdot}1 = 14800\text{V}$, assuming a 10% rise in supply voltage. Allowing 35% above this figure for safety, stacks capable of withstanding 20kV will be needed. Twenty avalanche rectifiers, type 1AS029, rated at 1000V each and connected in series are well suited for this application. The current rating of 1AS029 devices has been partly discussed. First, the asymmetrical peak current expected during a fault is 80A and the nominal current per stack is $10 \times 1{\cdot}1/3 \times 3 = 1{\cdot}22\text{A}$ mean both inside the rating of 1AS029 devices. Normally, equipments of this power would have a circuit breaker in the input to the transformer to cope with any overloads or fault currents. The speed of operation of an a.c. circuit breaker is about 60ms, i.e. 3 cycles in a 50Hz system. Taking into account the safety factor, the stacks should be capable of withstanding the fault current for at least 5 cycles, i.e. 100ms. In the example the value of the steady state fault current is $145 \times 1{\cdot}1/3 = 54\text{A}$. allowing 10% for unbalance. This value is again within the rating of the devices. As discussed, a loss of devices will necessitate an additional series resistor connected to each stack. The value of this resistor can be evaluated from:

$$R_S = 20 \times 0.875/10 \times 1{\cdot}5 = 1{\cdot}17\Omega \text{ say } 1{\cdot}2\Omega$$

Summing up:

Three h.v. stacks will be connected in each arm of a three phase bridge giving a total of 18 stacks.

A 1·2Ω series resistor is added to each stack.

Each stack will consist of 10 1AS029 avalanche rectifiers.

Efficiency: From equation 10 –

$P_R = 10 \times 2 \times 1{\cdot}0 \times 20 = 0{\cdot}4\text{kW}$

As the copper losses are = 2·4kW

The total losses = 2·8kW

$\therefore$ From equation (9) $\eta = [1 - 2.8/122.8]\,100\%$

$= 97.7\%$ at full load

Total losses at half load = $(0{\cdot}4/2) + (2{\cdot}4/4) = 0{\cdot}8\text{kW}$

Approximately d.c. voltage at half load = $12000 + 800/2$

$= 12400\text{V}$

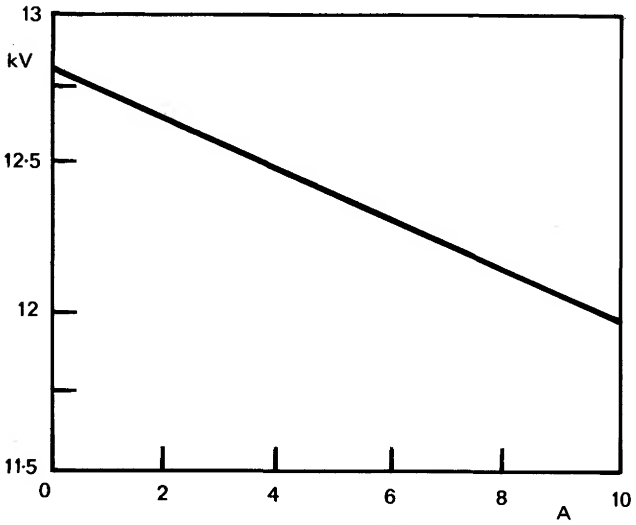


FIGURE 36. Regulation Curve

See Figure 36.

The output power at half load = $12400 \times 5/1000 = 62\text{kW}$

$\therefore$ Efficiency = $[1 - 0{\cdot}8/62{\cdot}8]\ 100\% = 98{\cdot}7\%$ at half load.

Power Factor: From equation 11 –

$\cos u = 1 - 2 \times 512/12800 = 0{\cdot}916$
$\therefore u = 23^\circ\ 36 = 0{\cdot}413$ rad
From equation (12)
$\tan \phi_1 = (0{\cdot}413 - 0{\cdot}4 \times 0{\cdot}916)/0.16 = 0{\cdot}3$
$\therefore \phi_1 = 17^\circ$
$\cos \phi_1 = \cos 17^\circ = 0{\cdot}956$

Assuming the magnetising current = 2·5%, from Figure 35, $\cos \phi$, the displacement factor, is 0·95 at full load.

At half load:

$\cos u = 1 - 2 \times 256/12800 = 0.959$
$u = 16^\circ 24' = 0.286$ rad

$\tan \phi_1 = (0.286 - 0.282 \times 0.050)/0.282 = 0.2$

$\phi_1 = 11^\circ 24'$, $\cos \phi_1 = 0.98$

and from Figure 35 $\cos \phi = 0{,}97$ (the magnetising current for half load is 5%)

Protection: As the equipment is supplying an inductive heating load an R.C. network connected in the primary winding of the transformer has been added.

The primary current

$I_P = 134{\cdot}4 \times 1000/3^{1/2} \times 440 = 176\text{A}$
$I_M = 2{\cdot}5 \times 176/100 = 4{\cdot}4\text{A}$
$C = 350 \times 4{\cdot}4/440 = 3{\cdot}5\mu\text{F}$ From equation (13)

and the series resistor
$R = 100/3{\cdot}5 \simeq 28{\cdot}5\Omega$ From equation (14)

As discussed, the stacks selected for the equipment are within their capabilities for the first symmetrical pulse, as well as for the steady state short circuit current for the time of 100ms. The circuit breaker selected must be able to open at up to 60ms to give a sufficient safety margin for satisfactory generation.

REFERENCES

1. Blundell, A. J., Kinman, T. H., Hibberd, R. G. and Williams, J., 'Silicon Power Rectifiers' *Proc. I.E.E.* Part A, Vol 108, No. 40, 1961.

2. Weidelich, D. L.: 'Voltage Multiplying Circuits', *Electronics*, 1941, Vol. 14, No. 5.

3. Weidelich, D. L.: 'Analysis of Full-Wave Rectifier and Capacitive-Input Circuits', *Electronics*, 1947, Vol. 20, No. 9.

4. Schade, O. H.: 'Analysis of Rectifier Operation', *Proc. I.R.E.*, 1943, Vol. 31, No. 7.

5. Read, J. C.: 'The Calculations of Rectifier and Inverter Performance Characteristics', *I.E.E. Proceedings*, 1945.

6. Budek, J. A. and Marchant, A. H.: 'Protective Methods for Silicon Rectifier Equipment', *Direct Current*, Nov. 1964.

II USE OF HIGH-VOLTAGE SWITCHING TRANSISTORS

by
Ken Salmon and Mick Maytum

The use of high-voltage power transistors in switching applications is practical and well established, the most common usage being in the horizontal sweep circuit of television receivers and inverters. The transistors are designed to withstand the large transient dissipation inherent in high-current, high-voltage switching circuits and will give effective and reliable operation in properly designed circuits.

The transistor structure differs in several ways from that of low-voltage power transistors and the resultant changes in the switching characteristics require new circuit techniques to ensure reliable operation. In order to understand the effects that this structure has on the transistor switching performance and circuit arrangement, the basic construction of high-voltage transistor is first explained and then an indication given of how their parameters and drive requirements are affected.

The horizontal line output circuit of a television receiver is used as an example of a switching circuit to show the method of using the transistor as, although the control of switching is important in all applications, the requirements of the line output circuit present one of the most difficult applications. The transistor switches scan coil current and generates the e.h.t. supply at a repetition frequency of approximately 15 kHz with a transistor case temperature which may rise to 80°C. This and the other applications of the device require careful control of the switching waveforms and information is given to enable the circuit designer to achieve this control in any switching circuit.

The circuit requirements, the transistor ratings, and the methods of use and measurement are described to enable the circuit designer to select the appropriate device and components for his application. Photographs of actual switching waveforms are included to clarify the difference between good and bad circuits.

CONSTRUCTION

An understanding of the structure limitation of high voltage transistors substantially enhances the performance which can be derived by the designer. Figure 1 shows the relative region widths for two power transistors. The low voltage epitaxial base transistor is typified by a shallow collector n region whose bulk resistance is negligible. As voltage requirements increase, the voltage sustaining collector increases dramatically both in depth and resistivity, so that for the 2200V transistor illustrated in Figure 1, there is an increase in collector depth of 15 times that of the 200V device and a bulk resistance of 50Ω.

The common emitter characteristics for a 200V transistor are shown in Figure 2, which demonstrates that any resistive components are negligible compared with the junction voltage, both in the saturation region where the collector base is forward-biased and in the active region where that junction is reverse-biased.

The effect of the 50Ω bulk collector resistance might be expected to produce the characteristic shown in Figure 3.

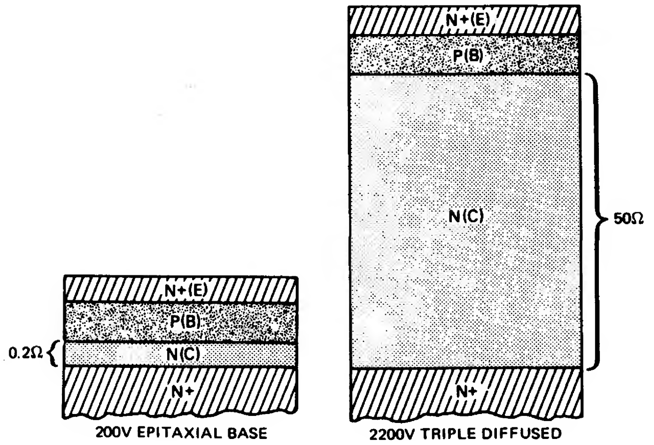


FIGURE 1. Typical Transistor Cross Sections

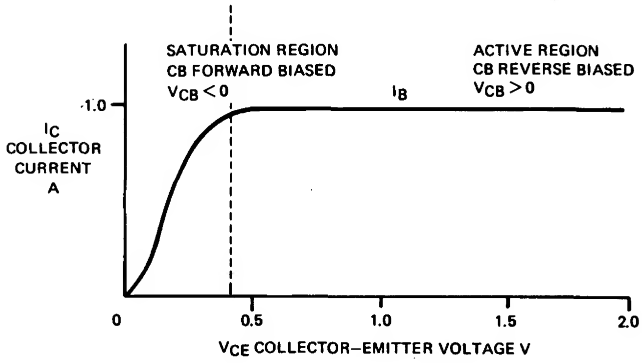


FIGURE 2. Common Emitter Characteristic of 200V Transistor

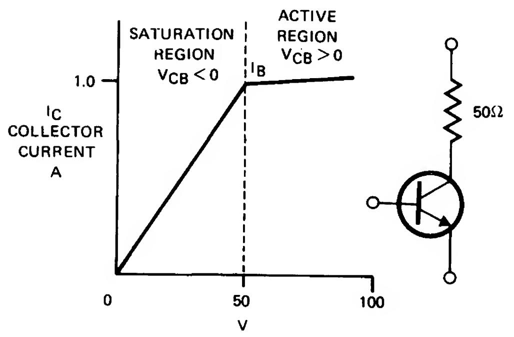


FIGURE 3. Composite Characteristic with External 50Ω Resistor

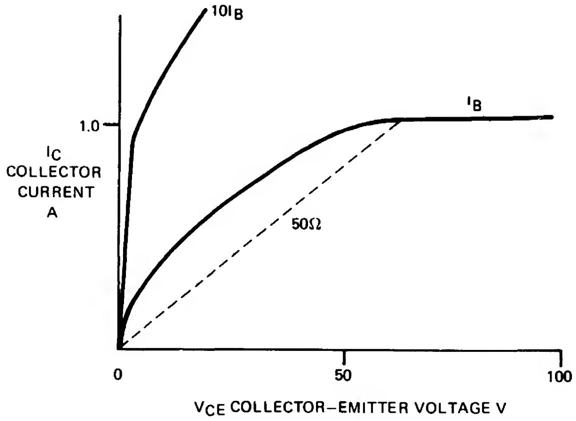
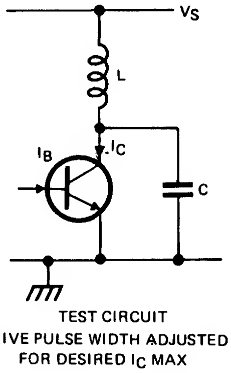


FIGURE 4. Common Emitter Characteristic for 2200V, 2A Transistor

The practical characteristics in Figure 4 show that indeed the line of 50Ω plus V_{BE} would provide a locus of points for $V_{CB} = 0$, however, in the saturation region, i.e., $V_{CB} < 0$, much lower voltages are obtained. The accepted explanation is that in saturation, the forward bias on the collector base junction produces a condition of 'high level injection' into the high resistivity collector which, within the constraints of space charge neutrality, result in a severe conductivity modulation of the region. Varying levels of saturation produce varying degrees of conductivity modulation so that when the device is just out of saturation the full effect of the high bulk resistance is apparent. For the 2200V transistor illustrated, this point would be when $V_{CE} \approx 50V$ (approx.) with a collector current of 1A. Thus, when the transistor is driven very hard into saturation, the collector resistance can be reduced to a negligible level which is obviously the requirement when the device is used as a switch. The resulting large quantities of stored charge accumulated in the collector region restrict device switching performance, and although this may be controlled by the base drive, the principles applied must comprehend that the collector region predominates in high voltage transistors.

EFFECT ON PARAMETERS

In a number of applications it is 'turn off' which is of prime interest since the collector current is at a maximum at this point. A high voltage transistor operating with an inductive load is shown in Figure 5, along with the typical waveforms obtained, Figure 6. Capacitor C limits the voltage at the transistor collector. The period of maximum dissipation is at 'turn off' when the collector current is falling and the collector emitter voltage is rising rapidly. When the base drive is first removed, after a period of conduction, the collector current continues to rise in the load, until the stored charge in the device is insufficient to maintain emitter injection. At this point, the collector current starts to fall. The period between starting to remove the base drive and the collector current falling to 90% of its peak value is commonly referred to as the storage time, t_s. During 'turn off', the base ceases to inject into the collector. The current flows are such that the collector base junction may be regarded as a diode in recovery, with the stored charge in the collector providing a source of majority carriers into the base. A relatively small majority carrier current in the base is required to maintain the emitter injection and this can be satisfied by the carrier flow from collector to base, providing this flow is greater than the reverse base drive, $I_{B(off)}$. During the storage time, the stored charge in the collector is constantly reducing. When the net inflow of majority carriers into the base from the collector is less than the net outflow in the form of $I_{B(off)}$, then emitter injection can no longer be maintained. This marks the onset of the collector current fall time, t_f. The part of the 'turn off' defined as t_f is normally taken as the time during which the collector current, I_C, falls from 90% to 10% of the peak value. With high voltage transistors, the time taken to fall from 10% to 0% can be several times greater than the 90% to 10% value and with a rapidly rising collector voltage, dissipation associated with this period can be very large. Thus comprehension of fall time 90% to 0% is essential.



TEST CIRCUIT
DRIVE PULSE WIDTH ADJUSTED FOR DESIRED IC MAX

FIGURE 5. Switching Circuits

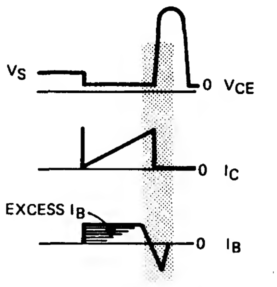


FIGURE 6. General Waveforms

It has been shown that the collector current starts to fall when $I_{B(off)}$ is greater than the majority carrier current into the base from the collector. Therefore, t_s will vary as the rate of fall of base drive dI_B/dt is changed. The effects of this are shown in Figure 7. With a high value of dI_B/dt a high level of reverse base drive is reached quickly. This will result in an early termination of the t_s period with large

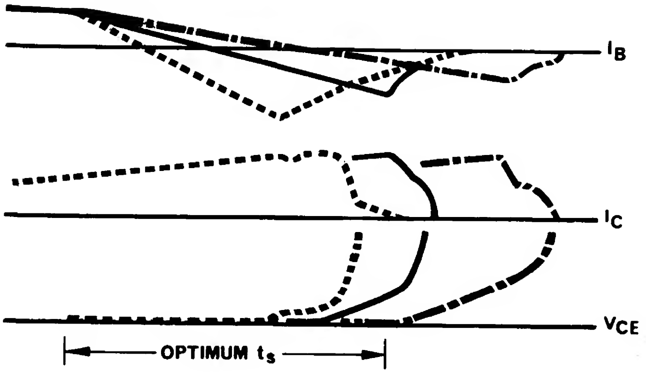


FIGURE 7. High Voltage Transistor Switching Characteristics – Effect of t_s

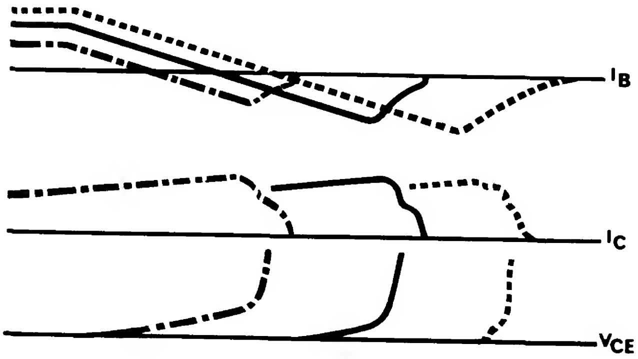


FIGURE 8. High Voltage Transistor Switching Characteristics – Effect of Base Current I_B

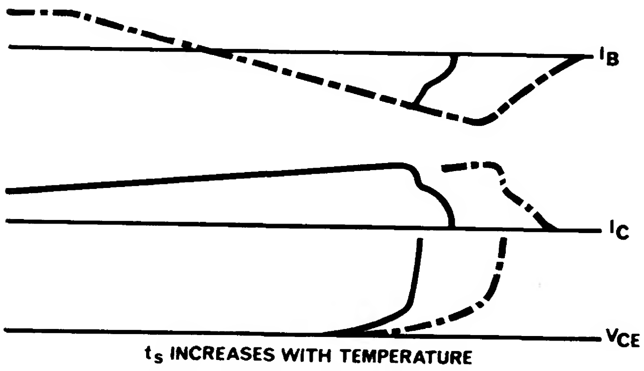


FIGURE 9. High Voltage Transistor Switching Characteristics – Effect of Temperature

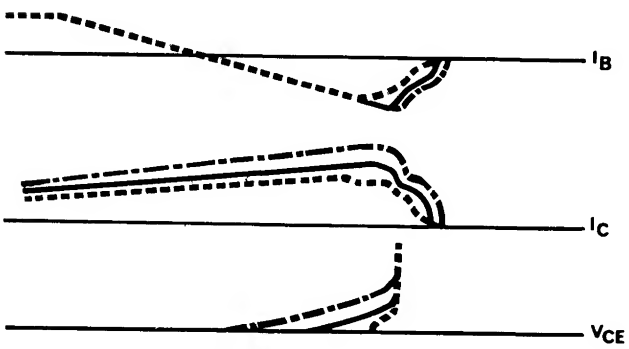


FIGURE 10. High Voltage Transistor Switching Characteristics – Effect of Collector Current I_C

quantities of stored charge remaining in the collector region. An increase in t_f will result, particularly during the latter part, producing a tail on the waveform which is characteristic of incorrectly driven high voltage transistors. Using a very low value of dI_B/dt extends the storage time. The reducing stored charge during this period causes a decrease in the conductivity modulation of the collector region, therefore increasing V_{CE} and dissipation. Under these conditions, in the fall-time period, the lower level of reverse drive removing the remaining stored charge results in an increase in t_f. However, t_f increases due to low values of dI_B/dt are not as significant as those due to high values of dI_B/dt but the dissipation incurred during the storage time with a low dI_B/dt can be very large. The ideal value for dI_B/dt, therefore, minimizes device dissipation during the storage time and the fall time.

The forward base drive $I_{B(on)}$ used to saturate the transistor determines the level of collector stored charged. Under-driving causes increases in saturation and storage dissipation, while over-driving can increase both t_s and t_f (see Figure 8). In practical applications, small variations in the waveform during the saturation period can be ignored. A convenient point for measurement is just before the base drive is reduced at turn off, $I_{B(end)}$. Minimizing device dissipation and optimizing switching performance must be major considerations when designing the base drive waveform, and to this end dI_B/dt and $I_{B(end)}$ are considered the critical parameters.

A full explanation of the effects of temperature is very involved, however a simple model of both emitter base and collector base junction injection inefficiencies increasing with temperature will generally suffice. At higher temperatures, this results in a higher level of stored charge in the collector region, for a given base drive, producing increases in both t_s and t_f (Figure 9).

With constant $I_{B(end)}$ and dI_B/dt values, variations in peak collector current can result in the transistor operating well away from ideal conditions (Figure 10). Reduction in I_C particularly causes substantial increases in t_f and device dissipation. Therefore, when optimizing the critical parameters of the drive waveforms, operational variations in collector current must be taken into account as well as maximum operating temperatures.

A CIRCUIT OPERATION

A simplified line output circuit is shown in Figure 11 It consists of the line output transistor VT1 and output and input circuits.

The output circuit comprises the inductor L_C, which simulates the combination of the line output transformer and scanning coils, and the capacitor C_C, which resonates with L_C during the flyback period. The inductor L_H, and the capacitor C_H, are incorporated to shape the flyback voltage waveform by the addition of third or fifth harmonics to which they are tuned. This simulates part of the winding inductance and capacitance in the output transformer.

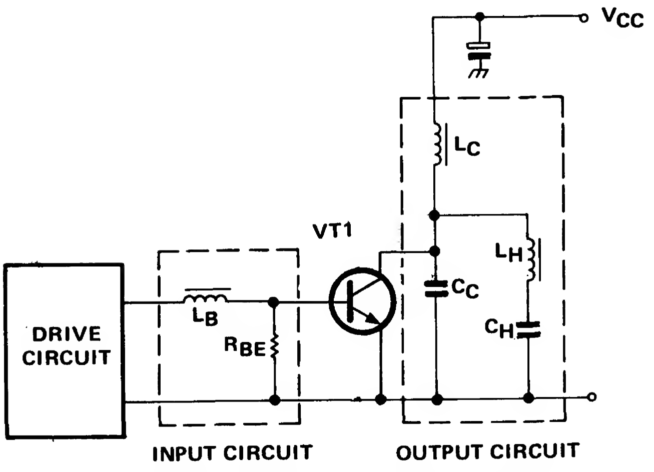


FIGURE 11. Simulated Line Output Circuit

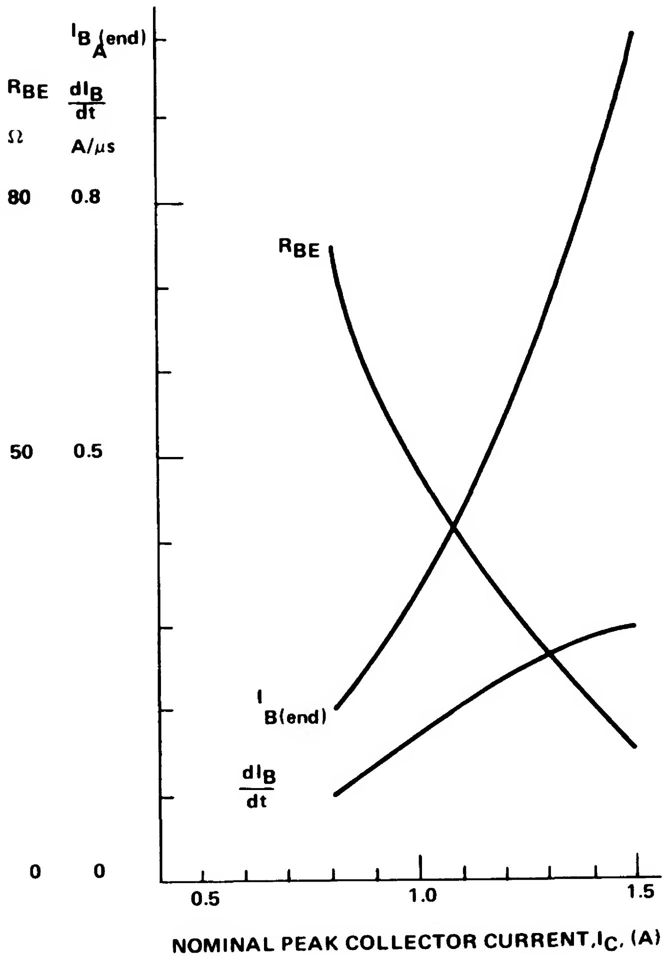


FIGURE 12. BUY71 Recommended Drive Conditions versus Nominal Peak Collector Current for Minimum Dissipation

REGION	ENERGY
1	SURPLUS RETURNED TO SUPPLY
2	BUILD UP TO MAXIMUM REQUIRED
3	SUPPLY TO E.H.T.

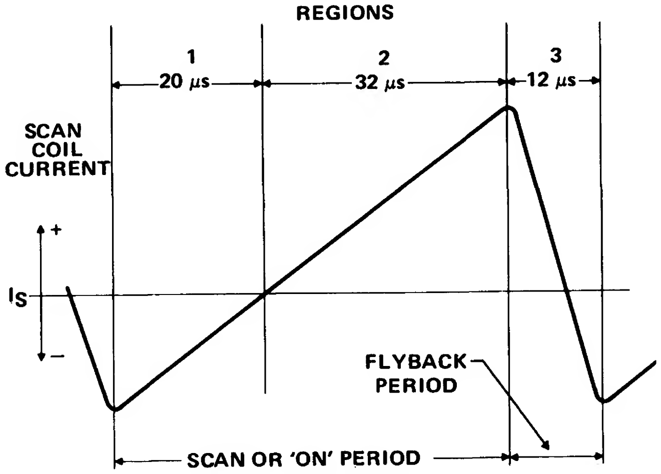


FIGURE 13. Scan/Flyback Cycle

The input circuit comprises the inductance L_B which, together with transformer leakage inductance, controls the shape of the base current waveform during switching, and the resistor R_{BE} which affects the voltage breakdown rating of the transistor and also reduces ringing due to parasitic inductance and capacitance in the circuit. The value of R_{BE} is not critical and a curve of typical values is shown in Figure 12. The current drawn by R_{BE} should be a small proportion of $I_{B(end)}$.

The drive circuit provides an alternating pulse output, supplying positive base current in one part of the cycle and negative bias voltage on the other part of the cycle. The drive circuit is operating at the U.K. line scan frequency of 15.6kHz (625 lines) and the mark space ratio of the combined scan/flyback cycle is shown in Figure 13.

In a television receiver, the drive circuit may consist of an integrated circuit pulse generator with an output transistor controlling the driver transformer. In this manner, an alternating drive is available but the transformer design is determined by the particular needs of the circuit.[1] To improve versatility in testing transistors, a simulated driver circuit is used which removes the need for special transformers. A simulated drive circuit is shown in Figure 14 but in normal circuit development, the drive circuit will evolve out of the input specification and is unlikely to need either the versatility or the complexity of the circuit shown. It is intended to guide the device user and is not a fully engineered circuit.

Figure 13 also shows the energy transfer system in the line output circuit whereby energy is built up in the inductance L_C during the 'on' period, and transferred to and from the resonating components, C_C, C_H, and L_H, during the 'off' period.

Any surplus energy not consumed by losses during switching or by dissipation in the e.h.t. circuit will be returned to the supply through the inversely biased transistor immediately after the flyback period. This reverse current flow takes place in the first part of the scan period and contributes to the total transistor dissipation.

TRANSISTOR RATINGS

The specific ratings required of high-voltage switching transistors are closely related to the needs of the circuit and, in the case of the line output transistor, the rating of the transistor must match the volt-ampere requirements of the cathode ray tube. Colour receiver tubes have greater volt-ampere requirements than black and white tubes and consequently make greater demands on the rating of the line output transistors. The current rating required is mainly determined by the design of the scan coils and the voltage rating by the e.h.t. generation circuits. This combination of high current and voltage and continuous switching creates a power dissipation problem and, because all these factors are interrelated, it is necessary to examine each in detail.

Current

In general, a transistor may be used up to the maximum data sheet ratings of current, voltage, dissipation, etc. The current rating necessary to use the transistor in line scanning circuits is explained below.

The horizontal and vertical movement of the electron beam in the television tube is controlled by the scanning coils which surround the neck of the tube. The basic requirement in line scanning is to obtain the sweep by generating an approximately linear change in scan coil current and it is one of the functions of the line output circuit to produce this current in the coils.

By suitable choice of coil inductance, this current change is derived from a constant voltage applied to the coil when the line output transistor is 'on'.

The current rating of the transistor is determined by the size and characteristics of the wafer and header and the type of circuit in which it will be used. In switching applications such as the line output scanning circuit the current rating required is the peak value of the collector current during the time when the transistor is saturated.

Voltage

The voltage rating of the high-voltage switching transistor is determined by the choice of h.t. voltage and the peak voltage generated during switching an inductive load. This may be unwanted leakage inductance or the chosen inductance of a line output transformer as described herein. To obtain the high-voltage rating, the transistors are designed with a 'thick' collector of high resistivity material. The transistor wafer incorporates new process methods to give a high-voltage rating and enable the device to withstand reverse voltages which may be greater than 2 kV. During the 'off' period, when the collector voltage rises to its peak value, the base of the transistor should be negatively biased with a few volts. Hence, the breakdown voltage rating is determined using an appropriate BV_{CEX} bias voltage with a low source resistance.

In a television receiver, the shaping and duration of the flyback voltage pulse is important in determining the e.h.t. characteristics. These characteristics are influenced by the values of the components C_C, L_H, and C_H.

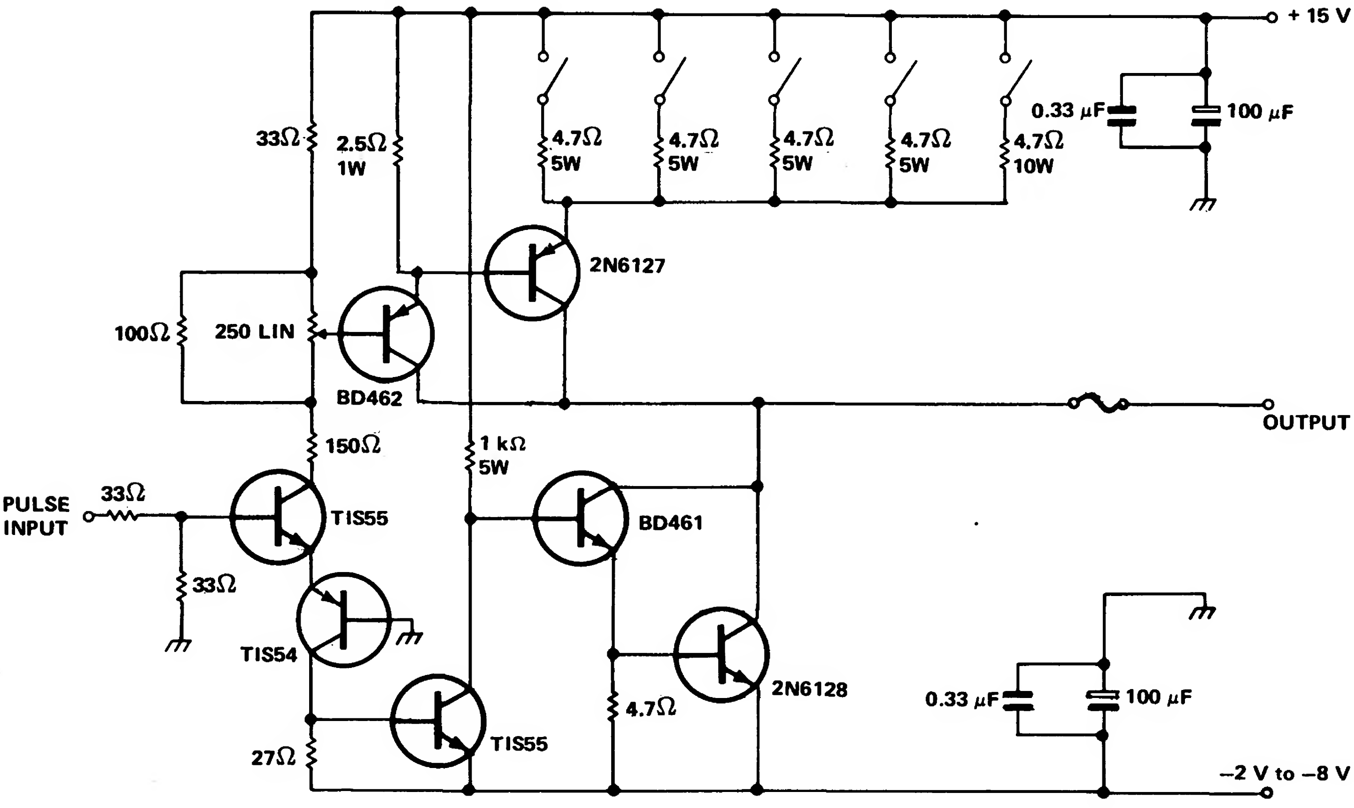


FIGURE 14. Simulated Line Driver Stage

The value of capacitor C_C is chosen to resonate with the inductor, L_C, to give the required peak flyback voltage and time period. Components L_H and C_H are normally part of the parasitics of the line output transformer but in the simulated circuit they are selected to give third or fifth harmonic tuning so that the voltage pulse has its shape modified to improve the energy content and the regulation of the e.h.t. generating circuit.

Power

In all transistor switching circuits, the device dissipation can be considered to be made up of three components, i.e., the 'on', the 'off', and the 'transition' periods. However, the total dissipation is usually integrated over the complete operating cycle by the header and the heatsink. The heatsink must be designed for continuous dissipation in the relevant ambient temperature. In a television receiver case, this temperature may rise to 80°C under certain conditions and poses a severe problem unless the line output circuit is designed for minimum dissipation and the heatsinking arrangements are adequate.

The 'on' component of heat dissipation is the integrated product of the saturation voltage, $V_{CE(sat)}$, and the collector current during the 'on' period. Also present during most of the time when the device is 'on', is the base drive power. For reasons to be explained, this power is larger than that needed to saturate low voltage power devices as the base current is usually not less than 0.25 $I_{C(peak)}$ and may rise to 0.75 $I_{C(peak)}$ in some cases.

The 'off' component of heat dissipation is relatively low, comprising leakage current while the device is sustaining the 'off' voltage. In the line scan circuit, the time period is approximately one-fifth the total cycle so that the integrated value is very small and may be ignored in calculating heat losses.

The dissipation which occurs during the transition from the 'on' to the 'off' period is the largest component of the total heat loss and is dependent on the transistor characteristics and the control exerted by the circuit design. The transient dissipation during switching is determined by the rise of collector voltage as the device comes out of saturation and the simultaneous flow of the collector current as it drops from peak value to zero during the fall-time. The shape of the collector current fall is critical in determining transient power loss and this shape must be carefully controlled by the characteristics of the drive and output circuits. Thus, the major dissipation is dependent on the control of switching and it is this need to control the switching which makes the high-voltage switching circuit different from most low-voltage switching circuits where there may be little or no inductance.

SWITCHING REQUIREMENTS

An effective switch must have a low 'on' resistance and in a transistor this means a low saturation voltage, $V_{CE(sat)}$, when the transistor is passing its maximum current. This condition is obtained when the voltage drop across the collector load forces the collector base diode into forward-bias and usually necessitates a large base current input.

In high-voltage transistors, the situation is made difficult because the large diffused mesa structure gives the required rating but, as discussed, has considerable collector body resistance.[2] This internal collector resistance can vary from 5 Ω to 500 Ω depending on the type of device and in a BUY71, a typical value would be 30 Ω to 50 Ω. The normal solution to obtain fast switching and high voltage is to use gold doping and epitaxy but the demands of the high-voltage power switching transistor prevent the use of these processes. The solution to the problem requires a technique to reduce the effects of collector body storage and this is done by carefully controlling the charge in the collector by regulating the charge in the base.

The internal resistance readily forces the collector base diode into forward bias but leaves a high voltage across the device terminals which is impossible to tolerate in power switching circuits. This internal resistance can be greatly reduced by passing large amounts of charge into the collector via the base. This process is known as 'conductivity modulation' and when fully charged, the collector resistance may fall to an ohm or two, giving an external $V_{CE(sat)}$ of 5 V to 10 V which is acceptable.

However, the transistor cannot be switched off until the collector charge has been removed and it is for this reason that conventional switching techniques are inapplicable because these assume that most of the excess charge necessary for saturation is in the base region. The removal of charge from the collector of a high-voltage transistor must be carried out, as stated, by the reduction of base current at a rate which allows sufficient time for the charge to be removed under controlled conditions. While the charge removal is in process, collector current continues to flow and the transistor remains in a nearly saturated condition although there will be a small increasing external saturation voltage.

When the excess collector charge has been removed, the external voltage begins to rise more rapidly and the current falls. When the collector load has inductance, the onset of current fall causes magnetic flux reversal in the inductance and there is a rapid rise in collector voltage as the inductance tries to maintain the current. When driving a line output transformer, the inductive surge is deliberate and the voltage generated is stepped up to provide the e.h.t. supply in the television receiver. The transistor is designed to withstand the high voltage, provided the switching conditions are satisfactory.

The time necessary to remove the excess stored charge, i.e., the storage time, is a function of collector characteristics and is related to the excess collector charge and the external and internal impedances of the transistor and its embedding components. It is convenient to measure this in a practical circuit, such as the line output stage, by measuring on an oscilloscope the interval between the start of base current reduction and the onset of fall of collector current. This delay period creates a phase difference, between the drive circuit and the output waveforms, which must be taken into account when designing circuits for continuous switching.

CONTROL OF BASE CURRENT

The control of base current can be accomplished in various ways, the simplest of which uses a series inductance in the base circuit with a rectangular waveform supplied from the drive circuit. In a line output circuit, the drive can be obtained from an integrated circuit type SN76544 line and frame processor, an amplifier and transformer at a frequency of approximately 15 kHz. The alternating output is rectangular giving positive base drive current for approximately 28 μs and a negative biasing voltage for 36 μs. During the 28 μs drive period, energy is stored in the inductance L_B and when the drive reverses, this stored energy gives an almost linear fall in base current as the voltage across the inductor is constant at approximately $(V_{off} + V_{BE})$. Choice of L_B and V_{off} can give a range of values of dI_B/dt which can be selected to give optimum storage time and hence satisfactory switching waveforms. The value of $I_{B(end)}$ is also critical and must be chosen to give an acceptable $V_{CE(sat)}$ during the 'on' period.

In the test circuit, the base drive is derived from a pulse generator followed by a power amplifier which gives constant current pulses during drive and negative biasing voltage when the drive is removed. A further refinement is the addition of R_S and C_S to shape the drive pulse in order to simulate actual operating conditions. The amplitude and characteristics of the base drive pulse are critical in determining overall switching performance and dissipation during the 'on' and 'transient' period. The measuring system is designed to permit a variety of drive conditions in order to optimize the transistor operating conditions.

MEASUREMENT PARAMETERS

The following parameters are critical in the design and specification of high-voltage switching transistors:

$I_{C(peak)}$	Maximum collector current
$I_{B(end)}$	Base current
I_S	Mean supply current
V_S	Supply voltage
$V_{C(peak)}$	Maximum collector voltage
V_{off}	Reverse biasing voltage
t_f	Fall time (90%-10% I_C)
t_s	Storage time
dI_B/dt	Rate of change of I_B during t_s
T_C	Transistor case temperature

The following section describes the methods of measuring these parameters and the system for optimizing the choice of conditions and components.

MEASURING SYSTEM

The parameters listed are set up or measured in a circuit which duplicates, as far as possible, the conditions in a practical high-voltage circuit. To simulate a difficult environment, the transistor is mounted on a heatsink giving a high case temperature and is switched at approximately 15 kHz. The drive pulse supplying base current I_B is shaped to resemble that normally obtained from a drive transformer having parasitic leakage reactance and winding capacitance. However, for convenience in evaluation, a transformer is not used. All the components are either selected values or adjustable. Measurements of time periods are made using a calibrated oscilloscope with a trace expand

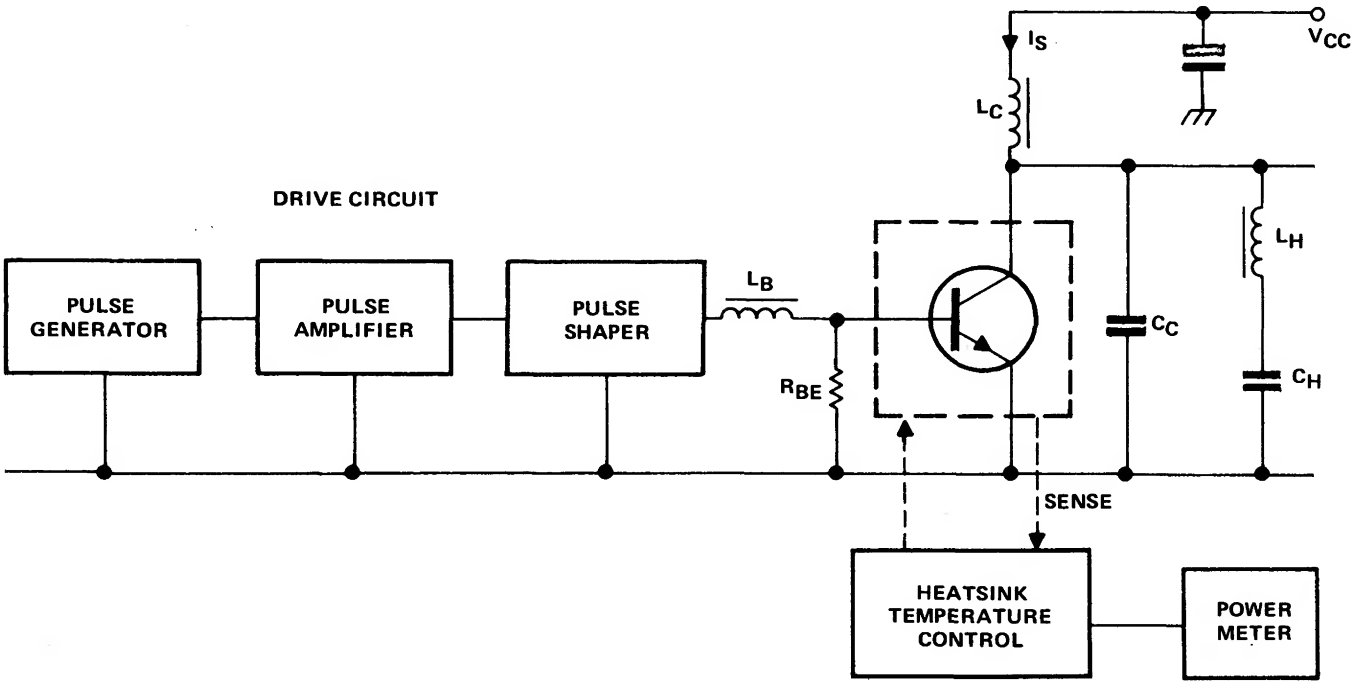


FIGURE 15. Measuring System Block Diagram

facility. Power dissipation in the transistor under test cannot be measured directly, but can be determined by the two methods described. The first is the measurement of the mean product of the supply current and the H.T. voltage, though this power measurement includes component losses. The power dissipation in the transistor under test may also be measured by a substitution method, even though this will include some error by assuming that one heat source is directly equivalent to another. A block diagram of the total measuring system is shown in Figure 15. The voltage current and time measuring points are shown in Figure 16.

MEASUREMENT PROCEDURE

The device to be measured is placed in the jig which clamps it tightly to the heatsink. The power control to the test jig heaters is regulated to give the required case temperature, e.g., 80°C, which is measured with a thermocouple. The base drive to the device is switched on and adjusted to give the required levels of $I_{B(end)}$, V_{off} and an acceptable pulse shape and length. The collector supply is now switched on and by monitoring the collector voltage and current waveforms, final adjustments are made to the drive circuits to ensure correct operation and timing. The circuit parameters can now be measured.

Collector Current

Collector current is measured using a current probe. The critical factors in this measurement are the shape and time length of the current fall from 90% to 10% of the peak value and the storage time, which is the interval between the end of the base current pulse, $I_{B(end)}$ and the start of the collector current fall. The fall-time is measured using an expanded time base, giving accuracy of about 0.1 μs. Where stray voltage pick-up is a problem, it may be necessary to insert the probe into the 'earthy' side of the output circuit, as shown in Figure 16.

Base Current

Base current is measured using a current probe and its amplitude and pulse length are set up before the collector supply is switched on. A value of $I_{B(end)}$ is chosen to ensure that the external saturation voltage on the transistor is low enough to prevent excessive dissipation during the 'on' condition. This value is approximately 20% to 80% of the required value of collector current. The drive pulse length is approximately 28 μs.

Collector Voltage

Collector voltage can rise to over 2 kV on devices such as BUY71 and BDX31 and requires care in the safety aspects of measurement. Its peak value is measured using a high-voltage probe on the oscilloscope and in the simulated circuit described, the time period is adjusted to be 11 to 12 μs, corresponding to the television line scan circuit flyback time. The shape is a half sine when operating with fundamental resonance when capacitor C_C resonates with inductor L_C. However, the shape can be modified using third or fifth harmonic tuning using additional components L_H and C_H. Figure 17 shows the change in waveforms due to the addition of harmonic tuning.

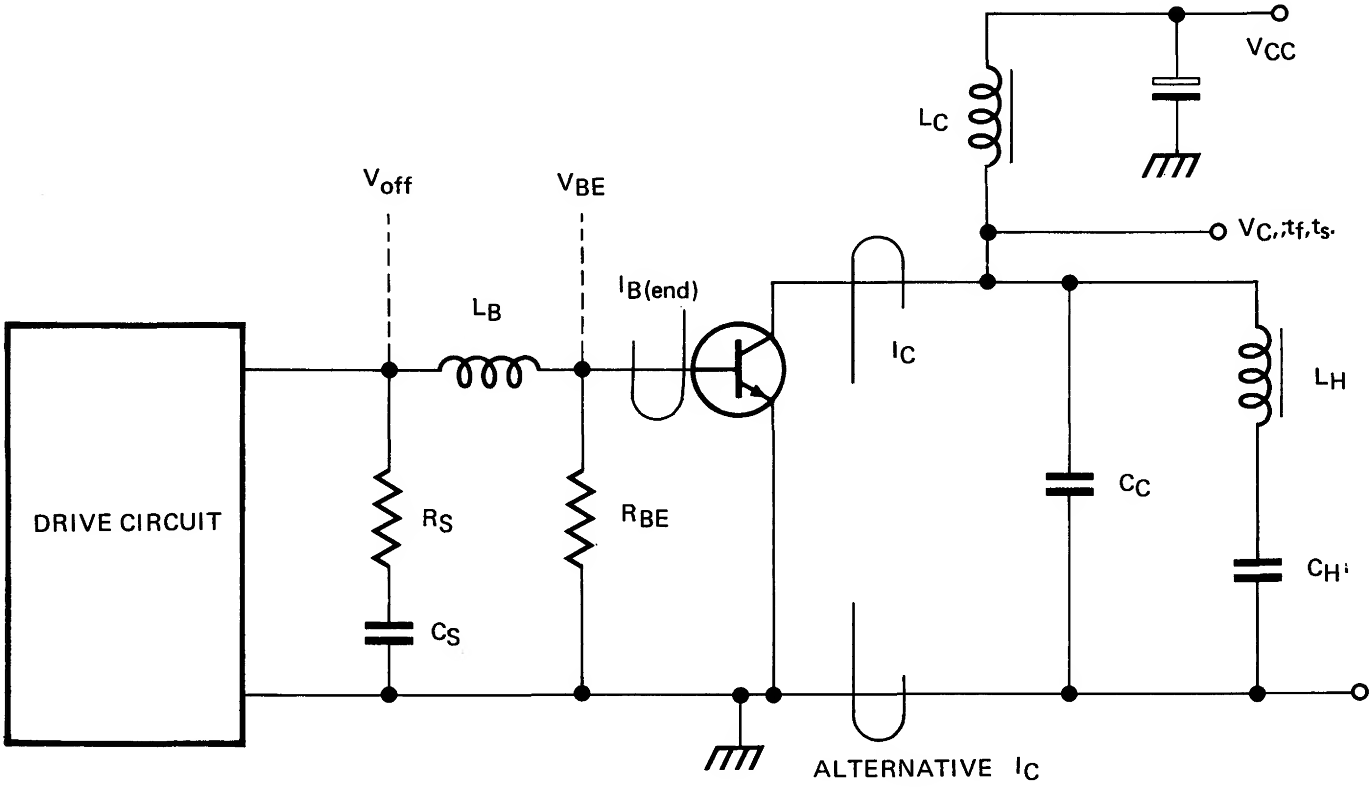


FIGURE 16. Measurement Points

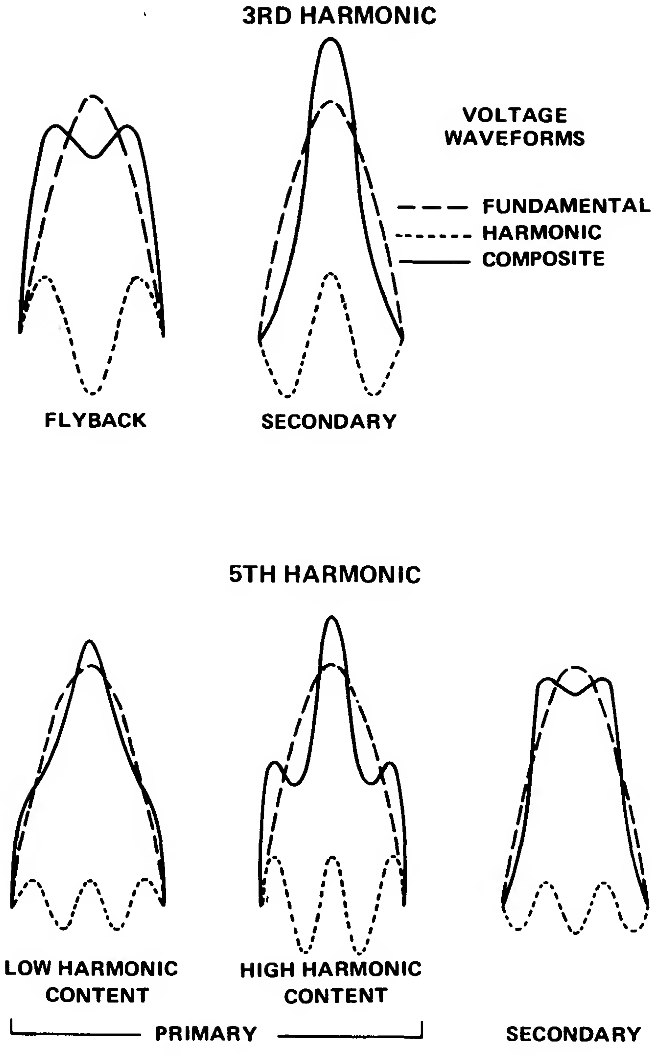


FIGURE 17. Effect of Harmonic Tuning

The external saturation voltage is critical to the design of optimum switching performance waveforms. Particularly important is the rate at which this voltage rises when the transistor switches off, because the simultaneous flow of collector current during this period will give very high transient dissipation.

However, the optimization of circuit parameters and components may not require this voltage be measured, only the losses during switching. If measurements of voltage are required, or if the shape is to be examined in detail, it may be necessary to utilize a back-off voltage or a clamping technique to obtain accuracy of measurement. The collector voltage at this point in the operating cycle may be only 0.25% of the peak value and increasing the sensitivity of the oscilloscope to improve accuracy of measurement may cause amplifier saturation and distortion.

One possible method for avoiding this problem uses a fast clamping diode connected across the probe output to restrict the peak voltage to about 700 mV. The diode capacity, ≈ 1.5 pF, must be compensated on the probe to avoid distortion of the waveform. The compensation is imperfect, but the errors due to diode storage occur on the trailing edge of the pulse, which is not measured.

DEVICE DISSIPATION

The magnitude of the peak current and voltage and the high ratio of peak-to-mean values make it very difficult to measure power losses in any of the circuit elements or the transistor by direct methods. However, two methods are used to evaluate the losses and to guide the circuit designer to the optimum choice of components.

Substitution Method

The transistor being measured is mounted on a heatsink to conduct the heat generated in the wafer into the sink via the header. The heatsink is designed to maintain the transistor case (header) temperature at a value which gives an acceptable junction temperature and hence reliable operation. In the test circuit, the heatsink is constructed with a second power source on it so that the sink temperature may be raised up to a value (80°C) corresponding to the possible temperature which it may attain in actual working conditions. If the power used for heating the sink is measured, it is possible to apply a substitution method to determine the losses in the transistor under test as follows:

> Adjust the heatsink power to the level necessary to provide the required sink temperature or the transistor case temperature, with the transistor mounted in position but not switched on. Note this power level (P_1).
>
> Switch the transistor on and reduce the heatsink power until the case or sink temperature is back to the original value. Note the reduced level of heatsink power (P_2).
>
> Subtraction of P_2 from P_1 indicates the change in power required to maintain the sink or case temperature constant and therefore corresponds to the power added by the transistor under test. It can be shown that the difference in thermal resistance is not important, but obviously any change in convection or radiation will upset the result and it is also subject to the inaccuracy of subtracting one relatively large quantity from another. However, experiment has shown that the errors are not excessive and the power loss measured in this way compares favorably with the loss measured by the circuit total loss method.

Circuit Total Loss Method

This method of assessing transistor dissipation is based on the fact that, excluding drive power and assuming a nondissipative load, the power supply current taken by the device and its circuit is directly proportional to the losses in the transistor and the components. If the components are chosen or designed to have low losses, then the product of the mean current input and the constant supply voltage gives a slightly pessimistic value of the transistor dissipation. Some of the component losses can be calculated and taken into consideration in computing transistor dissipation. However, it is clear that the input current is almost proportional to transistor losses and can be used as an indicator in selecting circuit components and parameters. If supply current is plotted against various values of dI_B/dt, it will be apparent that there is a minimum value corresponding to the optimization of switching waveforms and therefore of minimum dissipation.

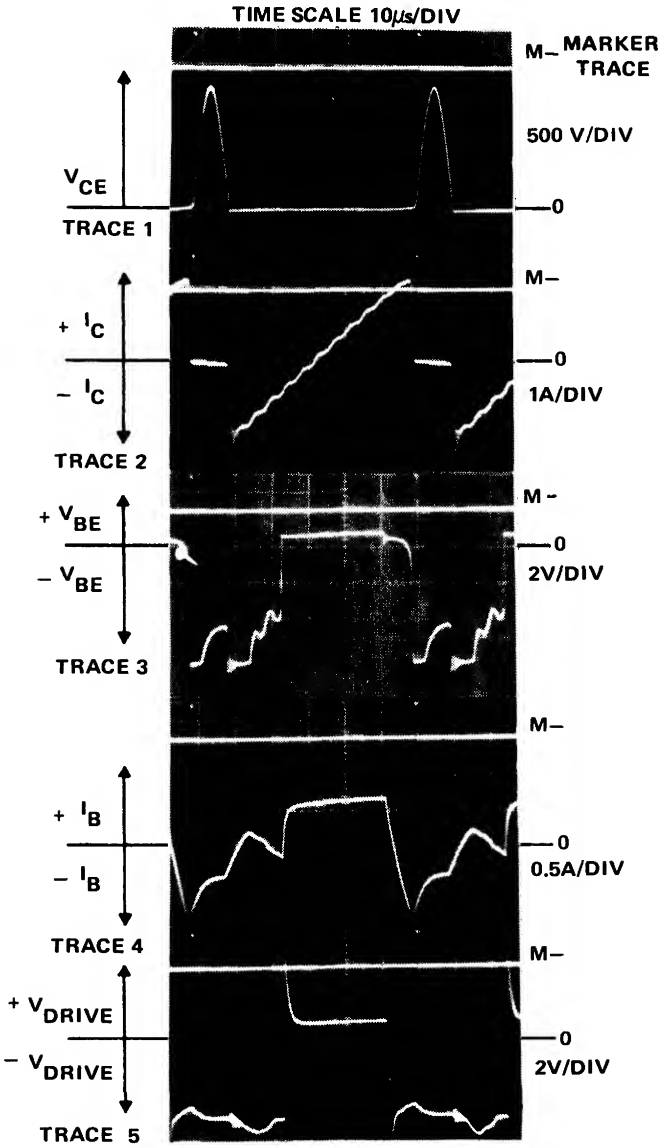


FIGURE 18. Actual Set of Waveforms with Fifth Harmonic Tuning

The minimum level will depend on the particular values of $I_{B(end)}$ and I_C chosen for the application.

ANALYSIS OF WAVEFORMS

Figure 18 shows a set of waveforms obtained by photographing oscilloscope traces. The actual test circuit, Figure 19, is very similar to the circuit shown in Figure 1.

Collector-Emitter Voltage (V_{CE})

Trace 1 (Figure 18) shows the collector voltage excursion having an amplitude of 1750 V and a pulsewidth of 12 µs. The waveform is a half sine wave, slightly modified by fifth harmonic components. The 'on' period between pulses is approximately 52 µs, during which time the transistor is in saturation. A slight rise in the collector-emitter voltage, V_{CE}, will be noticed during the 'on' period as the base current falls and the collector current rises. On switching 'off' the energy acquired by the inductor will be transferred into the capacitor giving the voltage pulse shown in Trace 1:

$$1/2\, LI^2 = 1/2\, CV^2$$

The resonance of L_C and C_C causes the capacitor to return its energy into the inductor until the transistor is turned 'on' again. The energy is now pumped from the inductance into the supply rail, through the transistor. The voltage across the resonant circuit is almost constant at the supply voltage, V_{CC}, while the transistor is saturated. There is a small negative voltage on the collector during the initial part of the 'on' period. This is caused by the energy flow from L_C into the supply rail through the transistor in the reverse of normal direction, i.e., the transistor is acting like a flywheel diode during the first part of the 'on' period. For about 6 µs, the emitter base diode is in breakdown as the peak negative collector current flows from the inductor into the supply rail. The collector base diode remains in forward-bias until the transistor is switched off at the end of the 'on' period. When there is no load on the resonant circuit, the total power dissipated is very small and the peak-negative current will be almost equal to the peak-positive current.

Collector Current (I_C)

Trace 2 of Figure 18 shows an almost linear rise in collector current from peak-negative to peak-positive value while the transistor is conducting during the 'on' period. The ripple on the ascending current is caused by the presence of harmonic tuning elements. Current during the 'off' period is virtually zero. When measuring with a current probe, it is difficult to remove the pick-up effects which may appear to give some current during this period, although the transistor is 'off'.

The ringing at the moment of switch-on is caused by parasitic capacitance in L_C and the transient effect of negative collector current forcing the emitter-base diode suddenly into breakdown. The effect is damped by the resistance R_{BE} and can be clearly seen on Traces 3 and 5.

Drive Voltage (V_{DRIVE})

Trace 5 of Figure 18 indicates the characteristics of the supply used for measurement of the transistor parameters described. It was designed to simulate the conditions required of a practical drive circuit although such a circuit would normally be a much simpler arrangement. The positive voltage is approximately equal to V_{BE} once the base inductor L_B has reached magnetic saturation. The spike at the start of the positive drive period is caused by the initial reactance of the base inductor forcing the constant current supply voltage up to its open circuit value. The amplitude of this spike will be determined by the output impedance of the drive circuit. The negative voltage is approximately V_{off} but is modified by the impedance of the source. This impedance permits the fluctuations in V_{off} due to the base current waveform and the voltage inputs from the base-emitter junction.

Base Current (I_B) and Voltage (V_{BE})

While the drive is positive, current is passed into the base at an almost constant level, reaching a maximum value of $I_{B(end)}$. When the drive is reversed, base current begins to fall, with a rate dI_B/dt controlled by the choice of inductor L_B, and the voltage V_{off}. This fall must continue until the collector charge has been removed. This charge removal causes a reduction in base-emitter voltage and a reduced rate of dI_B/dt. This eventually causes cumulative switch-off as V_{BE} goes negative and the base inductor voltage reverses. Base current I_B now falls from the peak-negative value to zero. The voltage generated by the base inductor forces the base-emitter junction into breakdown for part of the 'off' period. The base current reaches a steady state current determined by the resistances in the base circuit until the transistor is switched 'on' again which forces the base-emitter junction once more into breakdown. During this period, base current is controlled by the factors: reverse voltage V_{off}, ' input ' from the base-emitter junction under the influence of the collector current, the energy state of the base inductor, and the value of resistor R_{BE}

TRANSIENT ANALYSIS

Figure 20 shows the transient effects on I_C and V_{CE} caused by changing the value of dI_B/dt. The collector current fall time and the corresponding rise in V_{CE} as the transistor comes out of saturation are critical to switching performance and hence minimum dissipation. Three values of dI_B/dt are shown for a single value of $I_{B(end)}$ and $I_{C(max)}$ in order to demonstrate the effects of the changes.

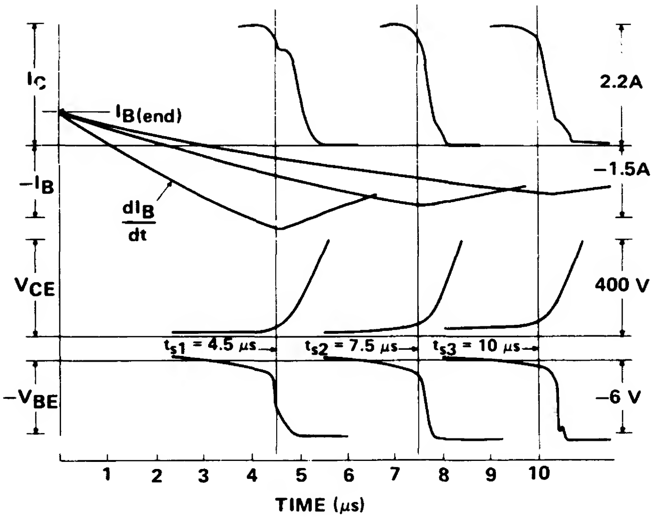


FIGURE 20. Transient Analysis

Before the transistor can be switched 'off', it is necessary to remove the excess charge stored in the collector. The time taken to remove this charge is known as the storage time t_s. Its value will depend on $I_{B(end)}$ and the rate at which the base current is reduced dI_B/dt. The three values of dI_B/dt shown in Figure 20 result in storage times 4.5µs, 7.5µs and 10µs respectively.

At the end of storage time the outflow of majority carriers (the base current) exceeds the inflow carriers injected from the collector body into the base region. Thus the base charge cannot sustain $I_{C(max)}$ and collector current begins to reduce. As this reduction takes place the collector depletion layer moves into the collector body enabling the

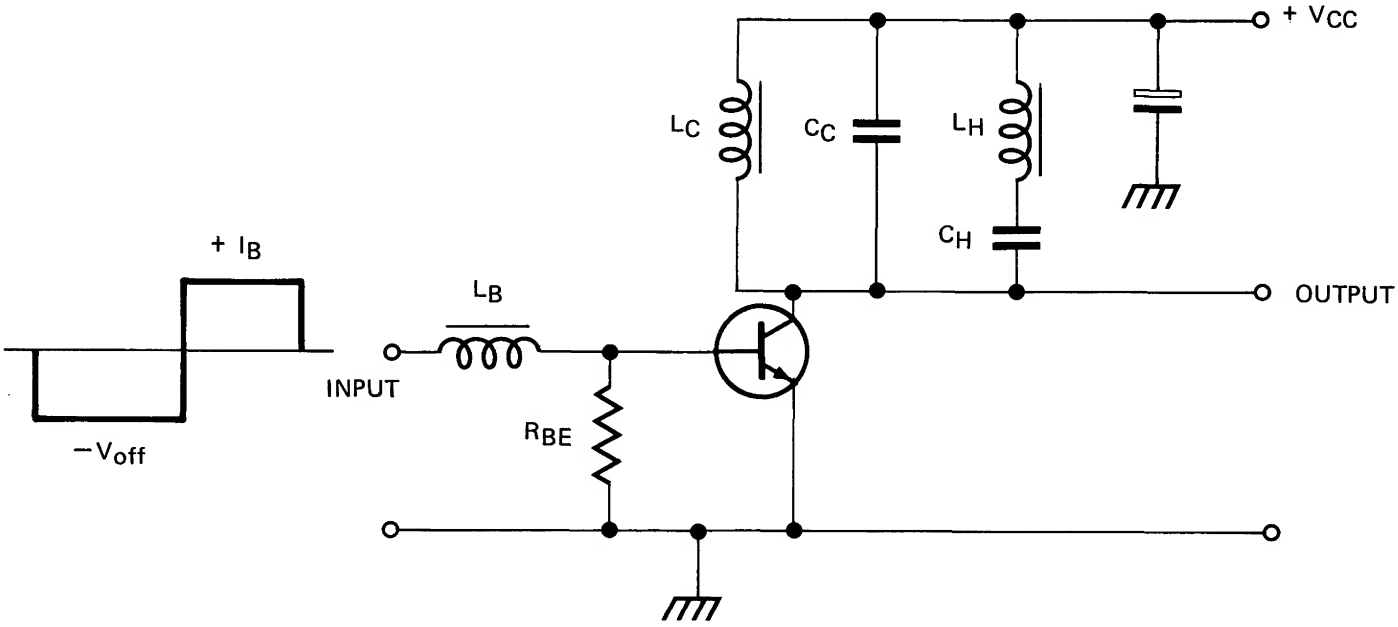


FIGURE 19. Switching Circuit used for Analysis of Waveforms

more rapid removal of excess charge. This, in fact accounts for the significantly shorter fall time as compared to the storage time. However the shape and time period of the collector current fall are influenced by several factors.

If I_B is reduced rapidly by a large value of dI_B/dt the storage time will be short but some charge may remain in the collector. This causes a slow reduction in current, the last part of which is known as 'tailing' and produces a high dissipation in the transistor. During characterisation it may be necessary to measure t_f from 90% to zero as the last 10% of the fall time could be large. With the correct value of dI_B/dt the transistor fall time will be short and the device will then provide effective switching and minimum dissipation.

Conversely, a low value of dI_B/dt extends the storage time but reduces conductivity modulation so that V_{CE} rises more rapidly which also causes high dissipation.

Other distortions are apparent in the collector current waveforms. These are due to the complex movement of charge levels in the collector region whilst the depletion layer widens during switch 'off'. The correct choice of dI_B/dt will help to reduce these distortions to give an acceptable value of t_f and hence dissipation. The waveforms associated with t_{s2} in Figure 20 give minimum dissipation although some distortion is present.

REFERENCES

1. Mick Maytum, "Monochrome TV Circuit Design using BUY71 2.2-kV Transistor," Texas Instruments Application Report No. B126.

2. J. J. Sparkes *Junction Transistors,* Pergamon Press.

III PROGRAMMABLE UNIJUNCTION TRANSISTORS

based on a report
by Glen Coers

In the first volume, the theory, operation and circuits of the conventional unijunction transistor, u.j.t., were described.[1] Its more modern counterpart the programmable unijunction transistor, p.u.t., is also a three terminal device which exhibits a negative resistance region under certain operating conditions, and has for its most numerous applications relaxation oscillators, trigger and timing circuits. In some ways, however, the p.u.t. is more analogous to a silicon controlled rectifier, s.c.r., being formed with four layers of alternate conductivity type semiconductor material, and having its three terminals designated anode, grid and cathode, as shown in Figure 1. (In practice the s.c.r. has become known as the thyristor, but if a literal translation is used for definition, then the p.u.t. is, of course, also a thyristor.) It differs from the s.c.r. in that it is the n layer next to the anode which is brought out as the gate, rather than the p layer next to the cathode as in the s.c.r. Figure 2 is a photograph of a p.u.t. wafer.

The starting material is n-type and this forms the gate, the external connection being made later to the back of the wafer. Forming a lateral pnp device two p-type diffusions are then made, the central circle becomes the anode and the square with a hole in its centre the externally unconnected p layer. A final n diffusion in the form of a makes the cathode. (An aluminium contact circle to the outer p-type region allows the device to be probe tested using its thyristor characteristics). The construction gives the p.u.t. a number of advantages when compared with the conventional uj.t. The major parameters of the p.u.t. are programmable; i.e. the anode (or peak) voltage at which the device triggers Vp, cf. η(eta) the intrinsic stand-off ratio of a uj.t.; the peak point current Ip; and the valley current I_V. It also has low leakage, high sensitivity, a high breakdown voltage, will operate from a low voltage, and provides fast high energy trigger pulses.

DEVICE CHARACTERISTICS

As stated the p.u.t. has a pnpn structure and thus three junctions, J1, J2 and J3 (Figure 1). To understand the operation of the p.u.t. more clearly, Figure 3 gives a two transistor analogy which allows the device to be analyzed in terms of the parameters of two transistors. The junction J1 acts as the emitter-base junction for the npn transistor. J3 acts as the emitter-base junction for the pnp transistor. J2 services as collector-base junction for both devices. The npn

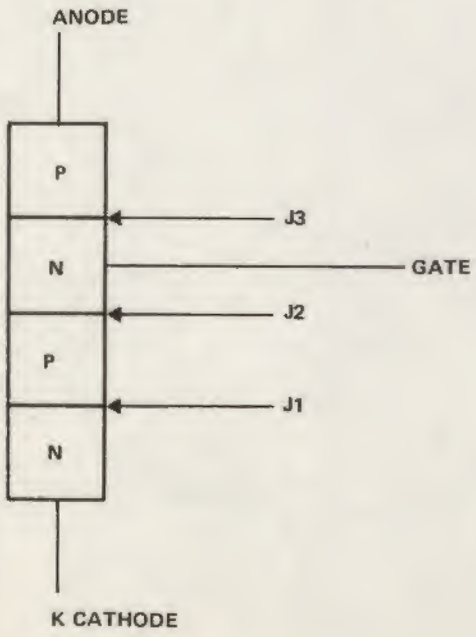


FIGURE 1. Structure of a Programmable Unijunction Transistor

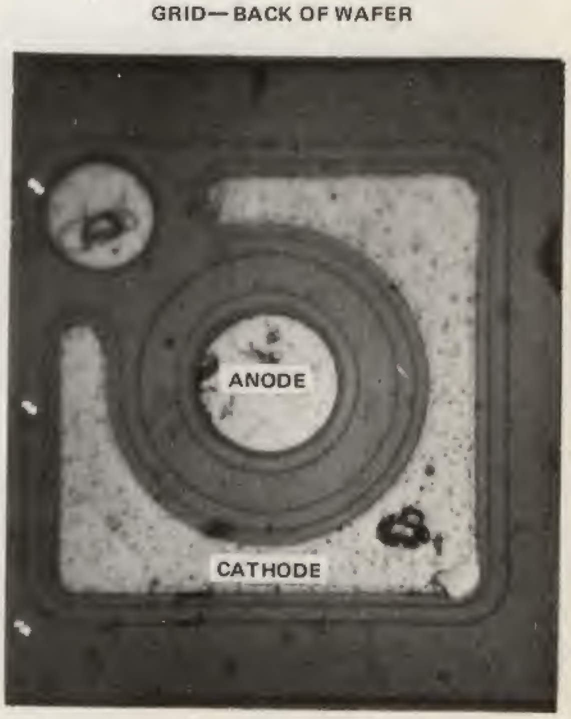


FIGURE 2. P.U.T. Construction

transistor has a current gain $h_{FE(npn)}$. The pnp section has a current gain $h_{FE(pnp)}$. These current gains will increase with increasing current flow in their respective equivalent transistors. Figure 4 illustrates the V-I characteristic developed at the anode by this arrangement.

When the anode voltage is less than the gate supply voltage V_S only a small leakage current, I_{GA}, flows from gate to anode, cf, the reversed biased emitter-base junction of the pnp transistor. (Since the current through the gate resistance, R_G, or its equivalent, is only on the order of nA, at this point, the voltage on the gate, V_G, is approximately equal to V_S).

As the anode voltage is raised above the gate voltage, gate current will begin to flow from the anode to the gate. This is emitter current for the pnp transistor which will cause pnp collector current to flow ($h_{FB(pnp)} \cdot I_A$). The npn base current times $h_{FE(npn)}$ is collector current for the npn and is also base current for the pnp. This re-enforces the initial gate current. At low currents, the npn and pnp current gains are low. However, as the currents increase, the gain of both transistors increases and regenerative action results. When this occurs, a negative resistance is developed between the anode and cathode and the device goes into a high conduction state. The anode voltage just preceding this point is the peak point, V_P. The difference between this voltage and the gate supply voltage

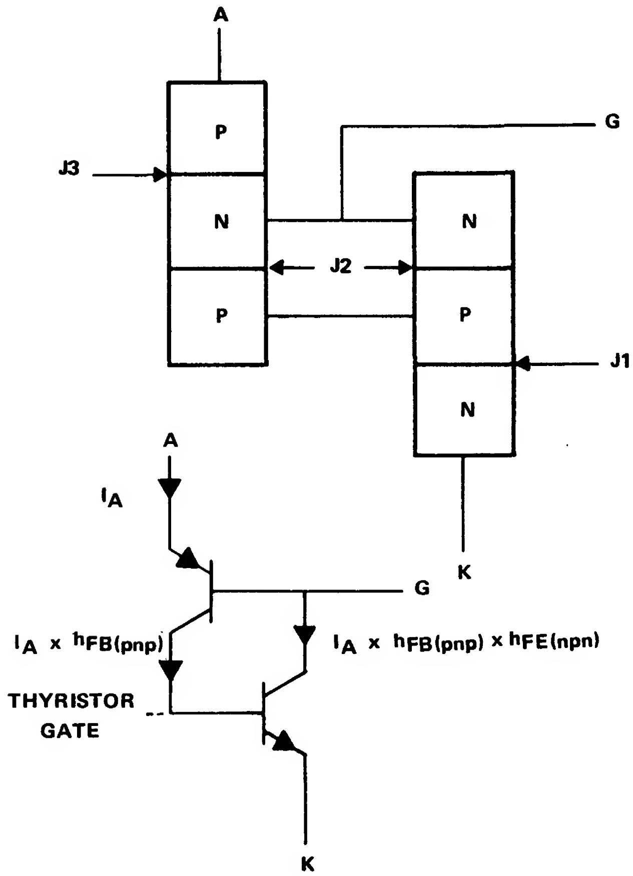


FIGURE 3. Two Transistor Anology to P.U.T.

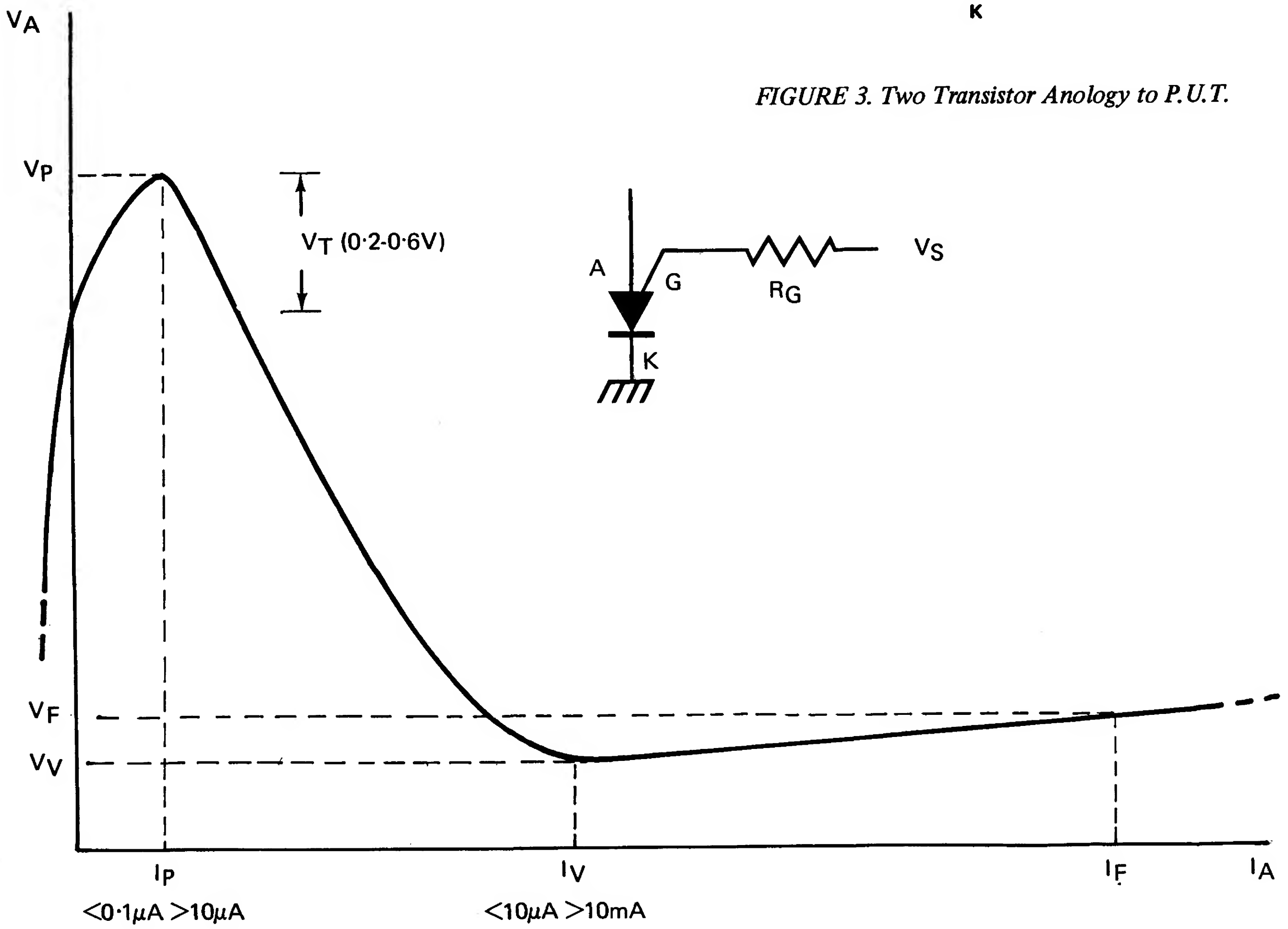


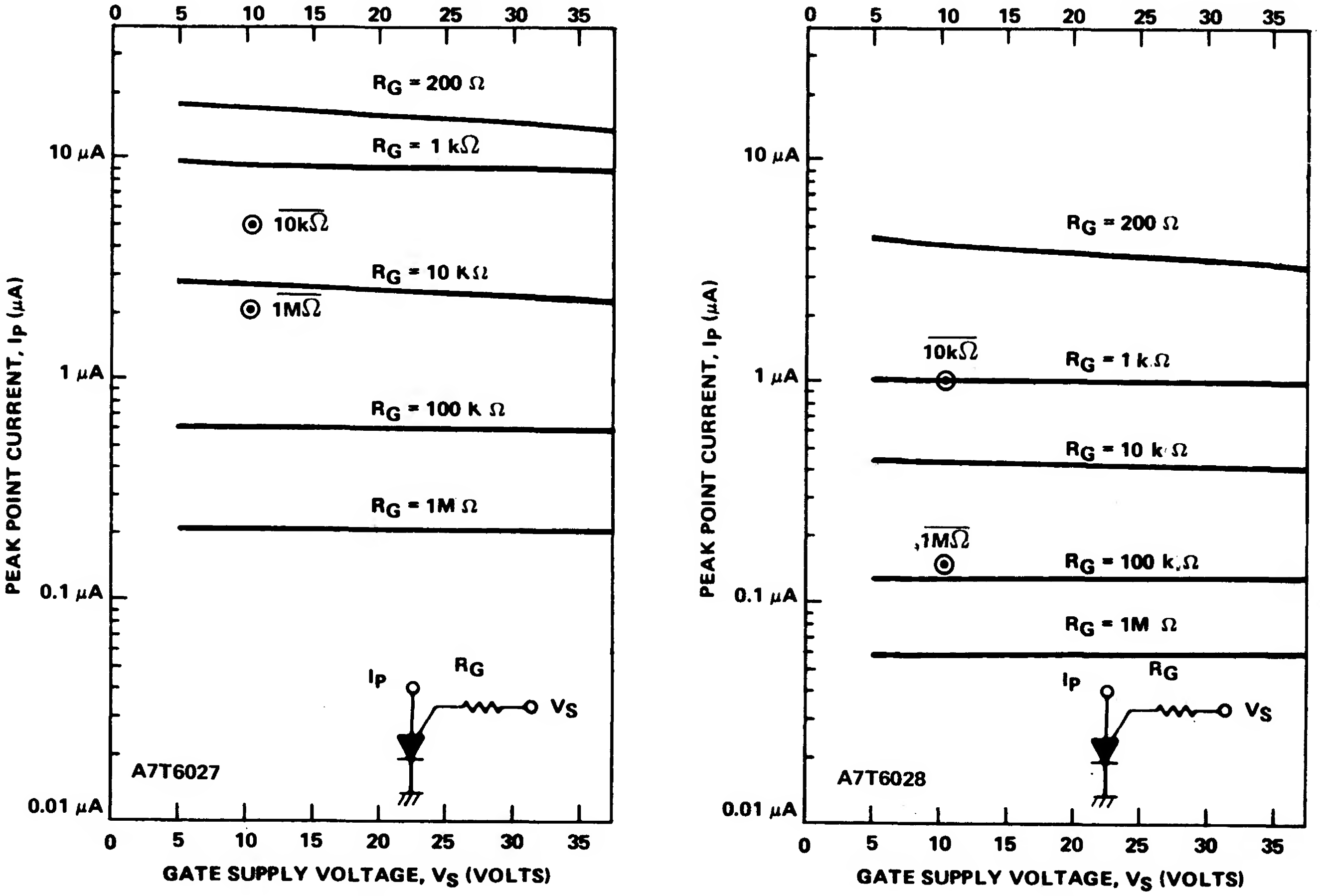
FIGURE 4. Anode Characteristic of a P.U.T.

V_S is known as the offset voltage V_T, (cf. $V_{BE(knee)}$ of the pnp transistor). Thus, by externally setting the gate supply voltage, V_S, the point at which the p.u.t. goes into the regenerative region is 'programmed', cf. η in a u.j.t. The current at which the regenerative action takes place is called the peak(point) current I_P and has a minimum value for regeneration which is strongly dependent on the gate resistance R_G, as shown for typical devices in Figure 5 (a) for an A7T6027 and (b) for an A7T6028. If this value is not supplied from the anode circuit, then the device cannot go into the regenerative region, and it is therefore by adjusting R_G that I_P is 'programmed', the higher the value of R_G the lower the I_P. In the u.j.t. the negative resistance characteristic results from the emitter-base 1 resistance being modulated to a lower value once the device's pn junction becomes forward biassed. In the p.u.t. the negative resistance is developed, not by conductivity modulation, but by the regeneration inherent in a pnpn device. Throughout the negative resistance area the anode voltage, of course, continues to fall as the anode current increases until a point where $dV_A/dI_A = 0$ and then further increase in anode current occurs an increase in anode voltage.

This point defines the valley current I_V and the valley voltage, V_V. The valley current is also strongly dependent on gate resistance R_G, as shown in the characteristics for typical devices in Figure 6, (a) for an A7T6027 and (b) for an A7T6028. Thus by adjusting R_G, I_V can be 'programmed' – I_V being inversely proportional to I_G.

With anode currents greater than I_V the device is in saturation, the pnp-npn transistors having sufficient current to sustain the regenative conditions. If the load line of an oscillator circuit intersects the curve in this area, the circuit will not oscillate, the device remaining in saturation. (Reducing the anode current, a point is reached where the current in the pnp-npn loop is just sufficient to maintain conduction, i.e. the holding current level.) A measure of the voltage forward drop, V_F, across the device at a particular anode current in this region, I_F, is given in the data sheets.

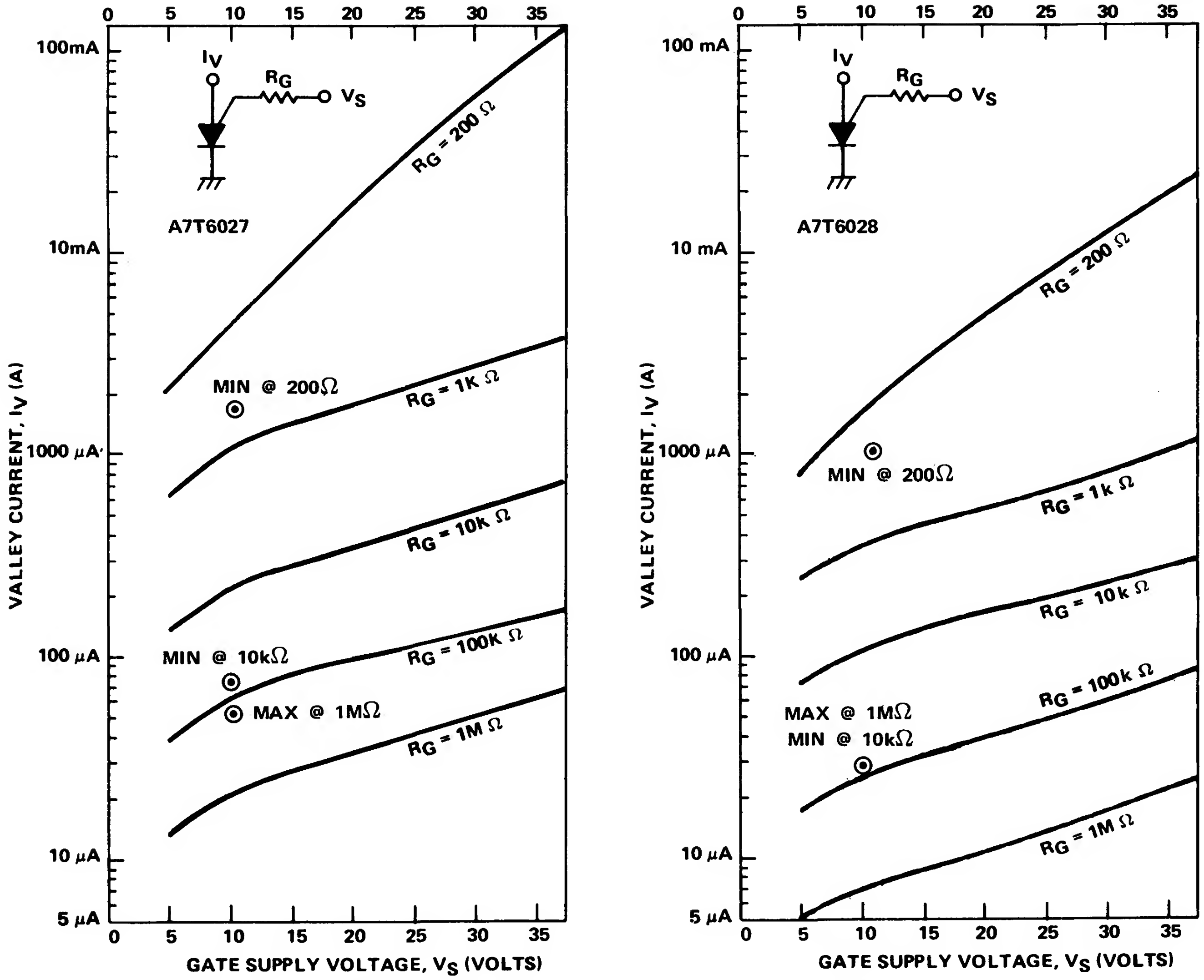
The dynamic resistance of a p.u.t. in 'on' condition is approximately 3Ω, and therefore the peak pulse output voltage (see Figure 7) across a cathode resistor V_O, is high compared to the u.j.t. The value of V_O (for an A7T6027/8) is shown in Figure 8 against gate supply voltage V_S, for various values of anode circuit timing capacitance.



(a)

(b)

FIGURE 5a and 5b. Relationship of Peak-Point Current, I_P, and Gate Resistance R_G



(a) *FIGURE 6a and 6b. Valley Current, I_V, verses Gate Resistance, R_G* (b)

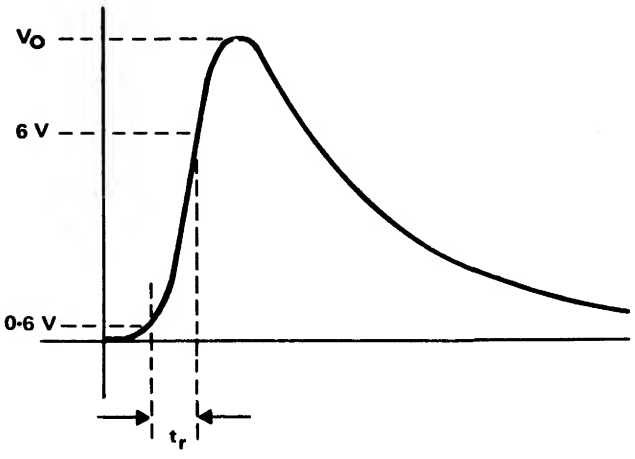


FIGURE 7. Definition of V_O and t_r

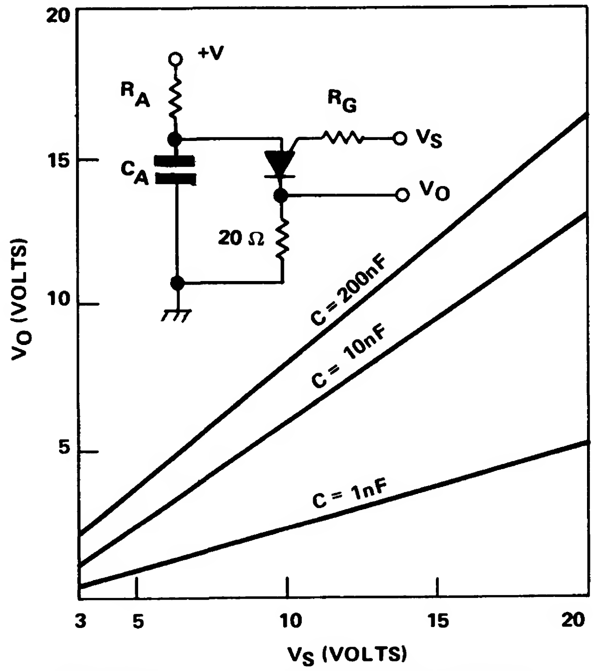


FIGURE 8. Pulse Output Voltage for Various Capacitor Values

The forward conductance of the p.u.t. is high and the risetime t_r, is fast, i.e. typically 65ns from 0.6V to 6V (see Figure 7), with a data sheet maximum for the A7T6027/8 of 80ns.

DEFINITION OF PARAMETERS

I_A	Anode Current – Current flowing into anode over the complete device characteristic (Figure 4).
I_F	Forward Current – Current flowing from anode to cathode in saturation defining the forward voltage V_F (Figure 4).
I_{GAO}	Anode to Gate Leakage – Anode to gate leakage current with the cathode open (Figure 9 (a)).
I_{GKS}	Gate to Cathode Leakage – Gate to cathode leakage with the cathode and anode shorted together (Figure 9 (b)).

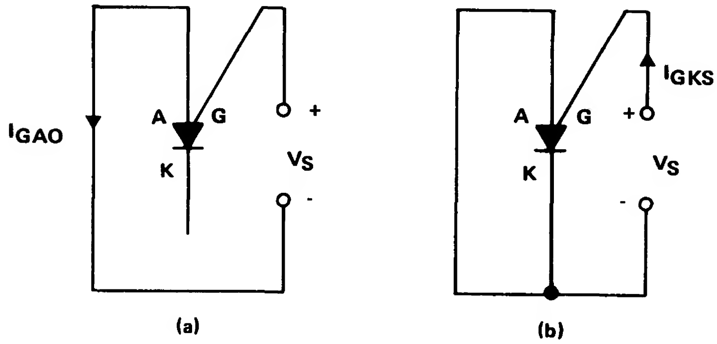


FIGURE 9. Test Circuits for I_{GAO} and I_{GKS}

I_P	Peak-Point Current – The minimum current required to cause the p.u.t. to go into conduction (Figure 4).
I_V	Valley-Point Current – The region where the transition is made from the negative resistance region to the positive resistance region, i.e. $dV_A/dI_A = 0$.
R_G	Gate Resistance – The equivalent source resistance of the gate supply voltage V_S.
t_r	Rise Time – The time required for the output voltage taken across a resistor in series with the cathode, to go from one specified value to another while operating under specified conditions (Figure 7).
V_A	Anode Voltage – Voltage on the anode over the complete device characteristic.
V_F	Forward Voltage – Voltage between the anode and cathode at a specified current, I_F (Figure 4).
V_G	Gate Voltage – Voltage on the gate of the p.u.t.
V_O	Pulse Output Voltage – The peak voltage measured across a resistor in series with the cathode when the p.u.t. is operating as a relaxation oscillator under specified conditions. (Figure 7).
V_P	Peak Voltage – The minimum voltage required on the anode in order that the device should go into conduction.
V_S	Gate Supply Voltage – The voltage applied to the gate when the gate current is zero, i.e. the 'unloaded' value of gate voltage. It is this voltage which is 'set' in order to determine the trigger point of the device, cf. η (eta) of a u.j.t.
V_T	Offset Voltage – The difference in voltage between V_S and anode voltage V_P when the device triggers i.e. $V_T = V_P - V_S$. (Figure 4).

APPLICATIONS

Relaxation Oscillator/Pulse Generator

Operation: The conventional u.j.t. relaxation oscillator circuit is shown in Figure 10 and the equivalent p.u.t. circuit in Figure 11. Although the actual values of passive components are varied to suit the characteristics of the active components used, as can be seen, the difference in the two circuits is the addition of a resistor, R1, to form a potential divider for the p.u.t. The operation of the

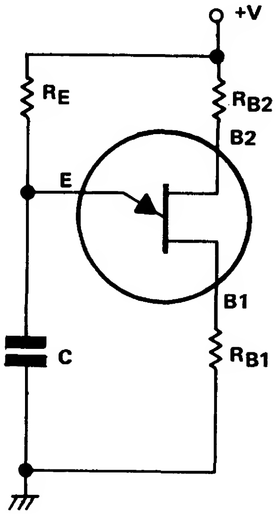


FIGURE 10. Conventional U.J.T. Relaxation Oscillator

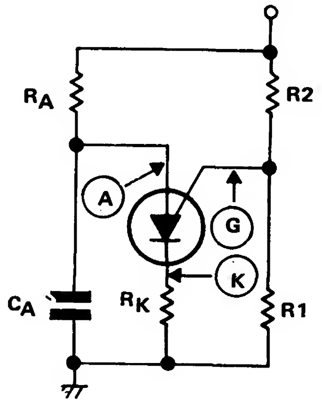


FIGURE 11. P.U.T. Relaxation Oscillator

circuit is also similar. Consider the p.u.t. circuit whose idealised operating waveforms are shown in Figure 12. When power is supplied from the voltage rail + V, capacitor C_A charges exponentially through resistor R_A, with a time constant $C_A.R_A$, until the voltage on the anode A equals the anode firing voltage V_P. At this voltage the anode gate junction becomes forward biased and the anode goes into the negative resistance region. Capacitor C_A discharges through the anode, dynamic resistance and cathode resistor R_K thus giving a positive pulse at the cathode K. As it falls in sympathy with the anode, a negative pulse is available at the gate. The capacitor discharges until the voltage across it is equal to the valley voltage V_V, plus the drop across resistor R_K ($I_V R_K = V_{R_K}$ say), and then the p.u.t. turns off. The capacitor starts to charge up again and the cycle repeats.

Calculations: The starting point and the order in which the values of the components are to be determined depends on the application and fixed values which go with it. As component values are inter-related some iterative method must generally be used. A typical approach would be:

Using the available, or desired, rail voltage, V, the ratio of potential divider resistors values R1 and R2 for a chosen gate supply voltage V_S is given from

$$V_S = V.R1/(R1 + R2) = \eta.V, \text{ say} \quad . \; . \; . \; . \; . \quad (1)$$

A value of equivalent gate resistance R_G is chosen by studying Figure 5 and knowing the purpose of the circuit. For example, if a long period timer is required the timing components R_A and C_A need to be as large as possible, therefore I_P needs to be small and thus R_G as large as possible; or conversely, if a high frequency circuit is required R_A and C_A need to be small, I_P large and thus R_G small. From equation (1) and

$$R_G = R1.R2/(R1 + R2) \quad . \; . \; . \; . \; . \; . \; . \; . \quad (2)$$

the values of resistors R1 and R2 may be calculated.

The time for a complete period of oscillation is given by the sum of the device 'off' and 'on' time,

i.e. $t_{off} + t_{on}$ (= 1/f) where f is the frequency of oscillation.

As the capacitor C_A charges exponentially from the valley voltage V_V to the peak voltage V_P, with a time constant $C_A.R_A$ towards a target voltage V

$$t_{off} = C_A.R_A.\ln\left[(V - V_V)/(V - V_P)\right] \quad . \; . \; . \quad (3)$$

As $\quad V_P = V_T + V_S = V_T + \eta.V$

$$t_{off} = C_A.R_A.\ln\left[(V - V_V)/(V - V_T - \eta.V)\right]$$
$$= C_A.R_A.\ln\left[(V - V_V)/(V(1 - \eta) - V_T)\right] . \quad (4)$$

If $\quad V \gg V_V$ and V_T

$$t_{off} \triangleq C_A.R_A.\ln\left[1/(1 - \eta)\right]$$

or

$$\triangleq C_A.R_A.\ln\left[(R1 + R2)/R2\right] \quad . \; . \; . \; . \; . \; . \quad (5)$$

If the negative pulse at the grid G is suitable for driving the following circuits then for most of the frequency range resistor R_K is not required. However, if the frequency is low and the value of capacitor C_A therefore large, care must be taken not to exceed the capacitive discharge energy rating, e.g. 250 pJ for A7T6027/8 p.u.t.s. Inclusion of resistor R_K can therefore become necessary in order to dissipate some of the energy. In general, of course, this resistor is included in order to provide a convenient point to obtain a positive pulse for driving subsequent circuits–especially thyristors, (although it does make the calculations for the 'on' time considerably more complex).

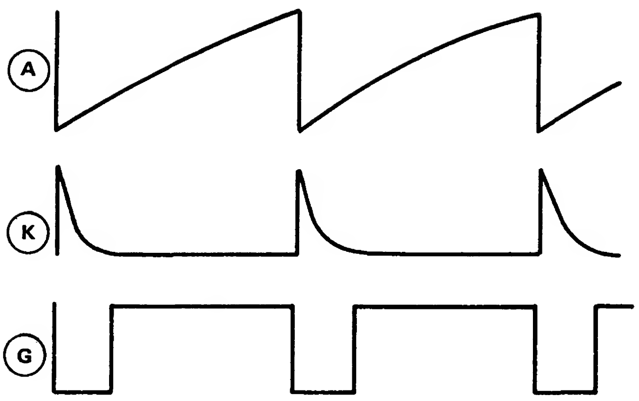


FIGURE 12. Idealized P.U.T. Relation Oscillator Waveforms

$$t_{on} = C_A.(r_{dy} + R_K).\ \ln\left[V_P/(V_V + V_{R_K})\right]$$

or

$$= C_A.(r_{dy} + R_K).\ \ln\left[(V_T + \eta.V)/(V_V + V_{R_K})\right] \quad (6)$$

If $t_{on} \ll t_{off}$ (Applicable to all but high frequency oscillation).

$$1/f \triangleq t_{off} \triangleq C_A.R_A.\ \ln(R1 + R2)/(R2) \quad . \; . \; . \quad (7)$$

(N.B. If R1 = R2 $\quad t_{off} \triangleq 0{\cdot}7C_A.R_A$)

An idealised p.u.t. anode characteristics curve with superimposed load lines and paths to illustrate the operation of the circuit is shown in Figure 13.

If the value of resistor R_A is large enough so that its load line LL1 intercepts the characteristic curve in the cut off region, then the peak point will not be reached and the p.u.t. can not trigger. Thus there is a maximum value represented by load line LL2, below which resistor R_A must be kept, i.e.

$$R_A < (V - V_P)/I_P$$

i.e.

$$R_A < (V(1 - \eta) - V_T)/I_P \quad . \; . \; . \; . \; . \; . \; . \quad (8)$$

where $\eta = R1/(R1 + R2)$

For the worst case value maximum values of V_T and I_P should be used.

(If $V_T \ll V \quad$ then $\quad R_A < V(1 - \eta)/I_P$)

When the device triggers the point of operation moves theoretically instantaneously from the peak point P1 to a point P2, at the same voltage, on the conducting part of the characteristic, as the voltage across the capacitor cannot change instantaneously. (In practice a time interval exists which allows the capacitor to partially discharge and the point P2 is lower down the characteristic). Capacitor C_A discharges down the characteristic towards the valley point. If the load line, e.g. LL3, is such that it cuts the characteristic in the saturation region, ($I_A > I_V$), then a stable state results and the p.u.t. will stay 'on' and no further action will occur. Thus there is a minimum value of resistor R_A represented by load line LL4, i.e.

$$R_A > (V - \left[V_V + V_{R_K}\right])/I_V \quad . \; . \; . \; . \; . \; . \; (9)$$

where for a worst case value V_V, V_{R_K} and I_V should be minimum. Under actual operating conditions, the variation in valley voltage with respect to valley current in the area of valley point is so small that in order to assure turn off, resistor R_A should be made two or three times larger than the minimum value, i.e.

$$R_A > 3.\,(V - V_V - V_{R_K})/I_V \quad . \; . \; . \; . \; . \; . \; (10)$$

If the value of R_A is selected correctly for oscillation then the load line will intersect the negative resistance region, as LL5. Then, once the operating point passes the valley point, it needs a higher voltage to support the current. As this is not available, the p.u.t. goes 'off' and point of operation moves to P3, ideally the same voltage $V_V + V_{R_K}$ on the 'off' section of the characteristic, and cycle repeats.

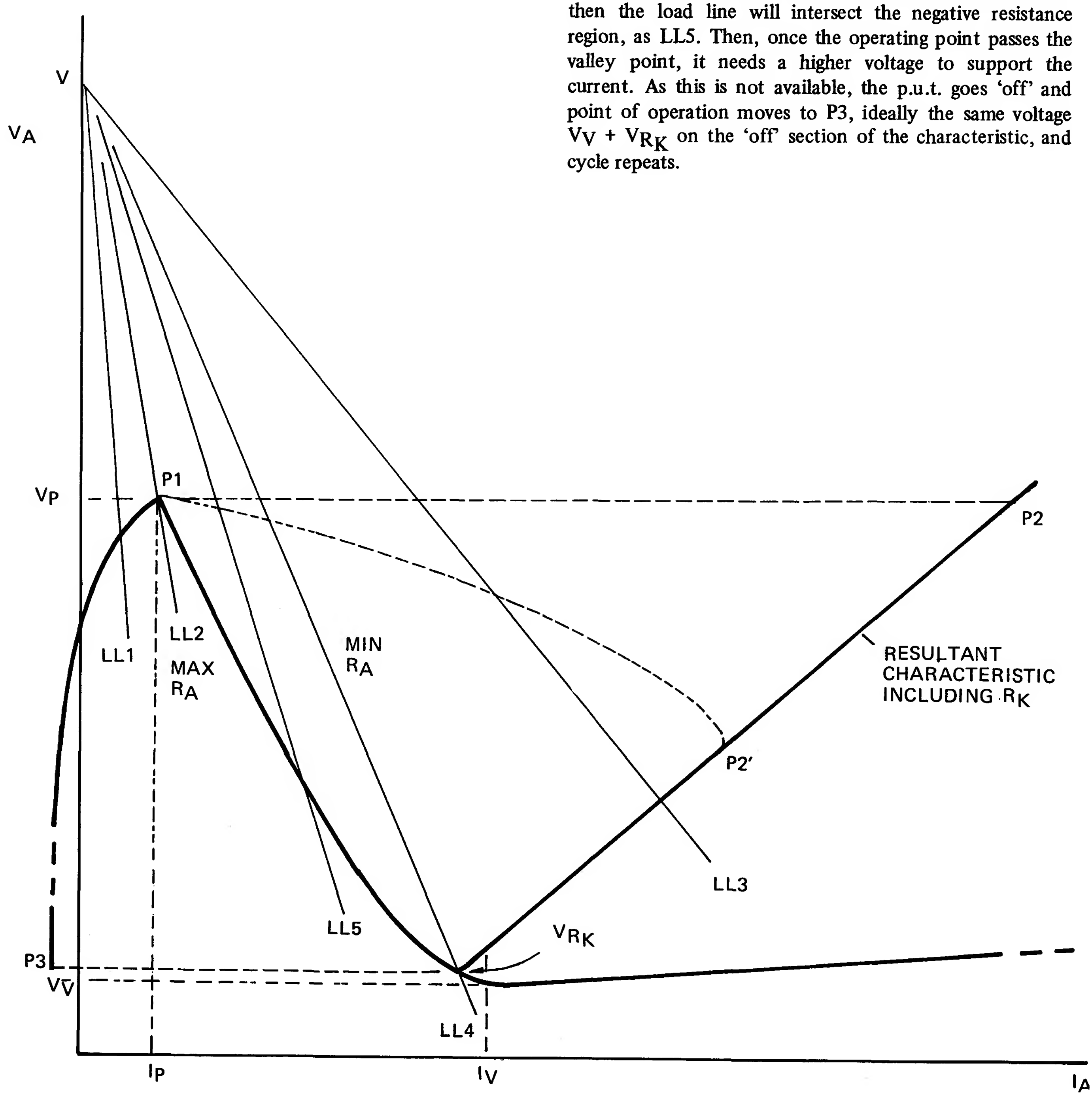


FIGURE 13. P.U.T. Oscillator Characteristics

Practical example: A typical pulse generator would run from a 10V rail at 1·5kHz, say.

Let $V_S = 5V \quad \eta = 0{\cdot}5$ then

$0{\cdot}5 = R1/(R1 + R2)$ from equation (1)

i.e. $R1 = R2$

Let $R_G = 10k\Omega$ then

$10 \times 10^3 = R1.R2/(R1 + R2)$ from equation (2)

i.e. $R1 = R2 = 20k\Omega$

At 1·5kHz t_{on} is negligible and $\therefore$ from equation (7) as $R1 = R2$

$t_{off} \mathrel{\hat{=}} 0{\cdot}67 \times 10^{-3}/0{\cdot}7 \times 10^{-8}$

Make $C_A = 10nF$, i.e. $10^{-8}F$

Therefore, $R_A \mathrel{\hat{=}} 0.67 \times 10^{-3}/0.7 \times 10^{-8}$

$\mathrel{\hat{=}} 100k\Omega$

From the data sheet values the maximum values for an A7T6027 p.u.t. of I_P and V_T at $R_G = 10k\Omega$ are $5\mu A$ and 0·6V respectively. Therefore from equation (8)

$R_A < \left[10(1 - 0{\cdot}5) - 0{\cdot}6\right] / 5 \times 10^{-6}$

$< 900k\Omega$

From the data sheet values on Figure 6(a) the minimum value of I_V at $R_G = 10k\Omega$ is $70\mu A$. Assuming the minimum value of $V_V + V_{RK} = 0$ from equation 10.

$R_A > 3 \times 10/70 \times 10^{-6}$

$> 430k\Omega$ i.e. too high.

If the value of R_A set by the frequency was increased the value of the capacitor C_A would need to be decreased to maintain the same frequency. This would lower the pulse energy so, as an alternative, the value of R_G must be reduced.

Let $R_G = 1k\Omega$ then $R1 = R2 = 2k\Omega$ ($2{\cdot}2k\Omega$ say)

Interpolating from Figure 5(a) the maximum $I_P = 15\mu A$.

$\therefore R_A < 300k\Omega$

and from Figure 6(a) the minimum $I_V = 400\mu A$.

$\therefore R_A > 75k\Omega$ i.e. safe for correct operation.

Figure 14 shows the p.u.t. pulse generator circuit with the component values as calculated. The oscilloscope waveforms as shown in Figure 15 show, on the left hand side, an expanded view of the pulse section of the waveform at points K, G and A, and, on the right hand side, the complete cycle waveforms. With these component values the circuit will operate from below 2V to 40V, although if one of these two extreme values was to be the desired supply voltage then optimization of the component values would be required, e.g. a lower value of R_A for 2V and higher value for 40V. Also it should be noted that at low voltage the value of the V_T becomes significant and the capacitor has effectively to charge up to a higher point on the exponential curve, thus increasing the period and lowering the frequency.

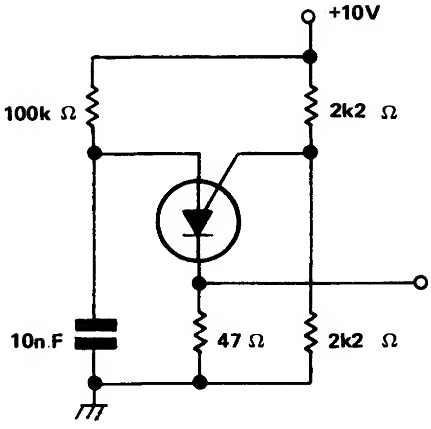


FIGURE 14. Basic Relaxation Oscillator Circuit Using P.U.T.

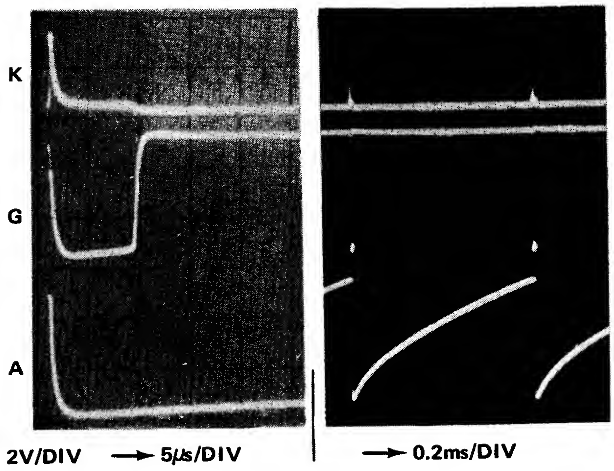


FIGURE 15. Oscillator Waveforms

Low Ip, High I_V Oscillator

If a long time period is required, i.e. a low Ip is needed, and yet a high current (I_V) capability is necessary, then the basic oscillator circuit may be modified as shown in Figure 16. Here when the device is 'off', the effective value of R_G is 1MΩ and therefore meets the requirement for low Ip. When the device turns 'on', the gate approaches ground. This forward biasses the diode D1. The diode impedance is now very low and as the effective value of R_G is the parallel combination of resistors R1 and R2. As these are low in value the requirement for high valley current is met.

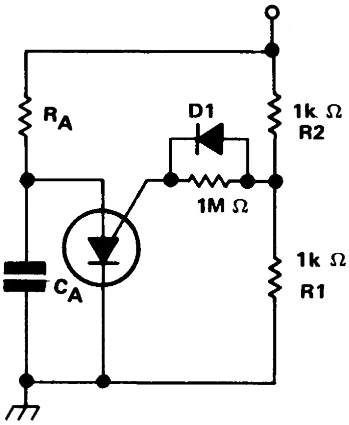


FIGURE 16. Low Ip, High I_V Oscillator

Temperature Compensated Oscillator

The addition of diode D1, and a resistor to ensure that the diode is always conducting, to the basic oscillator circuits, as shown in Figure 17, allows the p.u.t. circuit to be temperature compensated. In the basic circuit if the temperature rises, say, the threshold voltage V_T will decrease and, as the gate voltage stays constant, Vp will also decrease and the period is reduced. However, with diode D1 in circuit the forward voltage drop across it will also decrease by an amount similar to the V_T and, as its anode is held at a fixed voltage, the gate voltage will rise compensating for the drop in V_T, so that Vp remains at a constant level. (Temperature compensation is difficult with the conventional u.j.t. circuit as, although compensation can be made for the emitter 'diode', usually by adjusting resistor R_{B2}, other parameters which can affect the timing change with temperature).

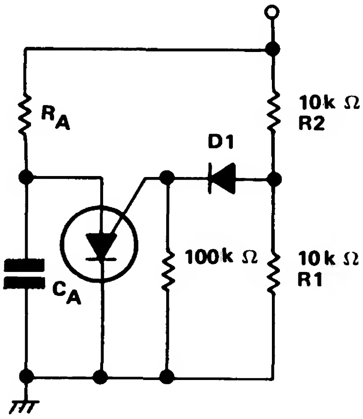


FIGURE 17. Temperature Compensated Oscillator

Astable Multivibrator

As with the conventional uj.t. circuit, the p.u.t. pulse generator circuit can be modified to define the 'on' time by the addition of a diode or transistor, whose base-emitter junction is acting as the diode, as shown in Figure 18. The advantage of using a transistor is that a well defined pulse is available on its collector which can be chosen to fit exactly with the subsequent circuit requirements, for example, t.t.l. devices. The circuit is now an astable multivibrator with one device 'on' while the other is 'off'. As only one capacitor, C_A, is used for the timing a saving is made, especially when a slow frequency and thus a large electrolytic capacitor is required. Without the cathode resistor R_K the valley point for the generator is a true V_V and I_V, and therefore the safety factor for the calculation of minimum R_A need not be as large. The combination of the load lines for charging resistors R_A and R_B should be such as to place the operation point in the saturation region of the p.u.t. characteristics. If resistor R_B is to be large, to provide a long output pulse, say, then additional components, diode D1 in series with resistor R3, should be added to supply the required latching current, as shown in

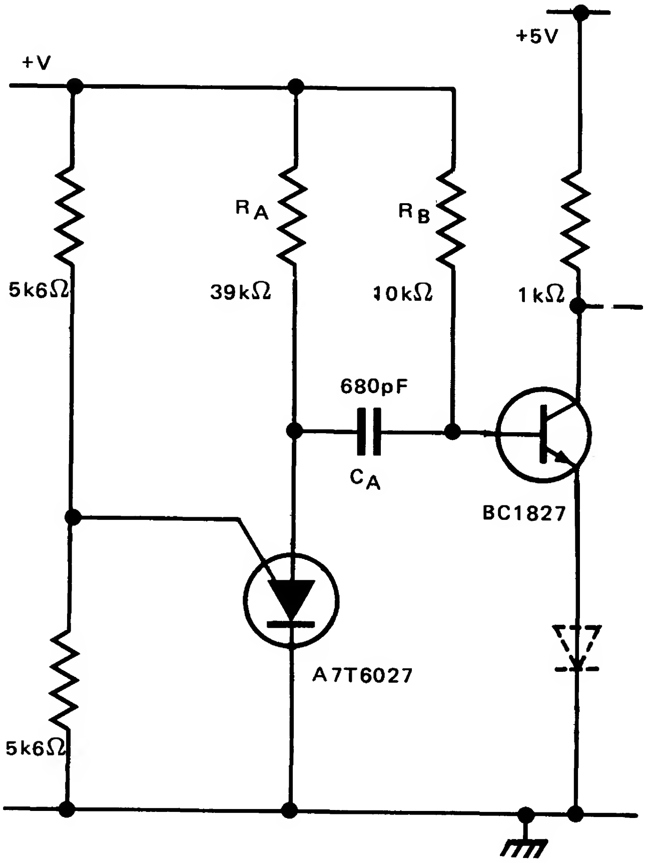


FIGURE 18 Astable Multivibrator

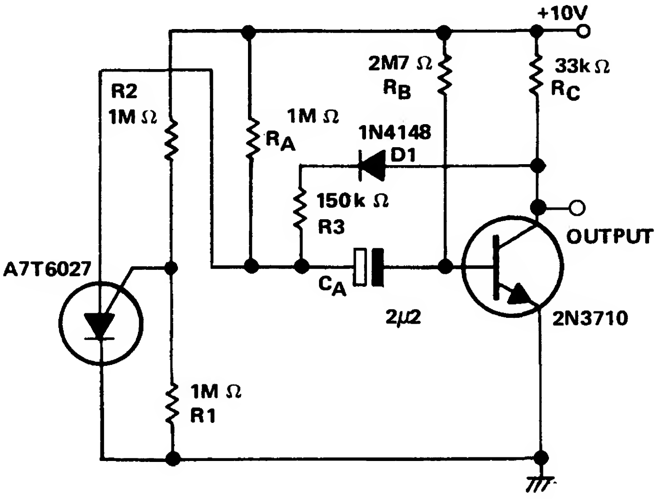


FIGURE 19. Long Period One-Capacitor Multivibrator

Figure 19. When the p.u.t. triggers in this circuit a voltage set $V_P - V_V$, is taken across the capacitor and, taking its base negative, switches the transistor 'off'. (Care must be taken to ensure that the reverse emitter-base voltage, V_{EB}, of the transistor is not exceeded as the timing would then be affected and damage to the junction could occur. If the rating is to be exceeded then a diode–cathode to base or anode to emitter, cathode to earth–should be employed.) The capacitor then charges up towards the supply voltage V with a time constant $C_A.R_B$. When the voltage on the base of the transistor reaches $V_{BE(knee)}$, it switches 'on' again, taking the current through R_B and leaving only the current through R_A for the p.u.t.–which therefore switches 'off'. The cycle then repeats. The 'on' time of the p.u.t. is therefore given by:

$$t_{on} = C_A.R_B.\ \ln\left[(V_P - V_V + V - V_{BE})/(V - V_{BE})\right]$$

$$= C_A.R_B.\ \ln\left[1 + (V_P - V_V)/(V + V_{BE})\right]$$

$$= C_A.R_B.\ \ln\left[1 + (\eta.V + V_T - V_V)/(V + V_{BE})\right] \quad . (10)$$

(If $V \gg V_T$, V_V and V_{BE}

$t_{on} \triangleq C_A.R_B.\ \ln(1 + \eta)$

and when R1 = R2 $t_{on} \triangleq 0.4 \times C_A \times R_B$)

(N.B. Due to the effect of storage time in both active devices the period will be slightly lengthened over the calculated values).

With the component values as shown in Figure 18, the operation is at 40kHz with a pulse period of 3–4µs. By using the component values as shown in Figure 19 the frequency is 0·25Hz and the output pulse period is 2·35 s.

Timers and Delay Circuits

Another major use of p.u.t.s is in timing or delay circuits. A typical delay circuit is shown in Figure 20. When the switch S1 is closed, capacitor C_A charges up with a time constant $C_A.R_A$, until after the delay time required, the voltage across it reaches the peak voltage V_P when the p.u.t. triggers. The positive pulse at the cathode turns on the thyristor. Components diode D1 and resistor R3 provide temperature compensation as previously explained. As the leakage current of the p.u.t. is not sufficient to trigger the thyristor, the 47Ω cathode resistor is not always necessary; the p.u.t. cathode feeding directly to the gate of the thyristor.

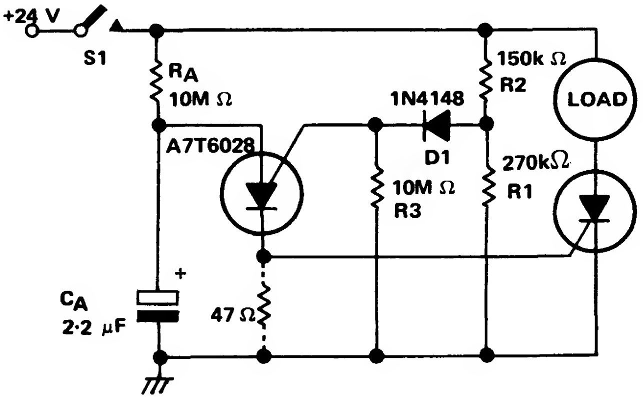


FIGURE 20. Typical P.U.T.Delay Circuit

The long delay timer shown in Figure 21 is possible because of the low leakage of the p.u.t.. With switch S1 closed, the left hand section of the circuit functions as a conventional pulse generator giving a small negative pulse at approximately 60 second intervals to point A. The 100Ω resistor in series with the large charging capacitor is to prevent over dissipation in the p.u.t. as it has no cathode resistor. The time constant of the right hand side of the circuit is considerably larger i.e. 500MΩ x 4·7µF ≏ 40 minutes. The current provided by this resistor is not

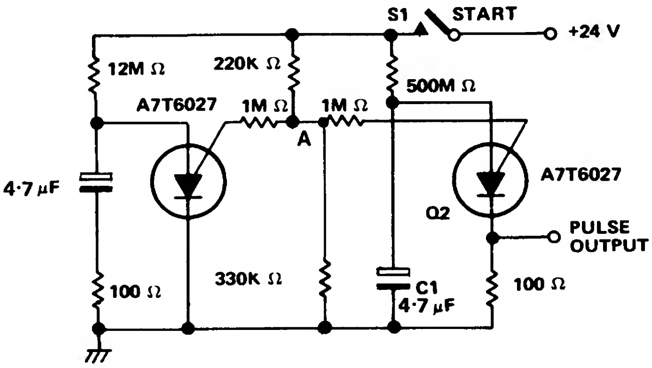


FIGURE 21. A Long Delay Timer P.U.T. Circuit

normally sufficient to allow the p.u.t. to trigger, but after the required delay period the next sharp negative excursion at point A causes the p.u.t. to trigger, current coming from the capacitor, and an output pulse is obtained across its 100 cathode resistor. (Both capacitors and the 500MΩ resistor must be of the low leakage type to maintain timing accuracy).

Monostable Multivibrator

A retriggerable monostable multivibrator (one shot) using a p.u.t. is shown in Figure 22. A positive pulse is available at the output whenever a positive input pulse occurs. The output will remain 'high' if another input pulse is received before the end of the timing cycle. Initially as the value of resistor R_A is low, the p.u.t. is held in saturation and the anode is at ≏ V_V (and the gate somewhat lower). When a positive pulse is applied at the input the transistor comes 'on' and further discharges the capacitor to its $V_{CE(sat)}$ level. This unlatches the p.u.t. and it turns 'off', the gate going positive to a level set by resistors R1 and R2. When the transistor switches 'off' the capacitor charges up exponentially towards the supply voltage and at V_P the p.u.t. fires and the gate voltage returns to its 'low' level. If at any time during the 'charge' portion of the cycle another pulse is received at the input the capacitor is discharged and the timing starts again.

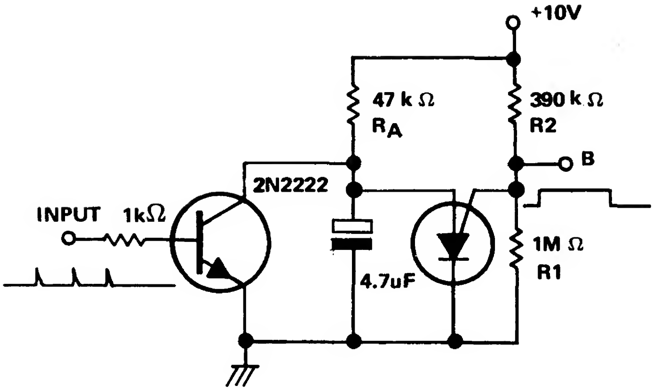


FIGURE 22. Retriggerable Monostable Multivibrator

Switch Contact Bounce Eliminator

Another circuit which is programmed so that I_V is exceeded and the p.u.t. once triggered stays in the saturated condition is shown in the switch contact bounce eliminator circit, Figure 23. When the switch is closed the capacitor charges to V_P and triggers the p.u.t. and the single output pulse on the cathode resistor operates the logic circuit. Any switch contact bounce is eliminated. If required with this circuit the charging resistor R_A could be taken to an alternative more suitable supply voltage.

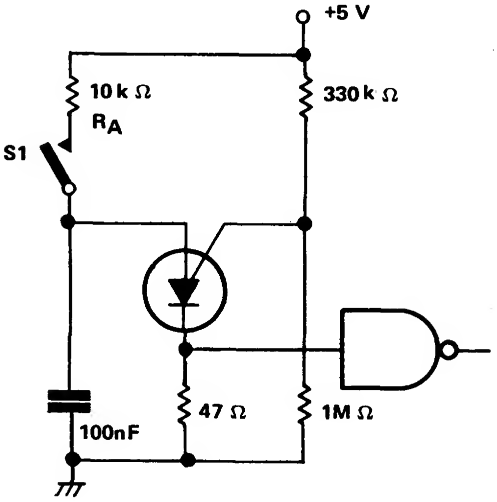


FIGURE 23. Switch Contact Bounce Eliminator Circuit

Zero Crossing Detector

In the zero crossing detector circuit shown in Figure 24, the p.u.t. is used to obtain an output pulse every 360 degrees at the zero voltage point on the a.c. waveform. Two d.c. supply voltages of approximately ±8·5V are derived from the bridge and smoothed by the 50μF capacitors. Prior to the bridge are two sinewaves, x and y, 180° out of phase with one another, one, y, fed to the base of the transistor and the other, x, to the potentiometer VR1 which controls the gate supply voltage of the p.u.t.. When the base of the transistor is taken a V_{BE} voltage below earth the transistor comes 'on' and charges up the 1μF capacitor to $-V_{CE(sat)}$. The p.u.t. remains 'off' because there is at this time a positive (half sinewave) voltage on the potentiometer VR1. However, the latter is set so that as the a.c. voltage on it passes through the zero point the p.u.t.'s gate is at value V_T below the level sitting on the 1μF capacitor and the p.u.t..triggers. A positive pulse therefore appears at the cathode as the sinewaves pass through the

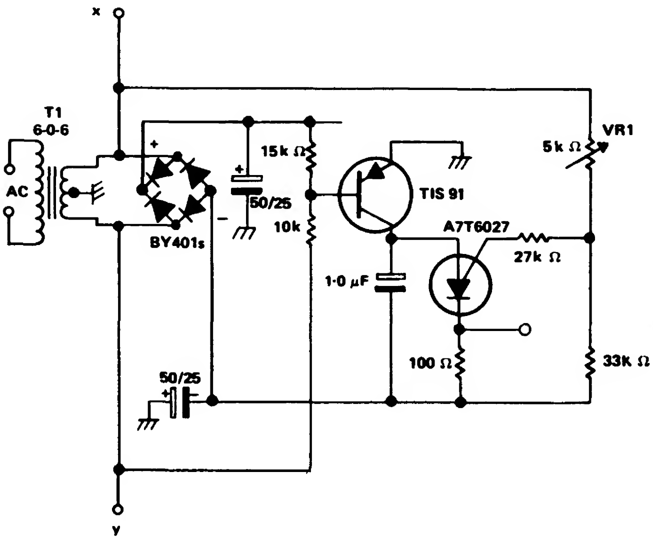


FIGURE 24. Zero Voltage Crossing Detector

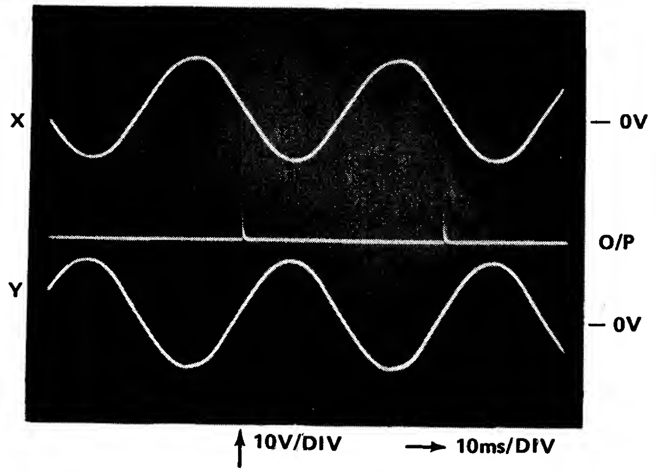


FIGURE 25. Oscillograms of the Circuit Waveforms

zero voltage point. Varying the potentiometer allows a phase adjustment of approximately ±5 degrees. (Larger variation, with more delay and thus more suitable for inductive load switching, could be obtained by increasing the value of the potentiometer). Oscillograms of the circuit waveforms are shown in Figure 25.

Voltage Controlled Oscillator

By using a constant current supply to the capacitor a voltage controlled oscillator can be made from the p.u.t. pulse generator circuit, as shown in Figure 26. With a constant current charge the voltage on the capacitor rises linearly and thus as the control voltage is changed the p.u.t. firing point and thus the frequency changes proportionally. (The control voltage terminal is a high impedance until the p.u.t. fires). The transistor is used to shape the output pulse and control its amplitude. Two methods of obtaining the constant current supply are shown, one using a field effect transistor and the other a transistor. The dynamic range of frequency change depends on the range over which the control voltage can be varied, e.g. with a supply voltage of 40V a control voltage change from 5 to 35V gives a 7:1 frequency change. Voltages lower than 5 could be used, but as the threshold voltage becomes more significant the linearity decreases.

REFERENCE

1. *Semiconductor Circuit Design,* Vol. I, Texas Instruments Limited, Chapter VI, pp. 35-36, April 1972.

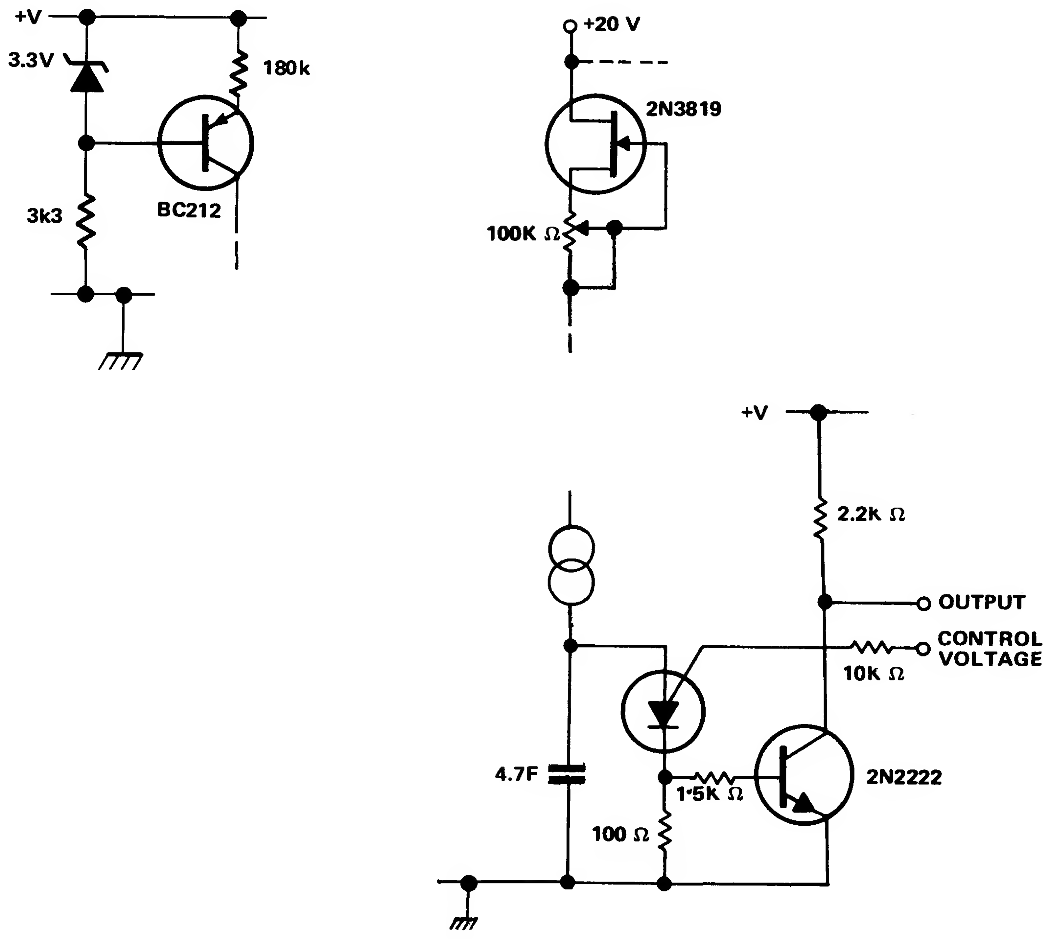


FIGURE 26. Voltage Controlled Oscillator

IV INVERTER/CONVERTER SYSTEMS

by
Bryan Norris

A number of actual practical circuits intended for a variety of particular functions are discussed in this chapter, the principles and design of inverters/converters being given in the first volume[1]. An inverter system can be considered to have two basic configurations, as shown in Figure 1; the driven and self oscillating. The driven type has a separate timing circuit which feeds into the drive unit controlling the switch turning the output power 'on' and 'off'. If the load is unknown or varying, this is the type to use but its premium is its complexity and thus cost. If the load is known and fixed, then a saving can be made by using the self-oscillating type where the timing and drive are one using positive feedback taken from the power output. In both of these configurations the output stage may employ either a single, active device–single ended–or two devices in a 'push-pull' arrangement.

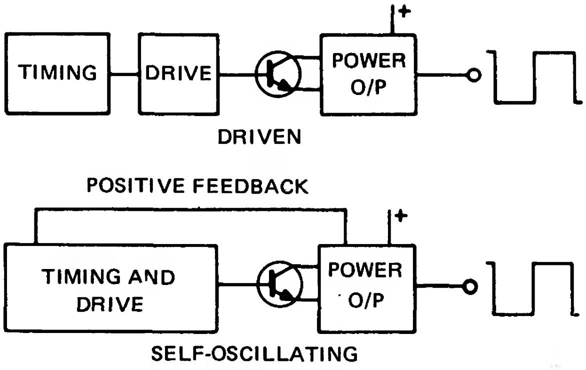


FIGURE 1. Inverter System

SINGLE ENDED SELF OSCILLATING CIRCUITS

13W Fluorescent Lamp Inverter

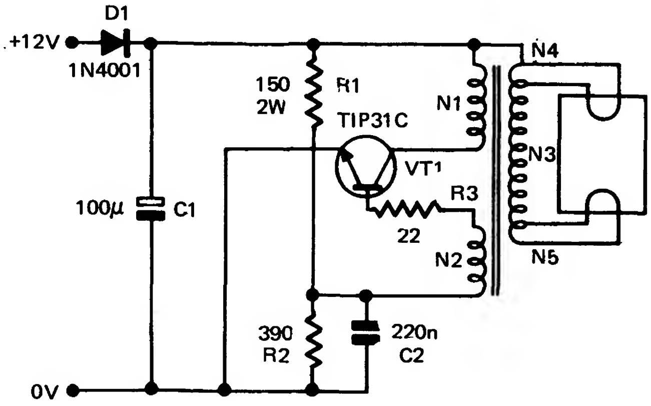
A good example of the self oscillating inverter is shown in Figure 2. It operates at 20 kHz and drives a 13W Fluorsecent Lamp, i.e. a fixed known load. The circuit is based on the conventional 'blocking oscillator' where the timing is a complex function depending on the resistors R1 and R2, capacitor C2, and the inductance of the transformer. As the transistor VT1 switches 'on' regenerative action occurs and the collector current rises until limited at $I_B h_{FE}$ when the transistor starts to switch 'off' again. The main function of the base resistor R3 is to stop parasitic oscillations but it provides a degree of protection when the device goes 'off' for its base-emitter junction. The diode D1 gives protection against a reverse polarity connection and with capacitor C1 stops radiation from the battery leads. Windings N4 and N5 provide warm up for the heaters of the lamp to reduce its striking voltage.

The typical waveforms are given in Figure 3. Points to notice are:

Until the lamp strikes, the collector-emitter voltage rises to 80V, so that the device must be capable of withstanding this voltage, although its normal running voltage is of the order of 60V.

With the 2A maximum collector current the ideal transistor for this inverter is a 100V TIP31C.

Using this device the power developed, 13W, is relatively small, but there is no reason why the output cannot be increased by employing a large power device in the same configuration.



Windings on
1½"x¼" dia Former
N1 = 100T @ 26SWG
N2 = 40T @ 30SWG

N4 40
+ +
N3 540 @ 30SWG
+ +
N5 40
Core 2"x3/16" dia Ferrite Rod

FIGURE 2. Self Oscillating Inverter

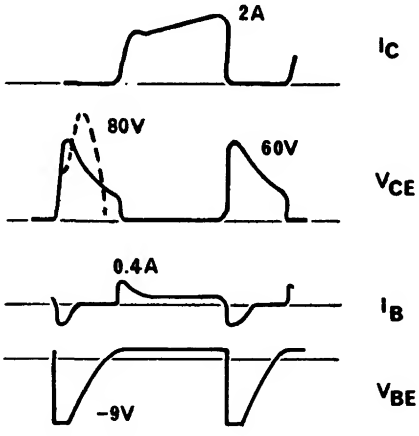


FIGURE 3. Waveforms for Lamp Inverter

120W Power Supply

Figure 4 shows an example of how, by using a BUY70B high voltage transistor for VT1, the basic circuit of a 120W power supply unit (p.s.u.) using a 25kHz converter is formed.

In this basic form, the bridge section and capacitor C1 derive a d.c. supply from the mains supply. The starting bias for the converter is supplied by the resistor R1 and diodes D1 and D2. As in the previous example, windings N1 and N2 are wound to give regeneration action and fast turn 'on' and 'off' of the transistor. As the device goes 'off' the energy stored either passes through winding N4, the diode D5 to the load (30V @ 4A) or if not required there, through the diodes D3 and D4 and winding N3 back to the supply. The 1Ω emitter resistor R2 and $3\mu F$ capacitor C2 serve to sustain the emitter voltage at $\simeq 2\frac{1}{2}V$ during the transistor turn 'off'; an important factor with high voltage transistors.

Referring to the waveform diagrams in Figure 5:- Apart from noticing that the maximum collector current I_C is $\simeq 2.5A$, the maximum collector emitter voltage V_{CE} peaks at –700V, settles to 650V–thus checking that the device ratings are not exceeded; the interesting points are given on the right in the expanded waveforms of the 'off' edge. A strong constant negative base current I_B is maintained even during the fall time as a result of the emitter network described. Typical fall times of this transistor under these conditions is 500ns. However to minimise its dissipation the collector voltage must rise at a slower rate than this; $400V/\mu s$ being a suitable figure. Therefore to achieve this controlled rise a special circuit must be employed, as shown in Figure 6.

As the transistor switches 'off' and the collector current falls, the primary current passes through a diode D6 into a capacitor C3 and back onto emitter resistor R2 (to effectively hold the emitter voltage up and assist turn 'off'). As I/C is constant, dV_{CE}/dt, the rate of rise of the collector voltage, is held constant as required. Resistor R3 is present to prevent a heavy capacitive discharge spike as the transistor comes 'on', diode D6 now being reverse biassed. Resistor R4, capacitor C4 and diode D7 form a maximum V_{CE} limiter. The voltage at their common point is at approximately 700V and the diode therefore removes any spikes on the collector which would otherwise exceed this level.

In the basic p.s.u. circuit the power output is proportional to the square of the supply voltage. This means that in order to take account of supply voltage variations the transformer must be made physically large enough to tolerate a large power increase at the high supply voltage level. If provision can be made in the p.s.u. so that the output power is proportional only to the supply voltage, then considerable saving can be made in transformer material. This can be achieved by using the peak I_E limiter section shown in Figure 7. When the thyristor Th1 fires the base of the transistor VT1 is shorted to zero so terminating its conduction period. The thyristor firing point is governed by the supply voltage (via the resistor divider R5 and R6) and the instantaneous emitter

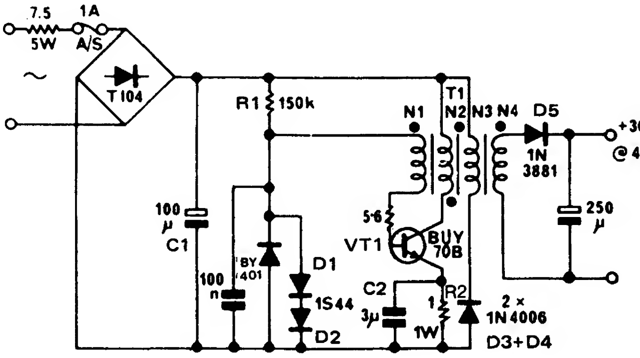


FIGURE 4. Basic 120W Power Supply Unit

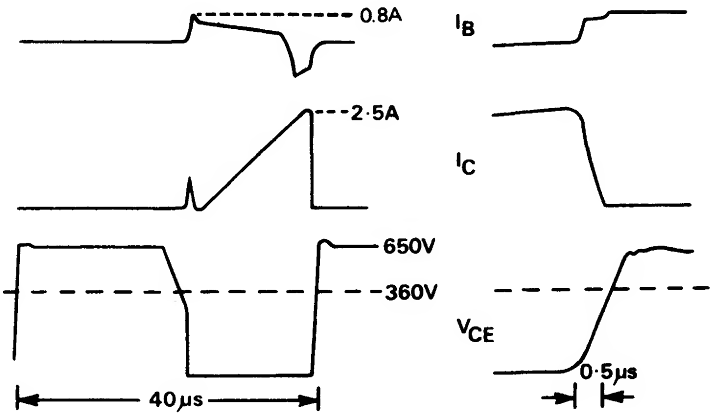


FIGURE 5. Waveforms of 25kHz Converter

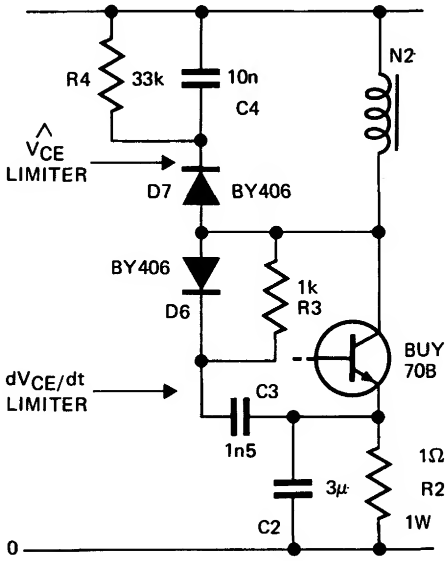


FIGURE 6. Controlled V_{CE} Rise Circuit

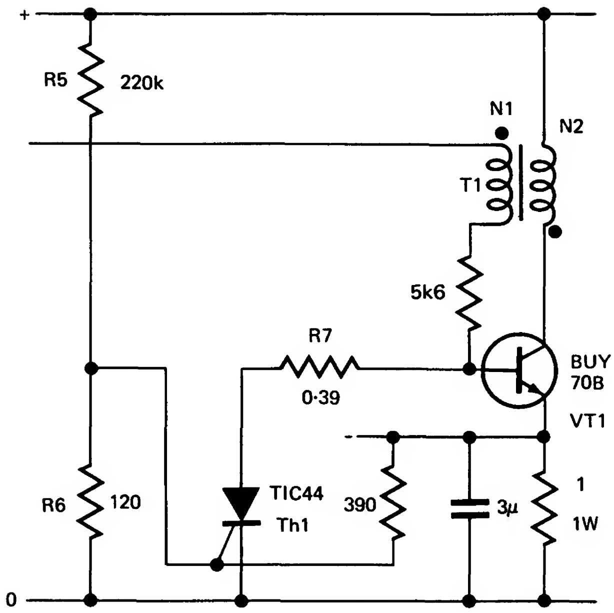

+
R5
220k
N1
N2
T1
5k6
R7
0·39
BUY
70B
VT1
R6
120
TIC44
Th1
390
3µ
1
1W
0

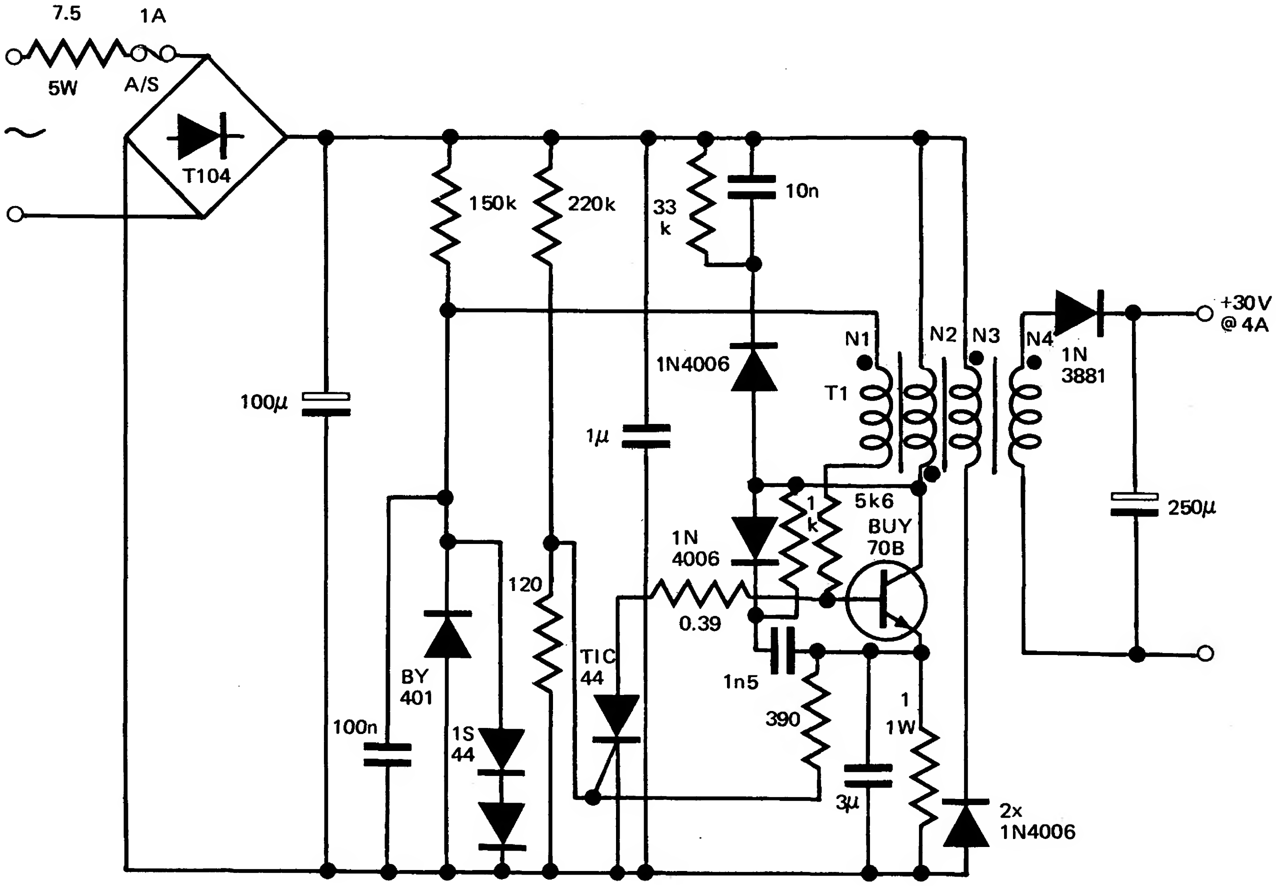
FIGURE 7. Peak I_E Limiter

current. As the supply voltage rises the peak emitter current value which causes thyristor firing reduces. Thus as the supply voltage increases the peak transistor emitter current reduces but the operational frequency of the converter increases. (Resistor R7 is present to prevent the anode current maximum of the thyristor being exceeded.)

With these two control circuits in position the basic circuit becomes the complete 120W p.s.u. shown in Figure 8. Although it appears complex, it is only made up of the simple circuit blocks previously described. It will operate into a short circuited load, and when compared with a conventional power supply, which, effectively, is the function it is performing, its cost disadvantage due to its complexity is offset by:

1. Size: It is much more compact and lighter as the large mains transformer and large low voltage capacitor are not used.
2. Efficiency: This is high, greater than 90% being achievable.

Thus such a unit should be seriously considered when size and/or efficiency are important criteria.


7.5
5W
1A
A/S
~
T104
100µ
150k
220k
33k
10n
1µ
1N4006
N1
N2
N3
N4
T1
1N3881
+30V @ 4A
250µ
1k
5k6
BUY 70B
1N4006
0.39
1n5
390
3µ
1 1W
2x 1N4006
120
TIC 44
BY 401
100n
1S 44

T1. Core: FX2243. Former: DT2206
Winding Order: ½ N3 40T 26 s.w.g., ½ N2 40T 24 s.w.g., N4 8T 22 s.w.g., N1 1T 0·125 in.cu. foil, rest N2 31T 24 s.w.g., rest N3 88T 26 s.w.g. All windings insulated.

FIGURE 8. The Complete 120W P.S.U.

SINGLE ENDED DRIVEN CIRCUITS

25V Shunt Switching Converter (Chopper)

The switching converter or 'chopper' supply[2], whose 4 fundamental components, i.e. a transistor, a diode, a capacitor and an inductor, as shown in Figure 9, provides a regulated output voltage in spite of wide variations in input voltage. Here the single transistor VT1 acts as the switch, the inductor L acts as the energy transfer device, the diode D1 reclaims the stored energy from the inductor after the transistor has switched off, and the capacitor C1 connected across the output terminals acts as an energy storage device and reduces the ripple voltage. There are two major ways of arranging the 4 basic components between input voltage V_S, output voltage V_O and the common line. The circuit shown with the transistor across the input, is the shunt mode, and has a characteristic where V_O is greater than V_S—the extent depending on the duty cycle. The normal working area is marked on the graph with a thicker line. The width of the collector current I_C pulses varies with input voltage V_S variation to maintain V_O stable, i.e. with V_S low the duty cycle is high and with V_S high, the duty cycle goes low.

Figure 10 shows a practical shunt switching converter. The four basic components, VT1, L, D1 and C1 are as before and the rest of the circuit comprises the voltage reference–zener diode D2, the error amplifier, transistor VT4 and resistor R1 to R4, and the duty cycle generator, programmable unijunction transistor (p.u.t.) VT3. The latter's 'off' time is determined by the charging of capacitor C2 through resistor R6 and the forward biassed base-emitter diode of transistor VT2. When the voltage on the gate of the p.u.t. exceeds its peak point voltage V_P, it fires forcing the lower end of capacitor C2 negative so switching 'off' transistor VT2. Capacitor C2 then discharges through resistor R7 and the gate impedance of the conducting p.u.t. The discharge stops when the lower end of capacitor C2's voltage rises sufficiently positive to forward bias the base-emitter of transistor VT2 when the cycle repeats. The discharge time may be shortened by additional current from the error amplifier transistor VT4. If, for instance, a rise occurs in the 25V output supply, transistor VT4 passes extra current, shortening the capacitor's discharge time, reducing the 'off' time transistor VT2, and the 'on' time of the output Darlington VT1. Thus less will be stored on the inductor L causing the output voltage to fall and compensate for the original rise. (Note that the p.u.t. operates with a fixed 'off' time and a variable

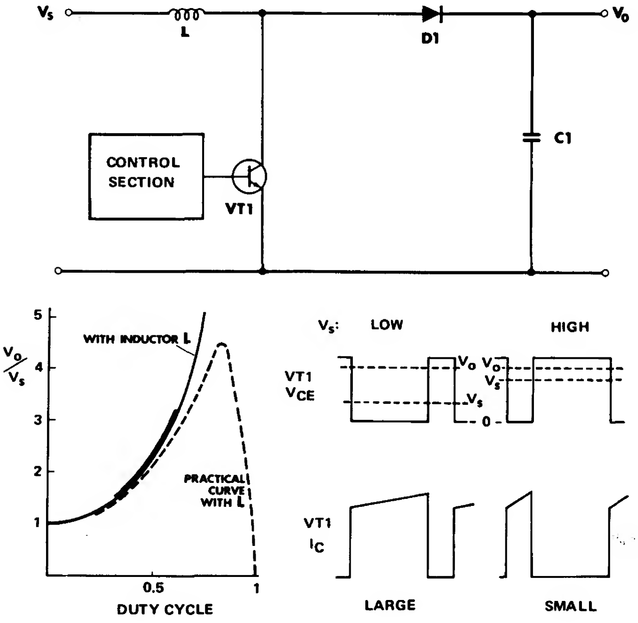
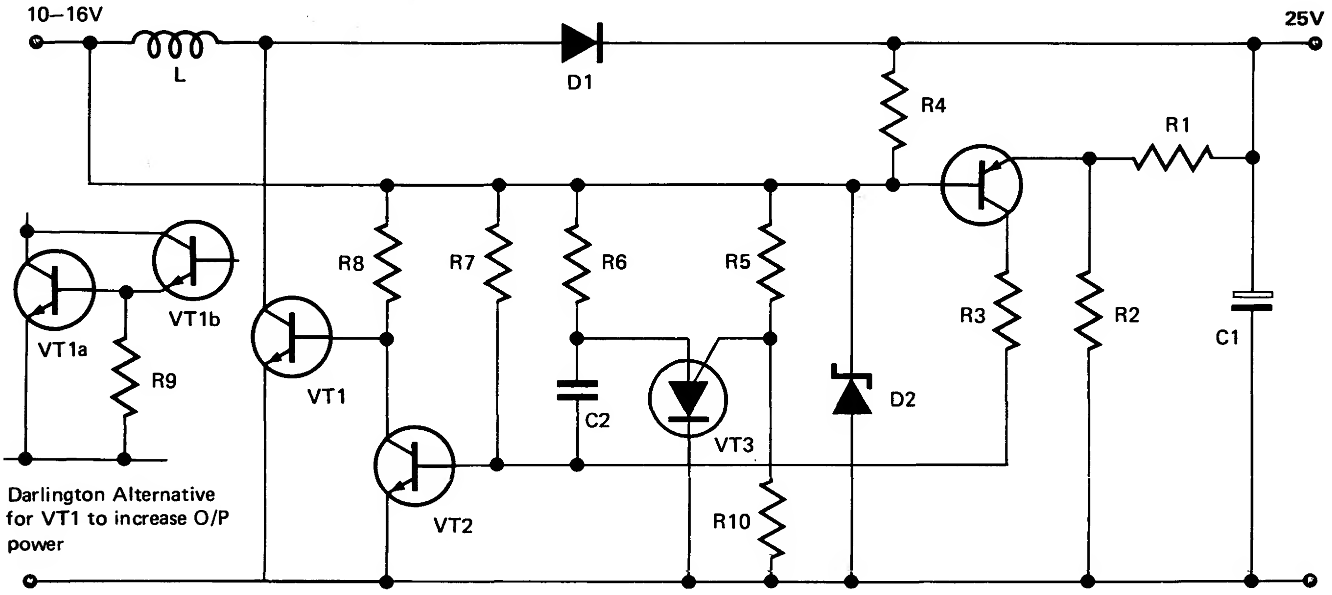


FIGURE 9. Basic Switching Converter and Waveforms



C1	100µF	L	1.5mH 4A	VT2	BC184	R1	910Ω	R4	1kΩ	R7	220kΩ	R10	3k9Ω
C2	1nF		VT1a TIP41	VT3	A7T6027	R2	390Ω	R5	2k2Ω	R8	2k2Ω		
D2	1S2068		VT1b TIS90	VT4	BC212	R3	4k7Ω	R6	10kΩ	R9	27Ω		

FIGURE 10. Practical Shunt Switching Converter

'on' time giving a variable duty cycle system.) If the converter is required to provide 30W, say, then transistor VT1 will pass approximately 3.5A and requires about 0.5A base drive through resistor R8. The p.u.t. provides only a small amount of current so that transistor VT2 cannot readily provide this level of drive. Therefore, instead of a single transistor for VT1, a Darlington arrangement must be used. Table 1 shows the diodes which have the speed and power necessary to be used in position D1.

Table 1. Fast Diodes for D1 Position

Case	$I_{F(av)}$ A	V_{RRM} V	Series
Stud	6	50-1000	BYW11-50 to 1000*
	6	50-600	1N3879-83/R
	12	50-600	1N3889-93/R
	15	50-1000	BYW12-50 to 1000*
Top Hat	1.5	200	BYW10-200
	1.5	300	BYW10-300
Plastic	1†	60-50	1SX170-5

* Soft Recovery

† Suitable for up to 20W only

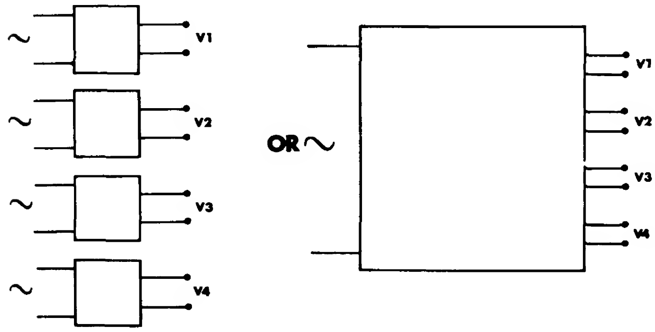


FIGURE 11. Alternative Arrangement for Multiple Output Power Supply System

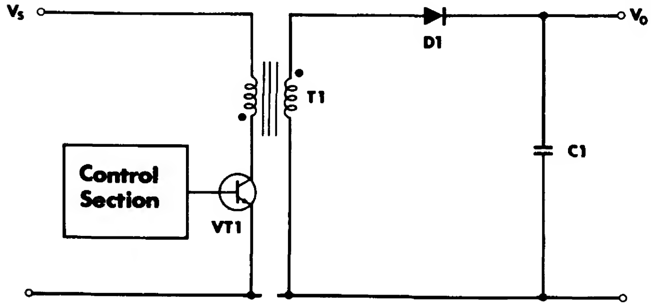


FIGURE 12. Basic Shunt Chopper with Isolation

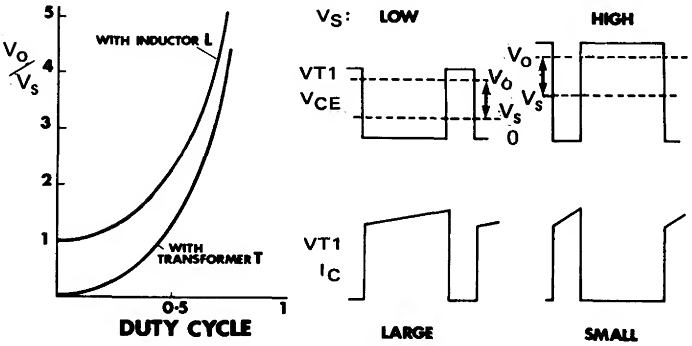


FIGURE 13. Shunt Chopper Waveforms

A Multiple Isolated Output Shunt Chopper Supply

In complex systems where, say, four stabilized power supplies are required, the designer has the choice of four separate supplies, each taken from the a.c. mains supply and producing regulated outputs, or one large supply producing all four outputs, as shown in Figure 11. The advantage of the latter is that it will be physically smaller than four separate units and since the number of components is reduced the potential reliability is higher.

As previously stated the normal shunt chopper, has for one of its four fundamental components, an inductor. By using a transformer in place of the inductor the common zero or earth line can be broken and isolation provided. Also by placing further windings on the secondary side of the transformer the required multiple outputs can be obtained. Figure 12 shows the new arrangement of the components in this type of shunt chopper circuit. Again the fundamental mode of operation is for the control circuit to switch transistor VT1 'on' for a certain time to store up energy from the supply V_S now in the transformer; then to switch transistor VT1 'off' and transfer the energy via diode D1 to the output V_O. Capacitor C1 serves as an energy storage device reducing the ripple voltage. Unlike the series type of power supply, chopper or conventional regulated, where if the transistor fails by going short circuit the output voltage goes to the input value; the shunt chopper is fail safe as the fuse in the V_S supply blows. Similarly if the transistor goes open circuit the output just goes to zero. With regulation tending to be poor at low power levels, it is usually necessary, to maintain a reasonably stable output voltage, to keep a minimum loading; but this is usually the case with a multiple output supply. The starting circuits for the shunt mode are, however, more complex than those required for the series mode.

In Figure 13 the relationship of V_O/V_S with duty cycle for a shunt chopper circuit using a transformer is compared with that for one with an inductor, and the state of its transistor's collector voltage and current for a low and high input voltage V_S shown. From the former it is seen that at a 0.5 (50:50) duty cycle the output voltage V_O is equal to the input supply voltage V_S (i.e. the peak voltage on transistor VT1 is twice the supply voltage V_S), and the steep curve indicates that only a small change of duty cycle is necessary to compensate for a large change of supply voltage, V_S, to maintain the output voltage V_O, constant. For constant output power, the lower the input voltage V_S, the greater the average current required and thus the duty cycle is large. If the input voltage V_S increases then, for constant power, the average current required is less, and the transistor is therefore required to conduct for less time and the duty cycle is small.

The small size of modern electronic equipment means that it is often necessary to operate it at a distance from a mains supply so that it is an advantage to be able to operate

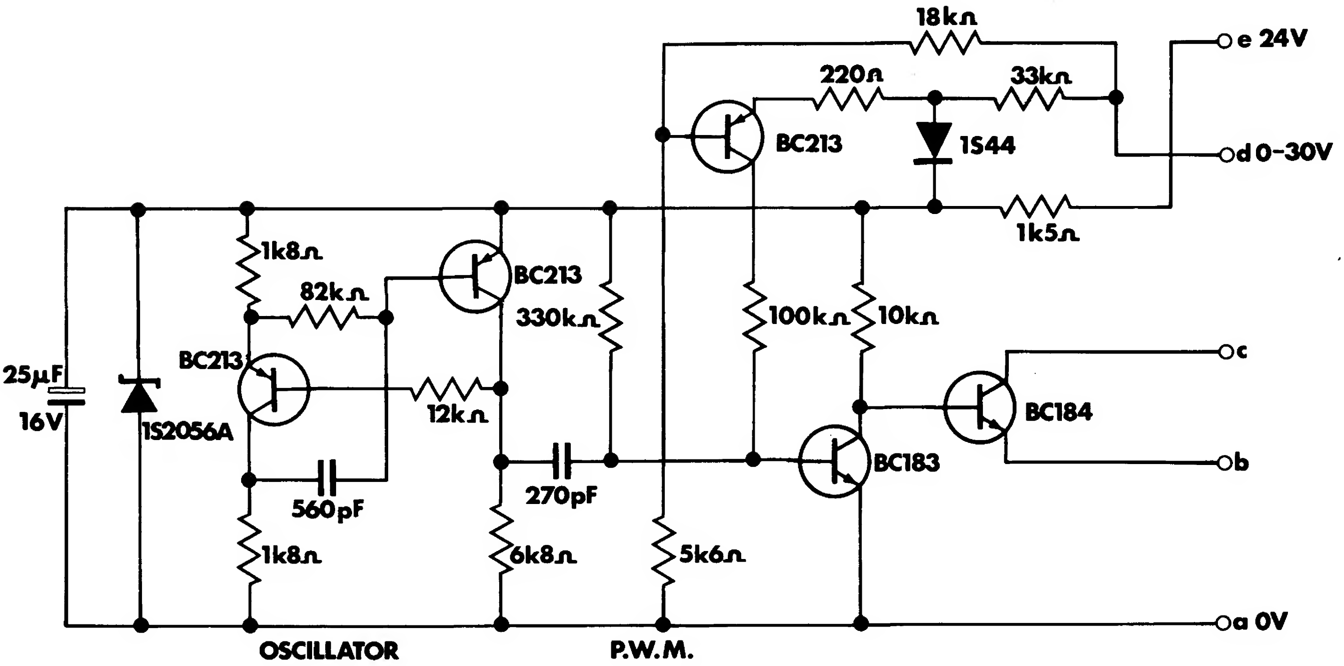


FIGURE 14. Discrete Control Circuit for Chopper

it from a.c. mains or batteries. Thus the practical discrete control circuit for a shunt chopper, shown in Figure 14, is designed to operate from 24V ± 8V (applied at e) which can be derived either using a simple step down transformer and bridge circuit from a 240/220V a.c. supply or a 24V battery–i.e. of worse case values 32 or 16V. This is fed through a 1k5Ω resistor to provide across a 5.6V zener diode (the 1S2056A) a reference voltage and supply rail for the control circuit. The 20kHz oscillator employs two BC213 transistors in a configuration chosen for its high astable working capability and good starting characteristics, i.e. it will oscillate from approximately 1½V at virtually the correct frequency. The $\simeq 4\mu s$ positive output pulse from the collector of the second transistor is coupled via the 270pF capacitor to the base of the BC183 transistor pulse width modulator. With no current flowing from the error amplifier at start up, the current flowing through the 330kΩ resistor passes insufficient current to discharge the 270pF capacitor, so that this transistor is only turned on for 4μs. When the supply is in operation the capacitor is discharged at a faster rate by the error amplifier transistor's (another BC213) current which turns the pulse width modulator on before the arrival of the next 4μs pulse, lengthening the 'on' conducting time. As the emitter of the error amplifier is taken to the 5.6V supply via the 1S44 diode, its base in normal operation sits at approximately 5.6V as the forward voltage drop of the diode.V_F, and the transistor's forward base-emitter voltage V_{BE} are approximately equal and cancel one another. If the output voltage rises, say, the base goes more positive and the transistor passes less current, recharging the capacitor at a lesser rate. The BC183 transistor is 'on' for less time, which through the power stage will cause the output to fall, thus stabilizing it. The 100kΩ resistor sets the maximum conduction time. In order that a modular construction may be employed and various output stages connected, a BC184 transistor is added to the output of this control circuit for better drive conditions and therefore, with its collector and emitter connections (c and b respectively), the control circuit has five connections (a to e) to be made to the rest of the system's circuits.

An alternative control circuit employing integrated circuits (i.c.s) which gives greater stabilization is shown in Figure 15. Two of the i.c.s. used are the versatile SN52/72555 precision timer. These devices are capable of producing accurate time delays or oscillation which is independent of the large range of supply voltage (5 to 15V) from which they will operate. Used in the astable multivibrator mode for the 25kHz oscillator of the control circuit, both the frequency and duty cycle are independently controlled by only the external two resistors (R_A = 4k7Ω and R_B = 2k7Ω) and capacitor (C = 5n6F). The capacitor charges through both resistors, and discharges, through resistor R_B only, between the threshold voltage level (approximately two-thirds of the supply voltage) and the trigger voltage level (approximately one-third of the supply voltage). As therefore the charge and discharge times are independent of the supply voltage this accounts for the frequency and duty cycle being independent of supply voltage. The timing for the circuit is given by:

Output high level duration, $t_H = 0{\cdot}693\,(R_A + R_B)C$
Output low level duration, $t_L = 0{\cdot}693\,R_B.C$
Therefore the frequency, $f = 1/(t_H + t_L)$
$= 1{\cdot}44/(R_A + 2R_B).C$

The oscillator output is coupled through the 100pF capacitor and 1k8Ω resistor to the trigger of the second '555 used as the pulse width modulator. The conventional method of pulse width modulating using this i.c., i.e. applying an external voltage or current to the control voltage pin (5), is not used as it is not possible to reduce the pulse width to zero. The configuration for monostable

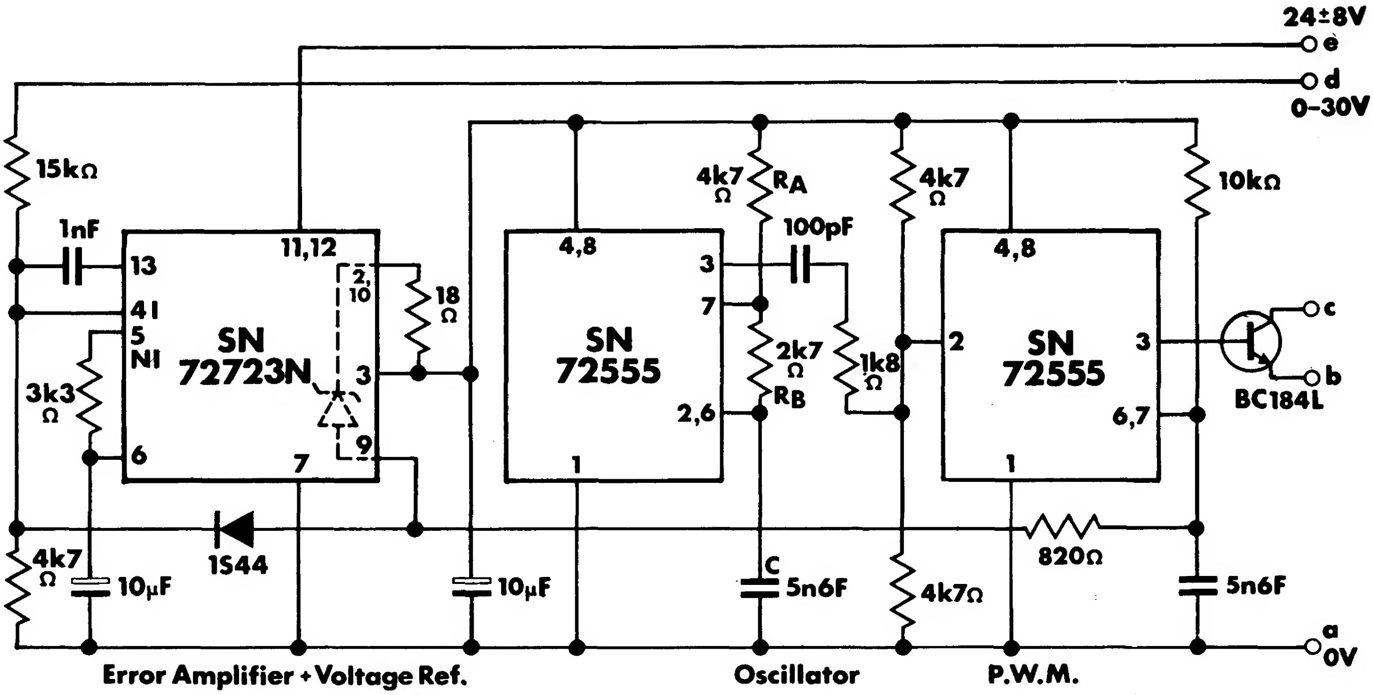

24±8V
e
d
0-30V
15kΩ
1nF
13
41
5
NI
SN 72723N
11,12
2,
10
3
9
6
7
18 Ω
3k3 Ω
4k7 Ω
10μF
1S44
10μF
4,8
SN 72555
3
7
2,6
1
4k7 Ω
RA
100pF
2k7 Ω
RB
1k8 Ω
C
5n6F
4k7 Ω
4k7Ω
4,8
2
SN 72555
3
6,7
1
820Ω
10kΩ
c
b
BC184L
5n6F
a
0V
Error Amplifier + Voltage Ref.
Oscillator
P.W.M.

FIGURE 15. I.C. Control Circuit for Chopper

operation is used and the width of the output pulse (from pin 3) changed by providing a proportional current through the 820Ω resistor to assist in the charging of the timing capacitor. No decoupling capacitor from the control voltage input to the zero voltage line was found to be necessary to improve the operation of either of these two i.c.s. Although the i.c. has a 200mA sink or source output current capability, the output was standardised by using, as with the discrete control circuit, a BC184 transistor to allow a modular output stage approach. The pulse width control voltage is provided from the third i.c., an SN72723N precision voltage regulator. It does this by measuring the feedback error voltage from the d input to the Inverting input, comparing it against the internal 7V reference voltage set on the Non-Inverting input, and modifies the output voltage (pin 10) accordingly. This voltage is level shifted by means of the internal 6V zener diode, so that it is from pin 9 that the control voltage is taken. Besides acting as an error amplifier this also provides a suitable supply voltage rail to the '555s, which, having an absolute maximum rating of 18V cannot operate directly from the 24 ± 8V (on e). The actual voltage provided varies from ≏ 6V to ≏ 14V, i.e. ≏ 7V from the inverting input, which will not rise higher than the 7V set on the non inverting input, plus ≏ 1V forward drip across the 1S44 diode, plus 6V across the internal zener diode. Thus the '555s are operated within their working range.

The arrangement of a shunt chopper system for four

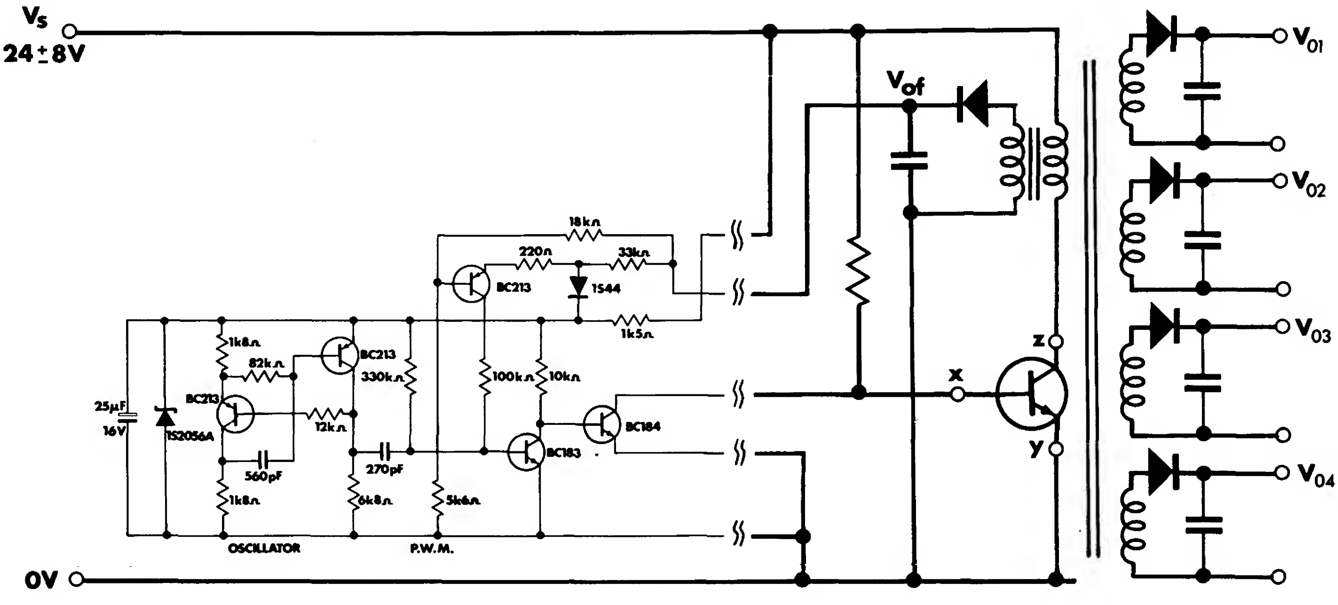

Vs
24±8V
0V
Vof
18kΩ
220Ω
33kΩ
BC213
1S44
1k5Ω
1k8Ω
82kΩ
BC213
330kΩ
BC213
25μF
16V
1S2056A
12kΩ
560pF
270pF
1k8Ω
6k8Ω
5k6Ω
100kΩ
10kΩ
BC184
BC183
OSCILLATOR
P.W.M.
x
z
y
V01
V02
V03
V04

FIGURE 16. Arrangement of Shunt Chopper System

regulated outputs is shown in Figure 16 using the discrete version control circuit. A number of methods of isolating the control circuitry can be used e.g. optocouplers. In this system an additional winding is used to monitor and give a feedback voltage of V_{of}. This takes into account, to some extent, the interwinding regulation differences of the multiple output supplies by providing a mean value back to the error amplifier in the control circuit. (It does not have to be isolated from the main chopper section so can have one side connected to 0V.) Thus the regulation of the supply rails V_{o1} to V_{o4} is dependent mainly on the transformer design as the mean level of output voltage V_{of} will be kept constant by the control circuitry. The output device which is placed between the connections x, y, z will, with a suggested 50:50 mark space ration at 24V, have a 2 X 24 = 48V across it normally and with a worst case supply of 32 will have to stand 24 + 32 = 56 peak collector volts. Therefore B options of power transistors (80V ratings) should be used. The area between x, y and z is expanded in order to provide larger and larger output currents using a modular technique.

The first of the output stages, shown in Figure 17, is for a 1A supply or ≏ 15W output power. The connections a to e are to the control circuit previously described. Between the x, y and z connections, the output transistor, a TIP29B, with its driver transistor, a super silect BFR39, are arranged in a Darlington configuration. (Darlington transistors, e.g. of the range TIP120/140, are not used as they tend to be slow in turn 'off' for these high frequency shunt chopper circuits which would increase the switching dissipation.) A form of over current protection limiting is employed. At 1A, the voltage developed across the 0.5Ω resistor is insufficient to trigger the small silect TIC45 thyristor, but when the current exceeds this value, the voltage developed is sufficient to trigger the thyristor which shorts out the drive and turns the stage 'off'. (When the driver transistor in the control circuit turns 'on' again it resets the thyristor for the next pulse.) The 22Ω base-emitter resistor serves to improve the turn 'off' speed. The 1k5Ω resistor provides base current for the Darlington configuration. The b connection as shown is such as to arrange the driver transistor in common emitter configuration. For higher output currents this is changed to an emitter follower configuration for greater drive.

This is illustrated in Figure 18 where an output stage of 3.5A and ≏ 50W total system output power is given. In practice a second transistor, here a 2N3704, is used, so that the two form a Darlington arrangement, whose speed performance is improved by the addition of the BY401 diode preventing heavy saturation of the control circuit driver transistor. For 3.5A, the output device must be TIP31B and its driver a TIP61B. Other component values are changed to suit the higher power, i.e. to ·15Ω, 6μF, 4Ω7, and 560Ω.

Figure 19 shows the 7A, ≏ 100W circuit where the larger output device required, a TIP 41B, is driven by a TIP29B. This transistor in turn needs a larger device to drive it, i.e. a TIP41 to replace the 2N3704. Again the relevant passive component values need to be changed to

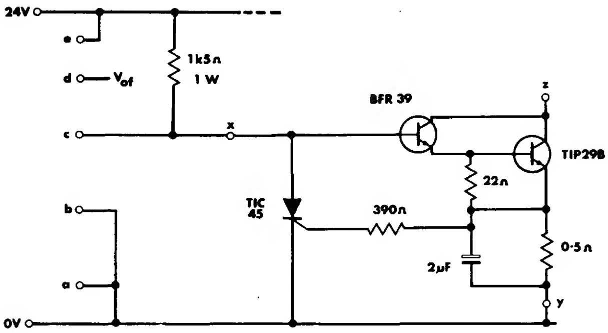


FIGURE 17. 1A Chopper Output Stage

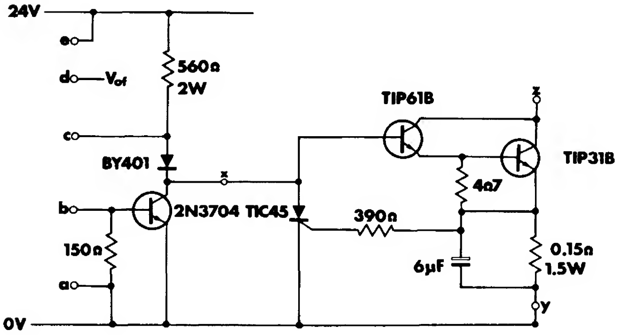


FIGURE 18. 3.5A Chopper Output Stage

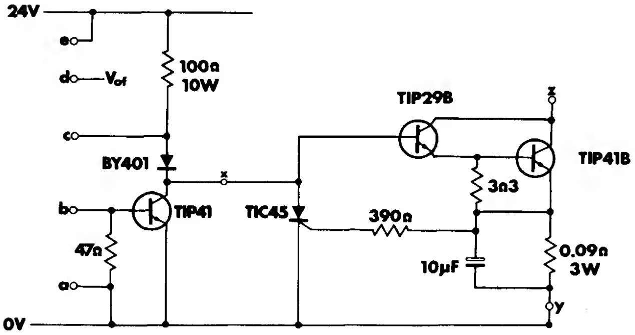


FIGURE 19. 7A Chopper Output Stage

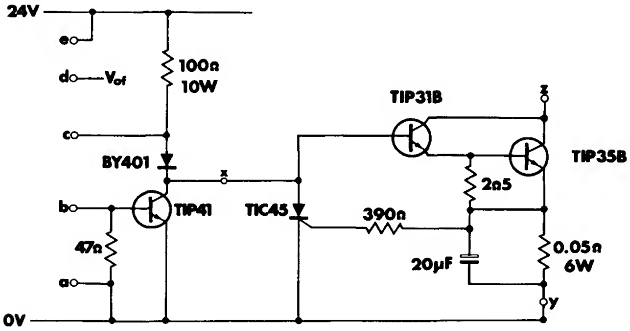


FIGURE 20. 13A Chopper Output Stage

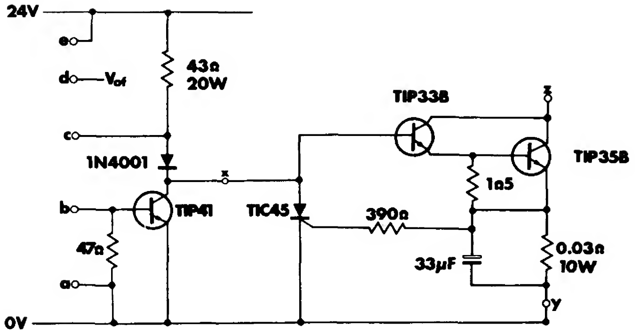


FIGURE 21. 20A Chopper Output Stage

suit the current flowing in this output stage circuit.

Similarly, as shown in Figure 20, the 13A, ≏200W circuit requires a TIP35B output device driven by a TIP31B and suitable passive component values, and for the 20A, ≏300W circuit, as shown in Figure 21, although the TIP35B is still suitable as the output device it must be driven by a TIP33B. Besides modifying the required passive component values the BY401 diode must be changed to a 1N4001 diode.

Thus by substituting the appropriate output stage, 1A to 20A, Figures 17 to 21, in the shunt chopper arrangement shown in Figure 16, the complete multiple isolated output shunt chopper system is obtained.

PUSH-PULL SELF OSCILLATING CIRCUITS

A High Voltage Supply (14kV)

For a simple supply to produce an output voltage which is a multiple or sub multiple of the input a single saturating transformer coverter[3] is ideal. The running frequency is independent of loading and can be as high as 50kHz without excessive losses in the core. The output voltage regulation will be nearly as good as the input voltage. Although the transistor turn 'on' dissipation is low the turn 'off' dissipation is high and is also independent of loading. The basic circuit is shown in Figure 22. At starting 'bleed' current flows from the 20V supply through the 1k8Ω resistor, and with diode D1 reverse biased, provides base current for both transistors. The one with the best gain, transistor VT1 say, will tend to come 'on' first, and with the transformer primary and base drive windings connected in a regenerative fashion will switch 'on' fast, the other transistor, VT2, being turned 'off'. (With the system operating, diode D1 is forward biased–its cathode being more negative than 0V–providing a low impedance base source.) Transistor VT1 stays 'on' for as long as the collector current is below $h_{FE}.I_B$. The transformer is dimensioned so that it saturates. When this occurs it results in the primary inductance falling to a low level leading to a rapid increase in collector current, a corresponding rise in $V_{CE(sat)}$ of the transistor, which via the drive winding reduces the drive to the base, which further increases the collector-emitter voltage V_{CE} and gives a fast regenerative switch 'off' of transistor VT1. The stored magnetic energy in the transformer reverses the voltages on the windings and VT2 switches hard 'on'. With transistor VT2 switching 'off' the cycle repeats. As can be seen from the waveforms in Figure 23, with the transformer primary to secondary turns ratio, n, small (<10:1) the output voltage waveform is good, indicating correct transformer coupling. However as n increases to a medium number (≏50) ringing occurs on the output waveforms. At low output currents the effect of this ringing being rectified produces a rise in the output voltage and regulation deterioration. Preloading will improve the

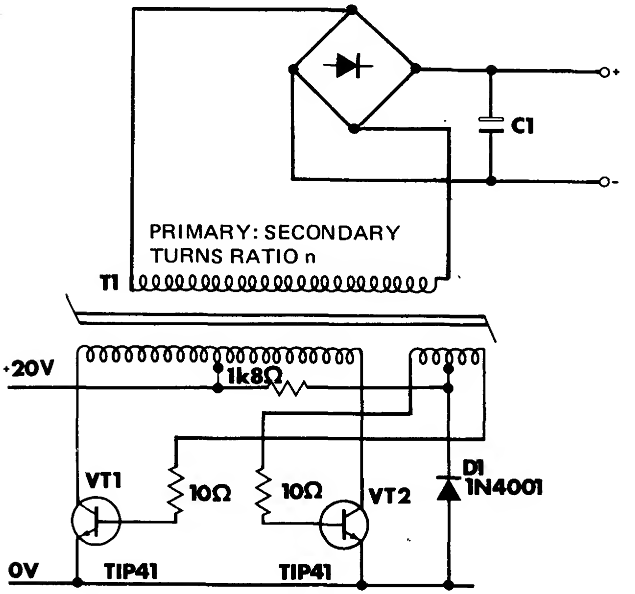


FIGURE 22. Basic Single Saturating Transformer Converter

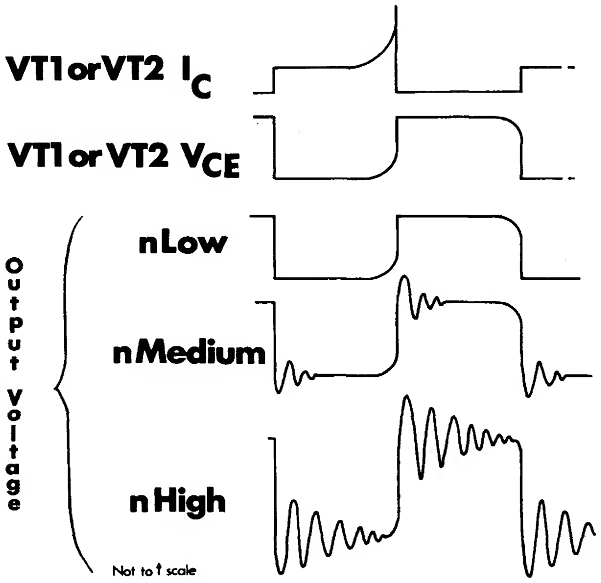


FIGURE 23. Waveforms of Single Transformer Converter

regulation but is wasteful in power consumption. At high values of n (>100) the ringing is so great that even preloading is not a practicable proposition to prevent the poor regulation performance. However, what appears to be a large disadvantage can be turned into an advantage in producing a high voltage supply, e.g. 14kV at 1mA, for applications such as supplying photo-multipliers, high vacuum systems using thermonic emission, etc.

Figure 24 shows the circuit of the basic single saturating transformer converter modified to operate at the resonant frequency of the secondary winding so that a sinewave converter is produced. (The actual frequency of operation is a function of the total number of turns and the overall size and isolation of the windings governing the leakage inductance and capacitance.) A voltage tripler is used to convert the 5kV obtained to 14kV, as ensuring adequate isolation at high voltages is difficult with transformers. The circuit for the sinewave converter has an additional three components when compared to the basic converter circuit of Figure 22. The 33nF capacitor is used to fine tune the primary to near to the secondary resonant frequency. Choke T2 performs two functions. Although the transformer waveform is now sinusoidal, the transistor should still switch from hard 'on' to hard 'off' for minimum dissipation and maximum efficiency. The winding in series with the 20V supply provides a constant current feed taking up the difference between the 20V input supply and the half sinewave on the centre tap. During the conduction period of either transistor, diode D2 is non conducting as the voltage across the second choke winding is positive. However, as illustrated in the operating waveforms given in Figure 25, during the short time that the base drive voltage passes between $\pm V_{BE}$ both transistors will be 'off'. The voltage on the centre tap of the primary winding will, during this time, tend to go very positive due mainly to the stored inductive energy of choke T2. With just over 20V across both choke T2's windings, as the supply holds the common point at +20V, the diode D2 will become forward biased, conduct and effectively clamp transformer T1's centre tap at 40V. Thus the maximum voltage across the transistors collector-emitter junctions is limited to 80V. This well defined peak voltage allows a C version of the TIP41 to be used with complete safety. The half sinewave on the 'off' collector is twice the magnitude of that on the centre tap, i.e. $2 \times \pi V_{supply}/2 \simeq 60$V. During the time that the transistor is 'on' i.e. V_{CE} is at $V_{CE(sat)}$, the transistor will conduct the collector current which peaks at ≃1.5A.

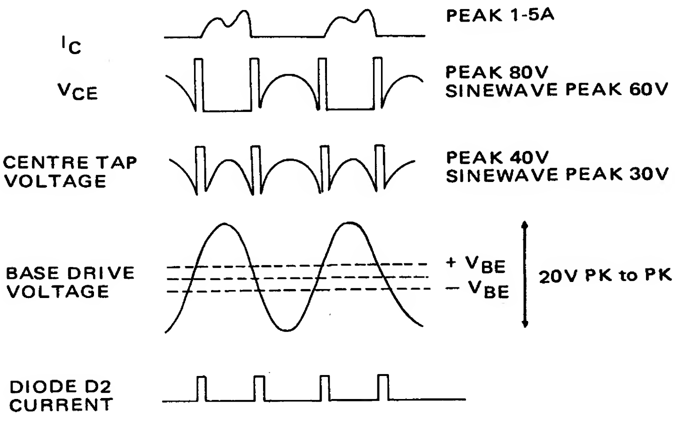


FIGURE 25. Operating Waveforms

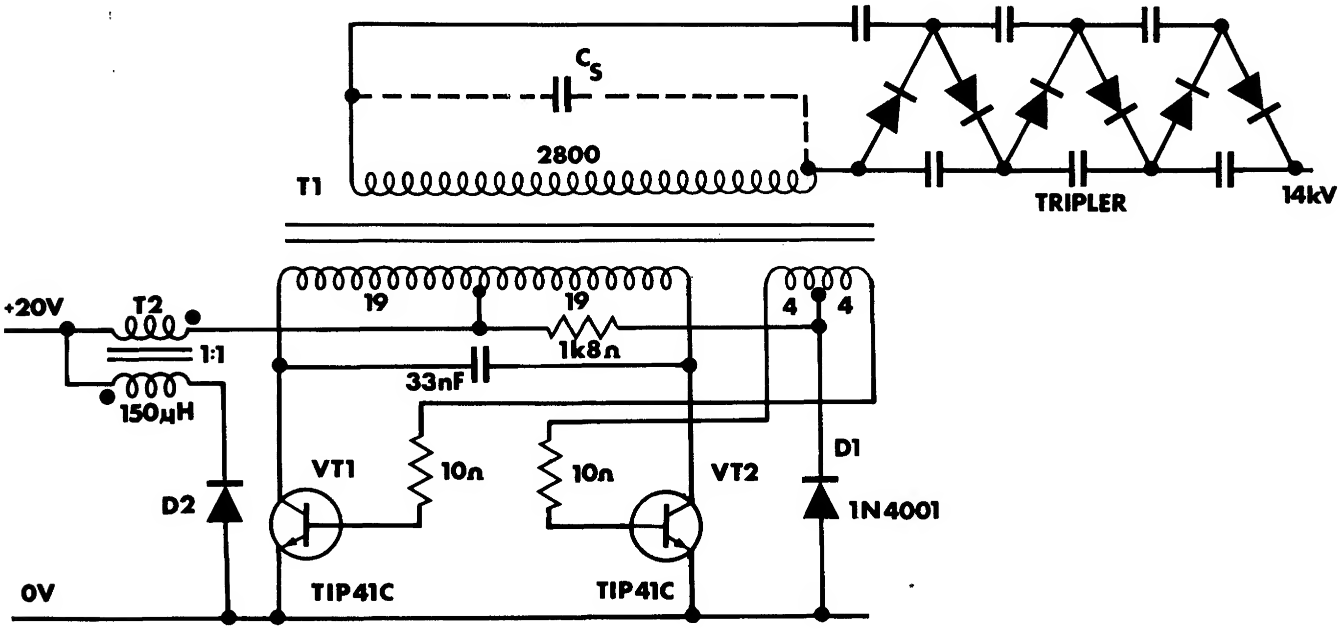


FIGURE 24. Sinewave Converter

PUSH PULL DRIVEN CIRCUITS

50Hz 12 to 240V 300W Inverters

A practical and useful example of the driven inverter, especially in times of electricity strikes, is one which will operate from a 12V battery and provide a 300W 50Hz supply, the basic output (o/p) configuration being shown in Figure 26. On the primary side each transistor's collector will swing from $V_{CE(sat)}$ i.e. approximately earth to twice the maximum battery voltage i.e. 2 X 16·5V = 33V. Therefore with a safety factor, a device rating of, say, 40V would be suitable. With 300W output 240V the average secondary current is 1·25A. Assuming an efficiency of 80%, the effective required average secondary current is 1·55A. The transformer's turns ratio must be 20, therefore the primary peak current, which must be switched by each transistor in turn, is approximately 33A. 33A 40V transistors do exist but they are extremely expensive, therefore the use of lower current transistors in parallel must usually be considered.

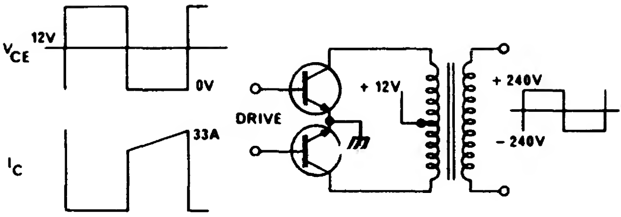


FIGURE 26. Basic Output Configuration

Figure 27 shows (a) the number of transistors required for a 12V primary, 300W, output stage plotted against device types and (b) the relative total cost of the particular number required. (In order to make $V_{CE(sat)}$ $\ngtr$ 10% of the battery voltage a collector current to base current ratio, I_C/I_B, of 8 is taken as the first calculation to derive the curve.) The cost curve recommends any of the transistors TIP41, TIP33, and TIP3055. Choosing a TIP33 transistor means that 10 transistors are required for the complete o/p stage, 5 for each side.

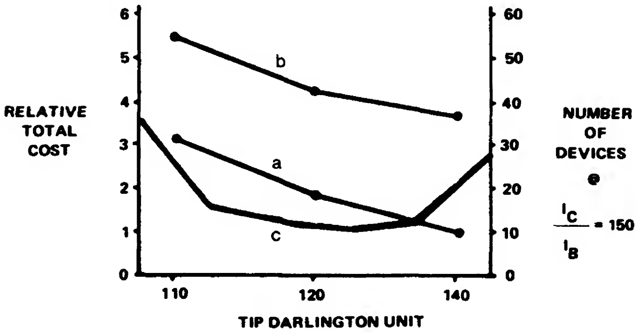


FIGURE 27. Requirement for 300W Output Stage

The practical o/p stage is shown in Figure 28 with the transistors in parallel. The 1.5Ω base resistors are there to equalize the base currents to the transistors, but note that no emitter resistors are necessary as with five in parallel, the devices are under-stressed. The 1S410 diodes, D1 and D2, are present to catch any negative voltage overshoots should

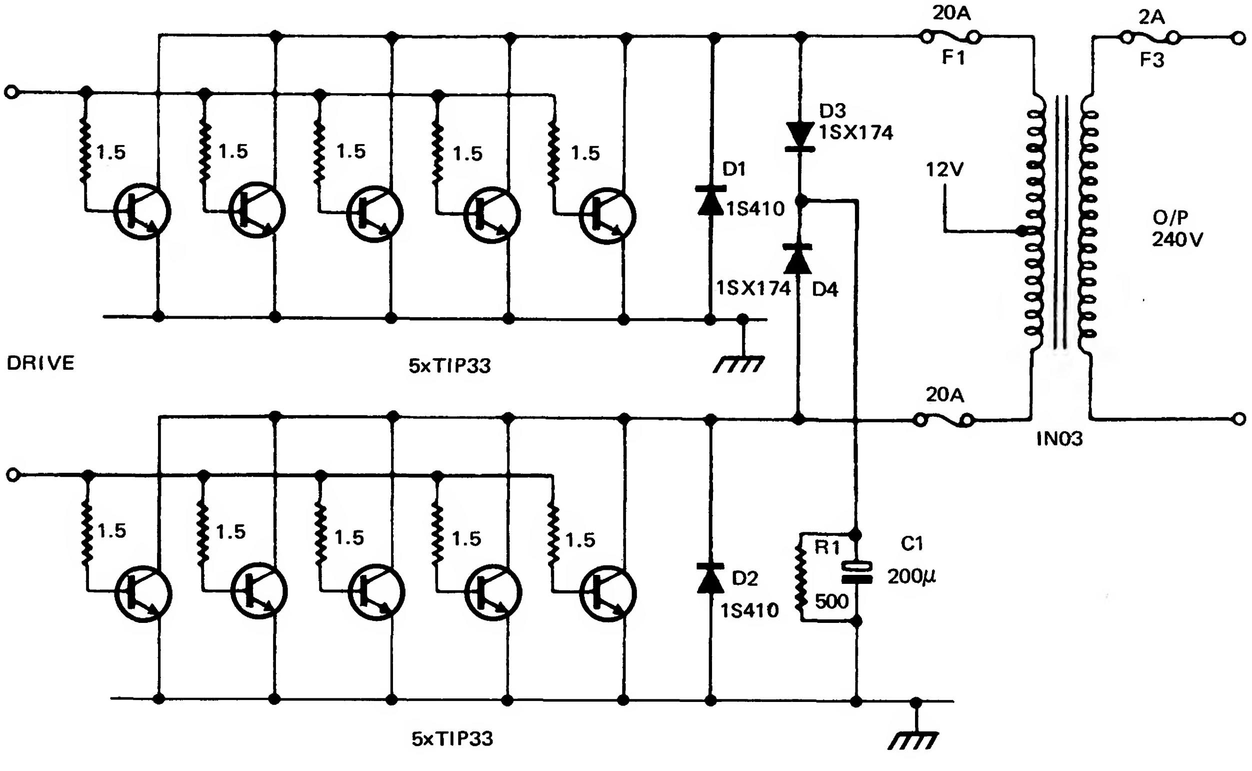


FIGURE 28 Practical Output Stage

the load be inductive. The two fast 1A rectifier diodes, D3 and D4, capacitor C1 and resistor R1 from a peak rectification circuit. Any fast short duration spike is clamped to a voltage just above twice the supply voltage. Fuses, F1 to F3, complete the protection circuits and need only be 20A on the primary side, F1 and F2, as each set of transistors is only 'on' for half the cycle.

The base current drive to this o/p stage needs to be about 4A each side and is supplied by a driver and timing circuit shown in block diagram form in Figure 29. The oscillator runs at 100Hz, i.e. twice the required output frequency, and its output, w, is divided using a bistable ÷ 2 so that two complementary outputs, y and z, of 50Hz with equal mark space ratio are obtained. (The latter is an important point as uneven mark space will cause dc magnetising to the driver and output transformers.) Waveforms y and z are a.c. coupled to two driver stages so that on start up all power transistors are certain to be 'off' until the oscillator is functioning correctly and no damage occurs to them. Using a 3:1 driver transformer, TX, the required secondary current, approximately 4A, is produced from the 1.3A primary current available.

The practical circuits to achieve these block functions are shown in Figure 30. A capacitor/resistor timed programmable unijunction transistor[4] (p.u.t.) circuit is used for the oscillator, the 'on' time being determined by capacitor C1 and resistor R1 plus potentiometer VR1. (Adjusting the latter gives fine tuning for 100Hz.) The 'off' time is fixed by the capacitor C1 and the resistor R2. The diode D1, normally placed between emitter of the transistor VT1 and earth to prevent its BV_{EBO} being exceeded, is here placed in the base so that the $V_{CE(sat)}$ output at the collector is at the correct level for driving directly into the clock input of the SN7472 divide-by-two integrated circuit (IC1). The 5V V_{CC} supply for this i.c. is derived by zener diode ZD1, resistor R3 and capacitor C2. As stated the bistable complementary outputs are a.c. coupled into the two driver stages. Use of TIP33s as the power transistors VT4 and VT5 allows uniformity with the o/p stage, but, more important, its gain at its required collector current allows a silect small signal transistors VT2 and VT3 to be used as its driver. The resistors in series with capacitors (R4 and C4, and R5 and C5) across the collector-emitters of transistors VT4/5 provide some spike damping.

Thus Figures 30 and 28 show the complete 300W 50Hz inverter. However, the driver transformer employed is a bulky and usually a costly item. Therefore it is worth considering its removal by using the Darlington transistors

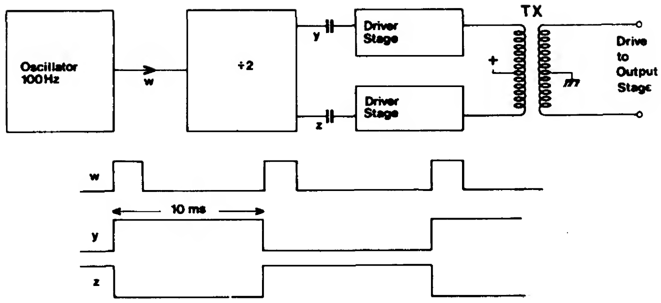

Oscillator 100Hz
w
÷2
y
z
Driver Stage
Driver Stage
TX
+
Drive to Output Stage
w
10 ms
y
z

FIGURE 29 Block Diagram and Driver Circuit

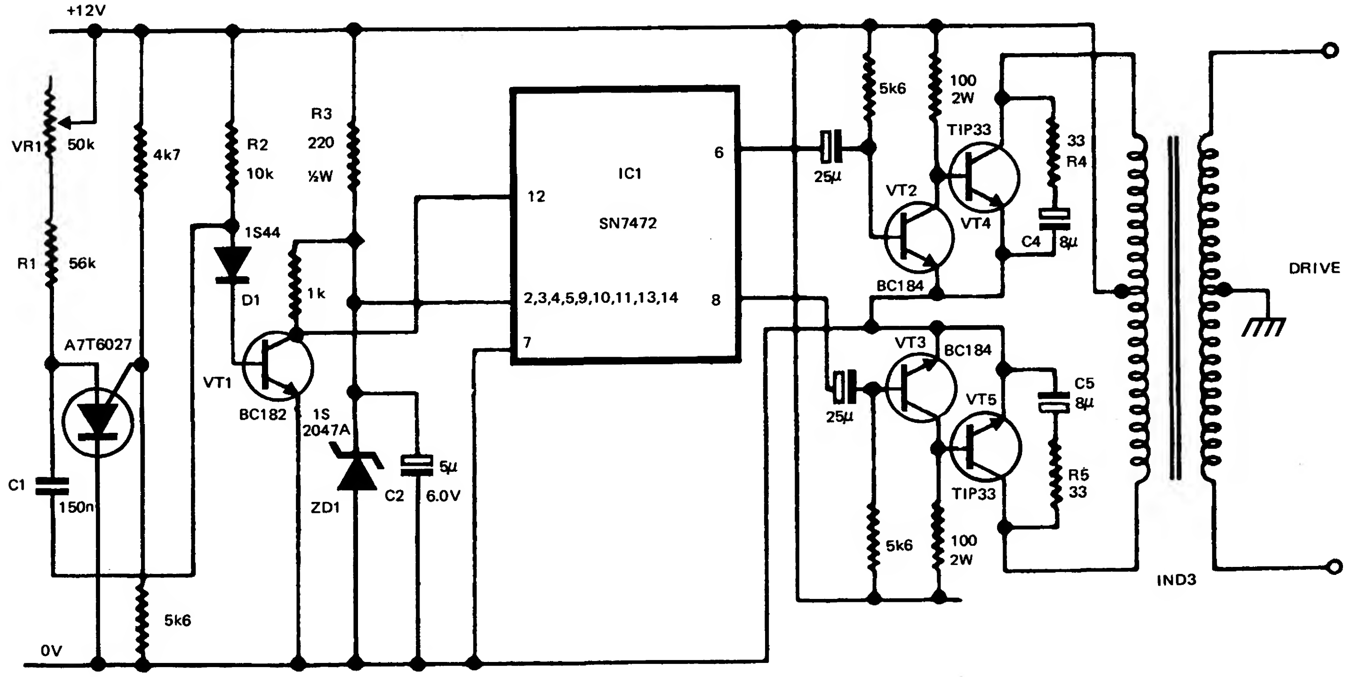

+12V
VR1
50k
4k7
R2
10k
R3
220
½W
R1
56k
1S44
D1
1k
A7T6027
VT1
BC182
1S 2047A
ZD1
C2
5μ
6.0V
C1
150n
5k6
0V
IC1
SN7472
12
6
2,3,4,5,9,10,11,13,14
8
7
25μ
5k6
100 2W
TIP33
VT2
VT4
33 R4
C4
8μ
BC184
VT3
BC184
VT5
C5 8μ
R5 33
25μ
TIP33
5k6
100 2W
IND3
DRIVE

FIGURE 30 Output Stage Driver Circuit

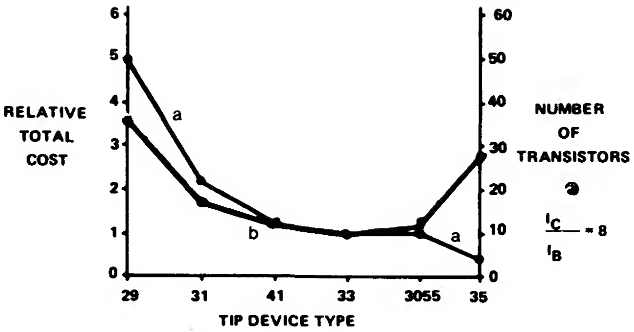


FIGURE 31 Darlington Requirement for 300W Output Stage

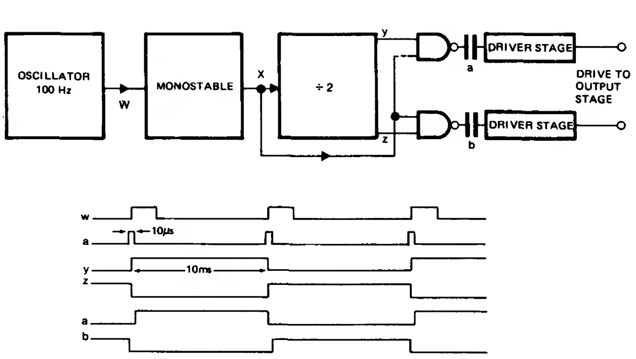

OSCILLATOR 100 Hz
W
MONOSTABLE
X
÷2
y
z
DRIVER STAGE
a
DRIVER STAGE
b
DRIVE TO OUTPUT STAGE
w
a
10μs
y
z
10ms
a
b

FIGURE 33. Modified Driver Circuit Block Diagram

in place of the discrete transistors to obtain the necessary gain in the system. Figure 31 shows, (a) assuming an I_C/I_B ratio of 150, the number of Darlington transistors required for the same specification, against Darlington device types, and (b) the relative total cost of the particular number required. Curve (c) is the relative total cost of the ordinary transistors transposed. If the driver transformer costs more than the vertical difference between (c) and the curve (b) it is economic to employ the Darlington transistors. The best type of Darlington transistors to use is TIP140s of which 5 a side are required. Figure 32 shows these fitted in the 300W o/p stage and the only difference from the ordinary transistor circuit is that with a forced gain of 150 now applying, the base resistors are increased to 22Ω. Although the driver circuit will not now require a transformer, Darlington transistors have a problem in that their turn off time (t_{off}) is long ($\simeq$10μs). The driver circuit must take account of this, otherwise both sets of output transistors could be 'on' at the same time.

Figure 33 shows in block diagram form how this is accomplished. As can be seen, it is achieved by inserting a monostable between the oscillator and divide-by-two circuit, and gating its output x, with the y and z complementary outputs to give new waveforms, a and b, to be a.c. coupled to the driver stages. The waveform diagrams show that the period of the monostable ($\simeq$10μs) is therefore subtracted from the leading edges of the waveforms a and b applied to the driver stages; thus allowing sufficient time for the 'on' Darlington transistors to switch 'off' before the others turn 'on'.

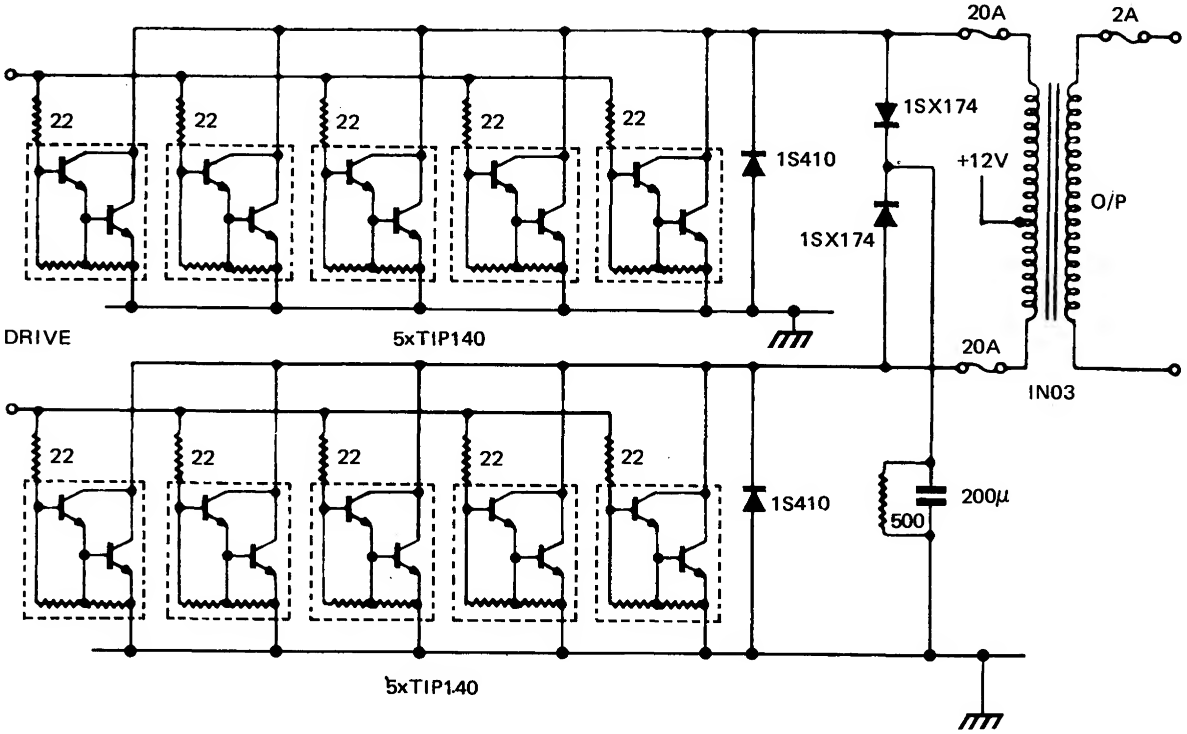
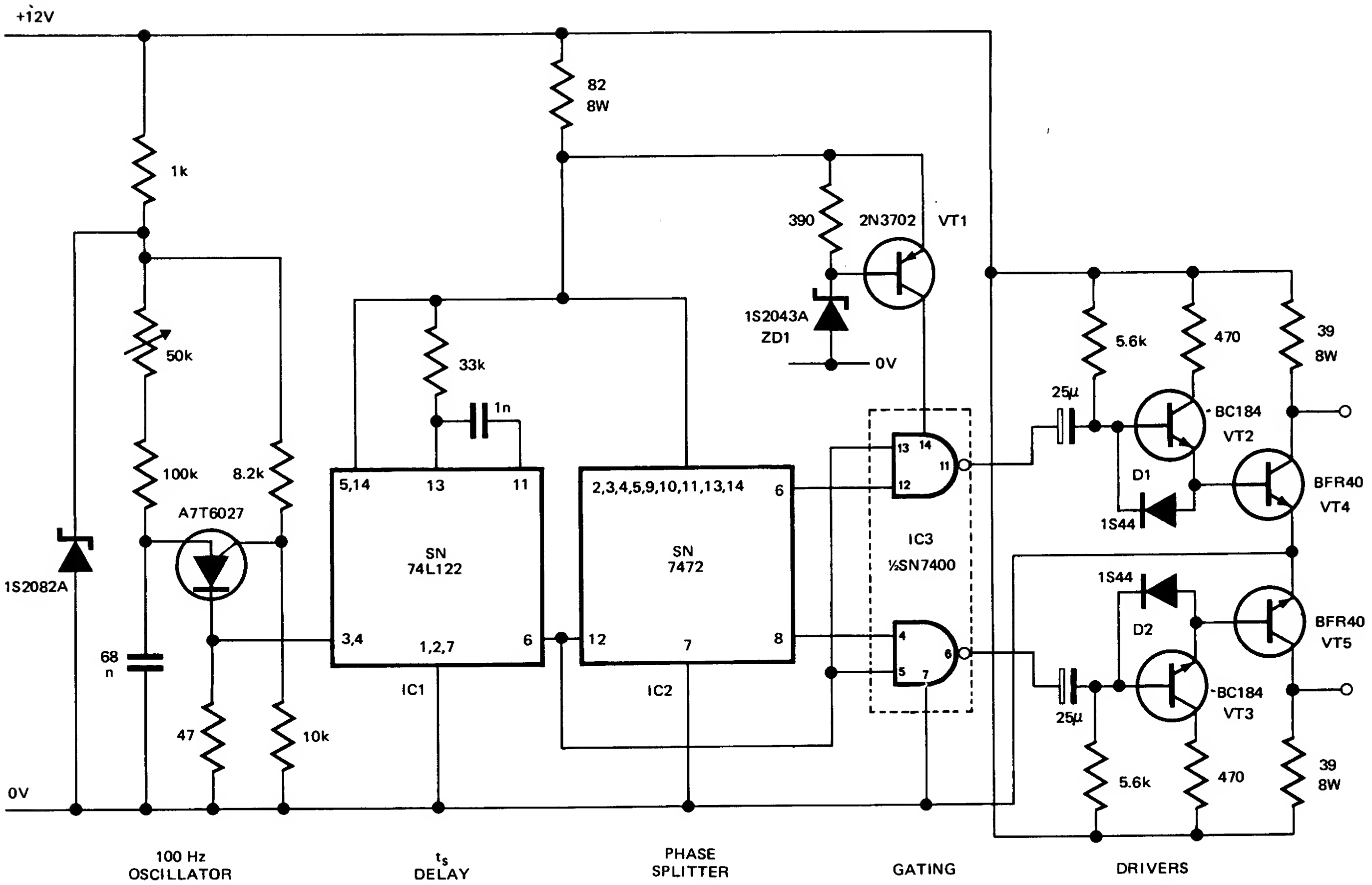

22
22
22
22
22
1S410
1SX174
1SX174
+12V
20A
2A
O/P
DRIVE
5xTIP140
20A
IN03
22
22
22
22
22
1S410
500
200μ
5xTIP1.40

FIGURE 32. Darlington 300W 50Hz Output Stage



+12V
82
8W
1k
390
2N3702
VT1
1S2043A
ZD1
0V
50k
33k
1n
5.6k
470
39
8W
25μ
BC184
VT2
D1
1S44
BFR40
VT4
100k
8.2k
A7T6027
5,14
13
11
2,3,4,5,9,10,11,13,14
6
13 14
11
12
IC3
½SN7400
SN
74L122
SN
7472
1S2082A
1S44
D2
BFR40
VT5
3,4
1,2,7
6
12
7
8
4
6
5 7
68
n
IC1
IC2
BC184
VT3
25μ
47
10k
5.6k
470
39
8W
0V
100 Hz
OSCILLATOR
t_s
DELAY
PHASE
SPLITTER
GATING
DRIVERS

FIGURE 34. Darlington Driver Circuit

The practical Darlington driver circuit is shown in Figure 34. Again a programmable unijunction transistor[4] (an A7T6027) is used for the oscillator to give a well defined pulse which will drive directly into the 't_s delay' monostable IC1. The latter is the low power version, i.e. the SN74L122, thus allowing a simple 5V power supply to be derived across zener diode ZD1 for both it and the phase splitter divide-by-two i.e. IC2. This supply is also taken to the gates, IC3, but via a transistor VT1 which does not switch 'on' initially until a full 5V level is reached. Thus an output pulse is not taken to the driver stage until the monostable is providing a correct 10μs pulse. As the driver stage needs now only to provide ≃215mA, Super Silect BFR40 transistors VT4 and VT5, themselves driven by Silect device, VT2 and VT3 can be used. The 1S44 speed up diodes, D1 and D2, across the base-emitter of the latter devices ensure that there are no t_{off} problems here. Thus Figures 34 and 32 show the complete 300W 50Hz inverter using Darlington transistors.

A Multi Purpose High Current (40A) Supply

Applications such as welding, spark erosion, battery charging, etc., conventionally use heavy bulk mains transformers. By using a switching mode supply for such equipment, considerable weight can be saved and improved efficiency obtained. However to realize these benefits the switching rate of the system must be at high frequency, e.g. 20kHz.

A block diagram of a multi-purpose high current switching mode supply is shown in Figure 35. The operation principle of the control section is similar to that employed for the 12V to 240V, 300W, 50Hz inverter described previously although the frequency of operation is, of course, changed. Here the oscillator feeding the delay monostable runs at 40kHz. The other parts of the control section are a variable pulse width monostable, a divide by two circuit and two gate circuits. The latter are followed by the driver section which in turn feeds the output and isolating stage.

The timing waveforms of the control section, and thus effectively the supply, as illustrated in Figure 36, can be used to explain how the system operates. The 40kHz oscillator provides a 4μs pulse (t) to trigger the first monstable whose 6μs delay later gives some protection against simultaneous conduction of both output stage transistors. Its pulses (u) are fed to the pulse width monostable, a divide by two circuit, and two gates. By gating v, the variable output pulse from the second monostable, and w and x, the 20kHz complementary outputs from the bistable, control outputs y and z are produced which can be varied in width by the potentiometer in the pulse width monostable from a maximum of 25–6 i.e. 19μs to zero.

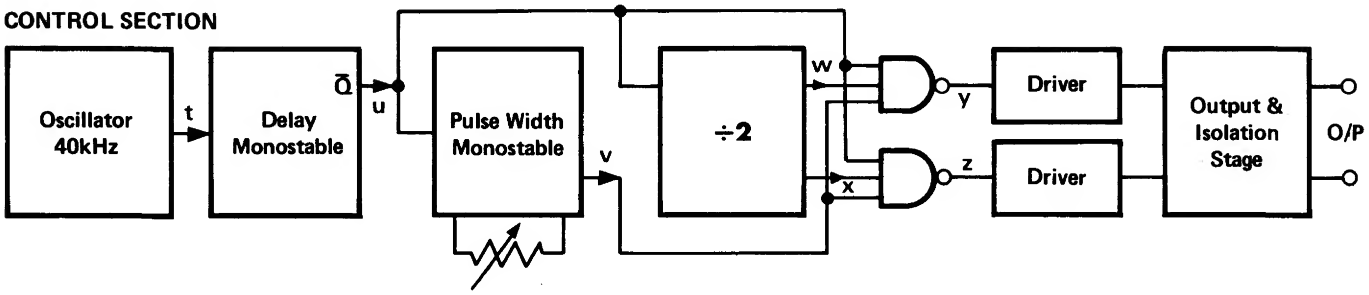

CONTROL SECTION
Oscillator 40kHz
t
Delay Monostable
Q̄
u
Pulse Width Monostable
v
÷2
w
x
y
z
Driver
Driver
Output & Isolation Stage
O/P

FIGURE 35 Block Diagram of Multi Purpose High Current Supply

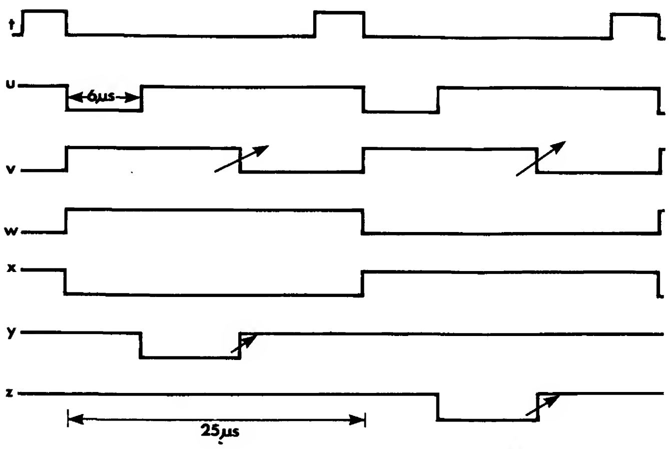

t
u
6μs
v
w
x
y
z
25μs

FIGURE 36. Timing Waveforms

The practical control section shown in Figure 37 again employs a programmable unijunction transistor[4] as the oscillator. (This functions adequately at 40kHz whereas conventional unijunction transistors would have some difficulty at this frequency.) The circuit is a conventional one. Its voltage supply is derived from a 26V rail by means of the 6k8Ω resistor, 10μF capacitor, and two 5k6Ω resistors. The latter two resistors also set the triggering level on the gate of the p.u.t. On application of a supply, the p.u.t. will be 'off', its anode being more negative than its gate. The anode voltage rises as the 680pF capacitor is charged up through the 39kΩ resistor until it goes more positive than the gate, when the p.u.t. switches 'on'. The negative edge passes through the capacitor to the base of the BC182L transistor and turns this device 'off' for a time determined by the charging rate of the same capacitor through the 10kΩ resistor and the relevant voltage step and

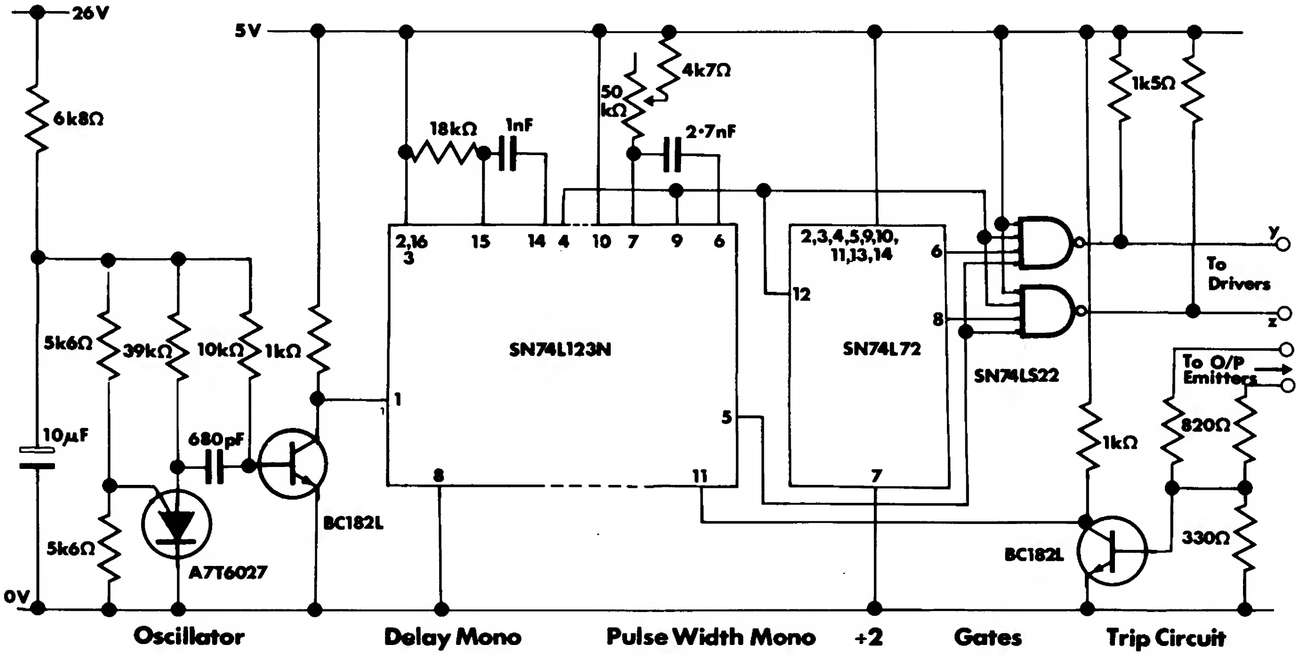

26V
5V
6k8Ω
5k6Ω
39kΩ
10kΩ
1kΩ
10μF
680pF
5k6Ω
A7T6027
BC182L
0V
18kΩ
1nF
50 kΩ
4k7Ω
2·7nF
2,16 3
15
14
4
10
7
9
6
1
8
11
5
SN74L123N
2,3,4,5,9,10, 11,13,14
12
6
8
7
SN74L72
SN74LS22
1k5Ω
y
z
To Drivers
To O/P Emitters
820Ω
1kΩ
330Ω
BC182L
Oscillator
Delay Mono
Pulse Width Mono
÷2
Gates
Trip Circuit

FIGURE 37. Practical Control Section Circuit

levels. Use of a transistor's base to emitter junction, rather than a diode in this position, allows a low impedance output pulse with correct logic levels to be taken from the collector to trigger the monostable. The 'L123N package contains two monostable circuits. The first of these with a 6μs pulse, set by the 18kΩ resistor and 1nF capacitor, is used as the delay generator. The second circuit with its timing period determined by the 2n7F capacitor, 4k7Ω resistor, and a 50kΩ potentiometer varies the output pulse width from <6μs to >25μs. Conventional i.c.s are employed for the divide-by-two circuit (a '72 edge triggered flip-flip) and gates. (All the i.c.s used however, are the low power versions, although the supply is for high currents, to enable a simple 5V supply to be made and give better noise protection.) The trip circuit, which is not shown in the block diagram, uses a BC182L transistor. This senses when the voltage across resistors (and thus the current through them) placed in the emitter circuits of the output stage exceeds a safe value and switches 'on'. This applies approximately zero volts to the 'clear' of the monostables terminating its pulse, switching 'on' the driver stage and thus turning 'off' the output transistor conducting too much current.

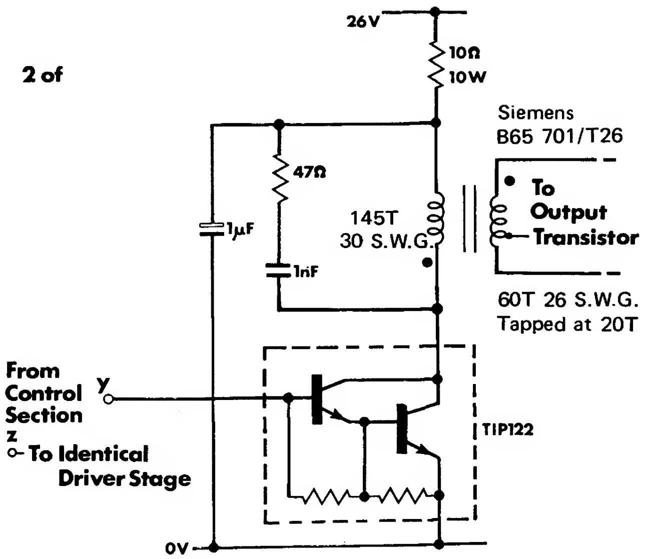

2 of
26V
10Ω
10W
Siemens
B65 701/T26
47Ω
1μF
145T
30 S.W.G.
1nF
To
Output
Transistor
60T 26 S.W.G.
Tapped at 20T
From
Control
Section
y
z
To Identical
Driver Stage
TIP122
0V

FIGURE 38. A Driver Stage

The driver stages use TIP122 Darlington transistors, as shown in Figure 38, which when turned 'off' by the waveform y (or z) from the control section release the energy (stored in the driver transformer), built up from the 26V supply when the Darlington transistor is 'on'. (The slow turn 'off' time of the Darlington transistors is not detrimental in this position as it only introduces a slight increase in the delay period before the output transistors turn 'on'. Their turn 'on' time is sufficiently fast.) The 47Ω resistor and 1nF capacitor across the primary winding of the driver transformer provide damping, and a 100Ω 10W resistor provides a current limit to avoid taking too much current at short conduction times. The released stored-energy passes from the tapping on the secondary to provide base drive current for the two BU137 high power transistors of output stage shown in Figure 39.

To ensure that these devices switch 'off' rapidly, the top end of the driver secondary winding is taken through 1S9001 diodes to prevent the transistors from going hard into saturation. The method of achieving this is to position

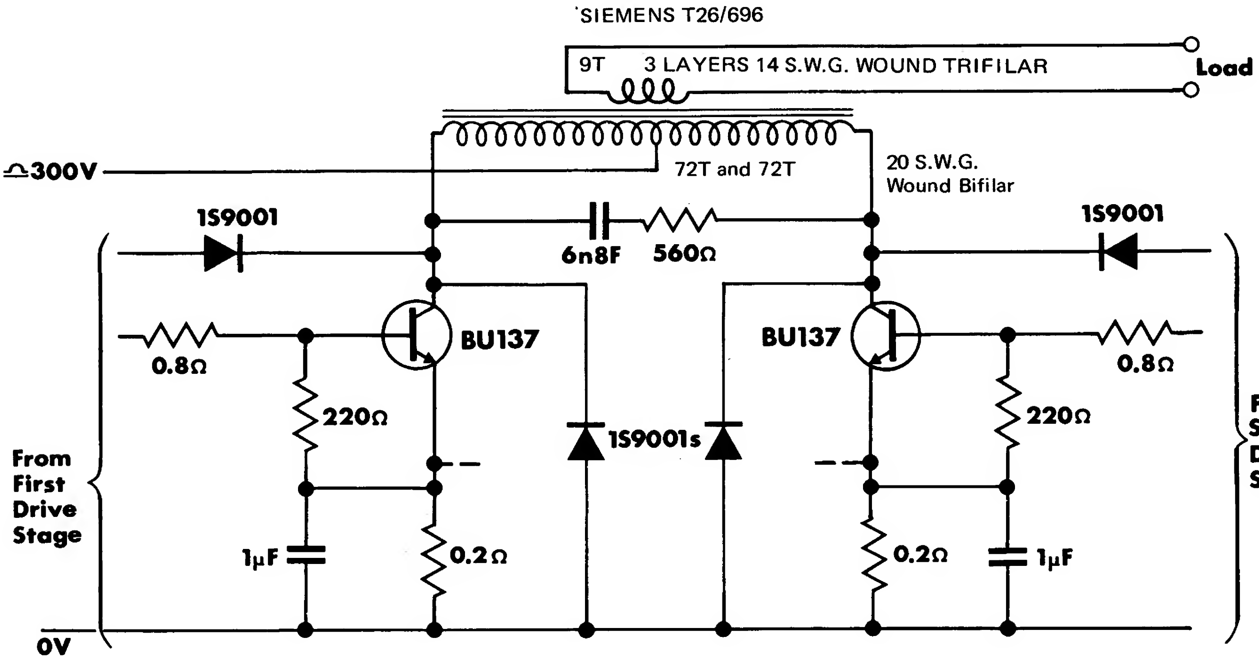

SIEMENS T26/696
9T 3 LAYERS 14 S.W.G. WOUND TRIFILAR
Load
≏300V
72T and 72T
20 S.W.G.
Wound Bifilar
1S9001
1S9001
6n8F
560Ω
BU137
BU137
0.8Ω
0.8Ω
220Ω
220Ω
1S9001s
From
First
Drive
Stage
From
Second
Drive
Stage
1μF
0.2Ω
0.2Ω
1μF
0V

FIGURE 39. Output and Isolating Stage

the tapping at about 1/3 up the winding so that the drive to the anode of the diode is about three times the drive to the base of the transistor. When the collector falls to below three times the base voltage level, the diode conducts reducing the level of base current. Thus an equilibrium is reached when the base current supplied to the transistor is just sufficient to keep its collector-emitter voltage V_{CE} equal to approximately twice the base voltage. Therefore when the transistor is turned 'off' there is relatively little stored charge in it and a fast turn 'off' time results. The 0.2Ω resistors in the emitters monitor the emitter current in the device and it is from this point that the current trip in the control section operates. The system is a push-pull one, using a central tapped transformer fed with rectified a.c. mains. As the inductive energy in the system is considerable, two 1S9001 diodes limit the collector's negative excursions while the positive spikes are damped by the 6n8F capacitor in series with the 560Ω resistor across the primary winding. With a turns ratio of approximately 8 to 1 the 7A in the primary is transformed into the required 40A output current from the secondary winding.

Circuits for deriving suitable voltage supplies fro the complete system are shown in Figure 40. The 300V rail is obtained from the a.c. supply by using a 10A bridge (1B100M60) and is protected by a 2Ω 50W surge limiting resistor and a 10A fuse. For most applications this rail can be unsmoothed as shown, although should a reasonably constant output voltage be necessary, then a high value, high voltage smoothing capacitor will be employed. A small 20V secondary mains transformer, bridge (1B20K10) and 5mF 30V electrolytic capacitor serve to provide the 26 and 5V rails. As only a small current is required from the 5V supply, as previously mentioned, the '723 i.c., with a TIP30 transistor to boost its output rating, can be used to accurately stabilize and regulate the 5V. In this type of system where heavy currents are flowing it is desirable to use a star earthing system where all the earth leads meet at a star point.

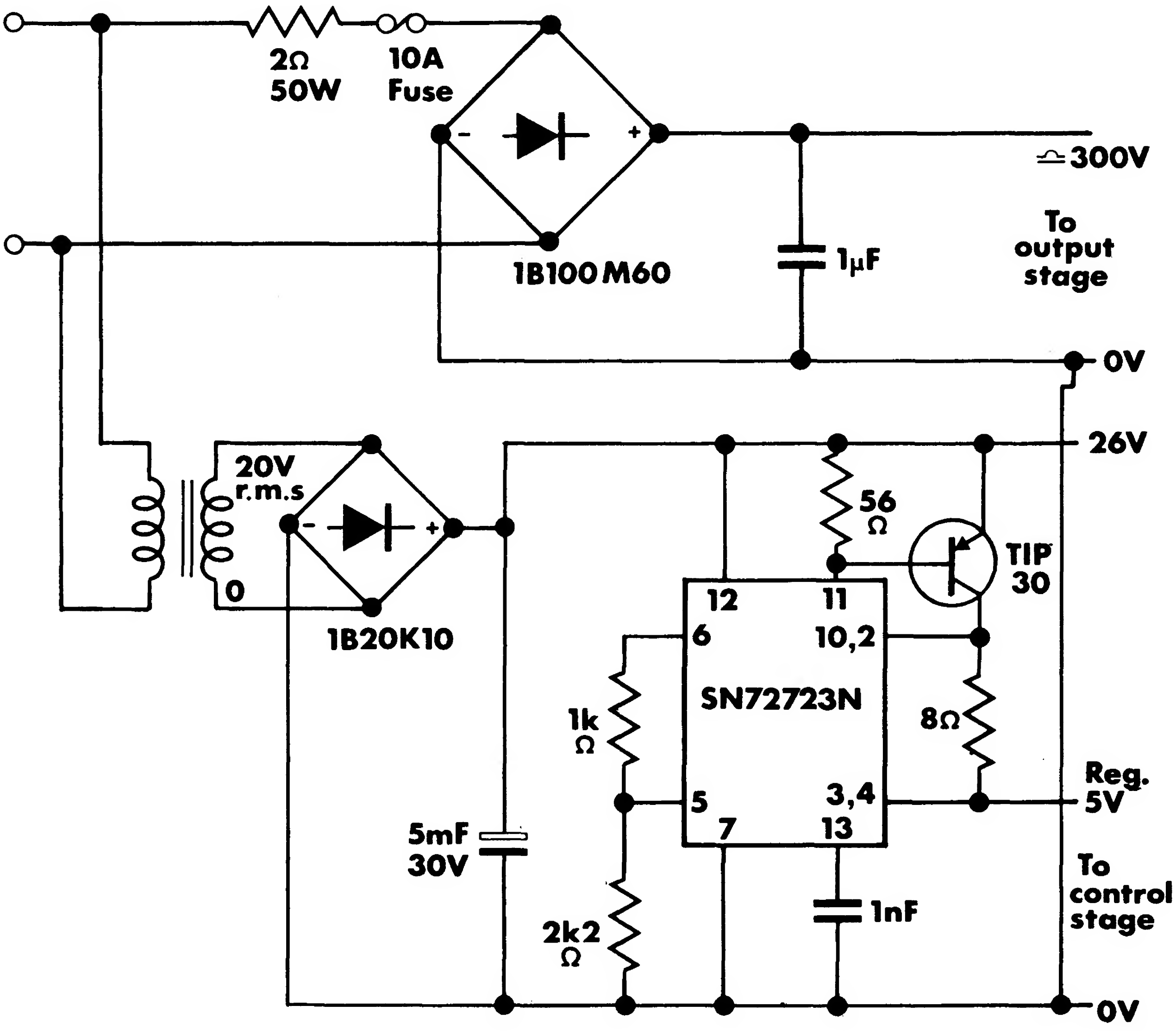


FIGURE 40. System Voltage Supply Circuits

REFERENCES

1,2,3 a) T. Roddam *'Transistor Inverters and Converters'* Iliffe Books Limited.

b) *'Semiconductor Circuit Design'* Volume 1 Texas Instruments Ltd., April '72 Chapter X for[1], pp. 91-94 for[2], and pp. 94-96, 115-117 etc. for [3].

4 Chapter III.

ACKNOWLEDGEMENT

I should like to thank Mick Maytum for the circuit designs and Gary Bentley who built up the practical circuits described in this chapter.

V SWITCHING MODE POWER SUPPLIES

by

Peter Wilson

The availability of reliable high voltage power transistors and control integrated circuits at an economical price allows the more complex switching mode power supply to be considered as an alternative to the conventional series regulator power supply. The major advantages of the switching mode supply, which also offset the complexity, are those listed for the 120W power supply unit described in the previous chapter, i.e. smaller size and weight, and higher efficiency. It will also regulate over a wide input voltage range and the choice of stabilised output voltage can easily be made by use of the appropriate number of transformer secondary turns. In the first part of this chapter a comprehensive power supply with two cascaded switching mode sections, which would be suitable for, say, a large (800W) computer 5V t.t.l. source, is built up stage by stage until the complete unit is assembled. Then in the second part a specific 'no frills' requirement is taken, that of a large screen colour television, and a worked example of the single power device approach is given, together with all its ramifications, for use as a design pattern.

CASCADED APPROACH

Mains Rectification Stage

The first stage, as shown in Figure 1, consists of a conventional bridge rectifier and smoothing capacitor. Depending on the loading and the mains supply itself the d.c. output will vary between approximately 220 and 380V. Provision of low tension (l.t.) supplies is provided by means of a small 5VA transformer, this being more efficient than providing them from the supply itself. For the sake of completeness the traditional l.t. supplies are shown in Figure 2.

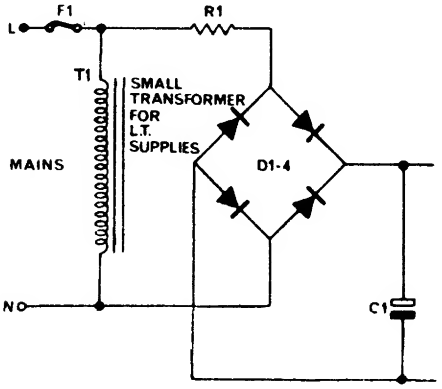


FIGURE 1. Conventional Mains Rectification

Shunt Chopper Stage

The 220 to 380V supply is stabilized into a regulated 220V by using the shunt chopper circuit, Figure 3, working at 20kHz. The BUY69B transistor, the inductor L1, the diode D5 and the capacitor C8 form the basic elements of the circuit. Note, that emitter resistor R3 and capacitor C3 are included to hold up the emitter potential during the switch 'off'—this transistor being a high voltage power device. Resistor R2 and capacitor C2 form a damping network, and resistor R5 provides feedback to the pulse width controller.

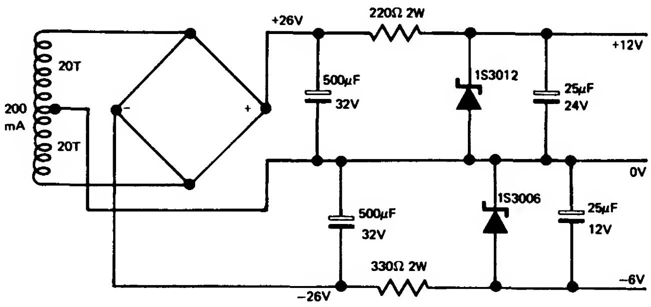


FIGURE 2. L. T. Power Supplies

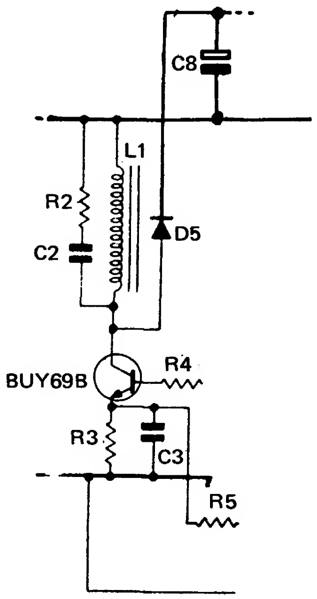


FIGURE 3. Shunt Chopper Circuit

D.C. to D.C. Converter Stage

Figure 4 shows the main stage of the supply, a two transformer d.c. to d.c. converter[1], working at 30kHz. (It is an inverter up until the secondary of transformer T3 and the addition of the diodes D7 and D8 and output filter C12, L2 and C13, make it a converter.) The timing is defined by the saturation of the driver transformer T4. A voltage waveform which switches from $V_{CE(sat)}$ to twice the supply voltage (400V) appears across the primary of the output transformer T3, and resistor R16 feeds back about half of this to the primary transformer T4. Components R19, C11 and D6 are present to ensure correct starting and resistor R17 and R18 regulate the base current to the transistor. Using high voltage BUY69C transistors means that emitter networks, R20 and C9, and R21 and C10 must be included for correct switching. From the output filter, the required 5V supply output is provided (for a large t.t.l. system). Although the system is basically complete, as yet there is no regulation.

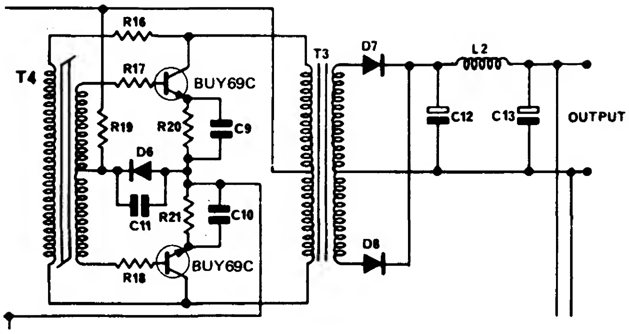


FIGURE 4. D.C. to D.C. Converter

Voltage Reference, Error Amplifier and Optoelectronic Link Stage

Figure 5 illustrates how an SN72723N voltage regulator i.c. is used to monitor the output and act as an error amplifier comparing the input fed to the INV terminal with the reference voltage set on the NI terminal.(Resistor R23 and R24 potentiably divide the internal V_{REF} level). The internal zener diode acts as a level shifter. Resistor R25 limits the amount of current into the diode of the optocoupler–an interconnecting but isolating device. The type of optocoupler used will depend on the isolation voltage required; i.e. the TIL111 gives 1·5kV isolation, the TIL114 2·5kV and the TIX109 5kV, and the value of resistor R25 must be chosen to suit the optocoupler employed.

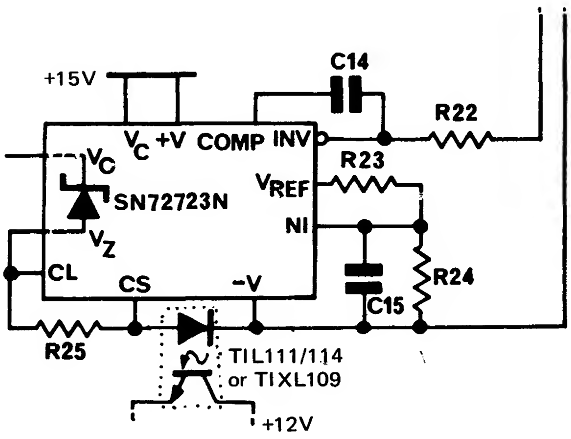


FIGURE 5. Voltage Reference and Opto Link Error Amplifier

Pulse Width Control Comparator and Oscillator Stage

The optocoupler output sets up the d.c. level on the inverting input of the pulse width control comparator (½ x SN72820), Figure 6. An equal mark space square wave is differentiated by resistor R11 and capacitor C6 and also fed to this point. On the positive spike the comparator switches over–regeneratively. It will either switch back on the negative spike, or depending on the emitter current ramp it is monitoring, it will switch back earlier and thus provides a pulse output whose width corresponds to the d.c. level, i.e. the error signal.

The equal mark space ratio square wave is obtained from the other half of the dual differential comparator SN72820 working as a 20kHz oscillator[2], Figure 7. (Positive feedback is applied by the potentiometer consisting of resistors R13 and R14, and the circuit time constant is given by C7, R12. Fine trim for an accurate 50:50 mark space ratio is achieved by having R15 as a potentiometer).

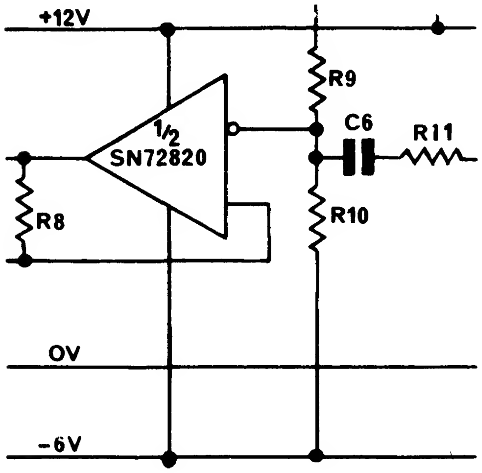


FIGURE 6. Pulse Width Control Comparator

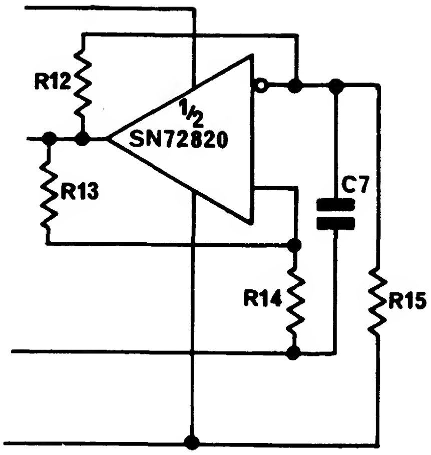


FIGURE 7. 20 kHz Oscillator

Driver Stage

All that is necessary now is the driver stage to raise the current output obtainable from the comparator up to the ≏2½A required base current of the shunt chopper transistor. It is achieved, as shown in Figure 8, by using a super silect BFR40 transistor as an emitter follower to drive the 300V 100mA BF259 transistor. This, in turn, has the step down 25:1 transformer T2 in its collector, providing from its secondary the ≏2½A needed.

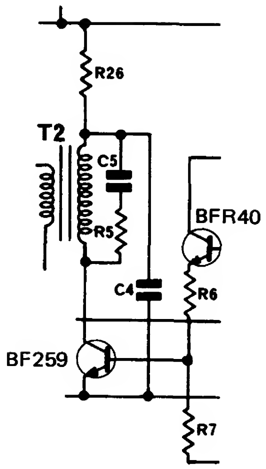


FIGURE 8. Driver Stage

Complete Switching Mode Power Supply

Thus in Figure 9 is shown the complete switching mode power supply which will supply 800W at an efficiency of ≏90% and be of physically small size. That the regulating system works correctly can be checked by assuming that the output goes high, say. Then the output of the optocoupler will fall, the comparator d.c. level will fall, its output pulse width is smaller, the emitter current ramps to a smaller value, and the chopper transistors 'on' time is reduced. Thus the 200V supply is reduced and the output from the inverter falls to compensate for the original increase.

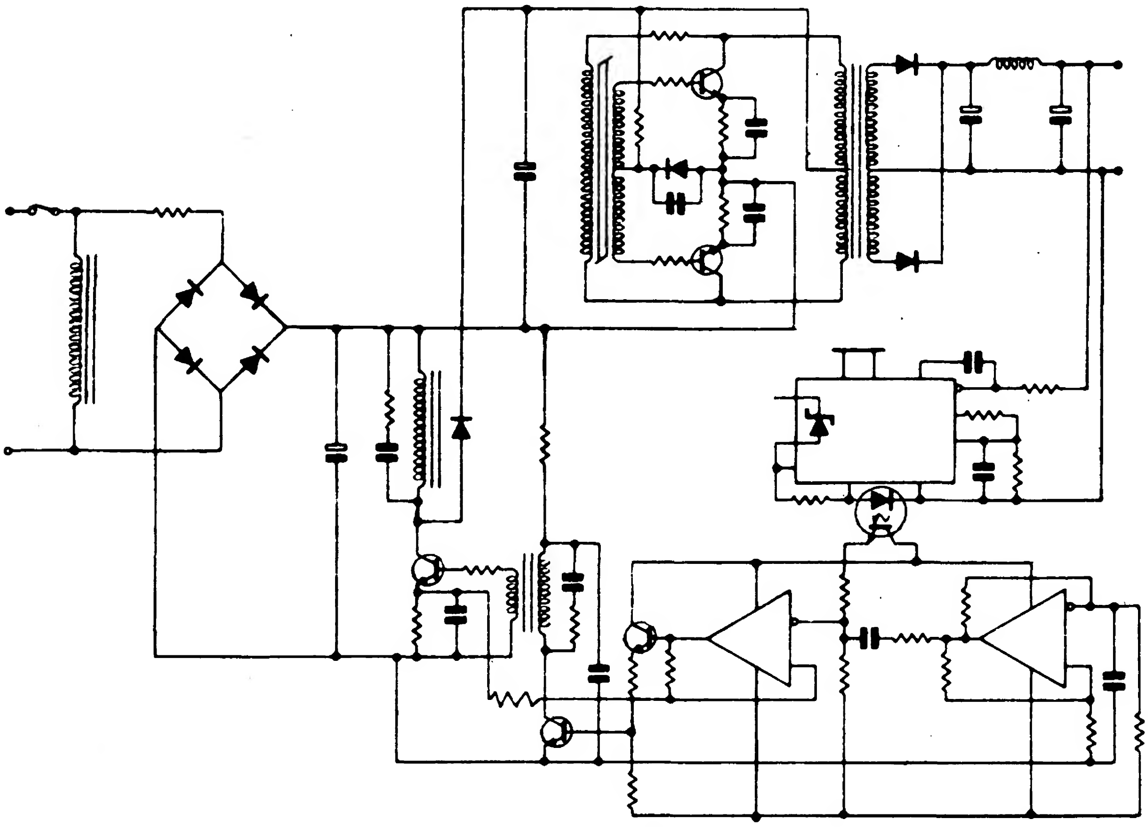


FIGURE 9. Complete Switching Mode Power Supply

DESIGN EXAMPLE (SINGLE POWER DEVICE APPROACH)

General

The power supply requirements for a 110° large screen colour television are shown in block diagram form in Figure 10. This illustrates the versatility of a switching mode supply in that several stabilized rails can be obtained, e.g. in order to drive the horizontal deflection coils a 90V supply is required, whilst the video driver stages require 220V. A stable 90V supply is necessary over wide input range (180 to 265V a.c.) in order that picture width variation should not be noticeable. Figure 11 is a block diagram of the proposed power supply. The unisolated section comprises of three blocks:

1. The output device which operating in a switched mode transfers energy from the rectified a.c. supply to the transformer during its conduction period. When the output device is switched 'off', stored energy is transferred to the regulated d.c. supplies, the amount of energy transferred in each cycle being dependent on the conduction time of the output device.
2. The driver stage which provides the required drive waveform to ensure safe and efficient operation of the output device.
3. The control circuit which compares the regulated supply voltage with a reference voltage, and provides to the drive stage a pulse width modulated output proportional to the voltage difference. The control circuit has additional features such as: controlled increase in pulse width on start up, and over current and over voltage protection for the output device.

The Output Transistor

The combination of input supply voltage, the desired operating frequency and the power requirement govern the choice of the power transistor. A BU126 transistor represents an economic solution, having a maximum collector emitter voltage rating, V_{CEX}, of 750V, and a maximum continuous collector current of 4A. The fast switching time of the device makes it suitable for operation at ultra-sonic frequency which, in turn, means that a small transformer core can be used. Typical switching waveforms for the transistor are shown in Figure 12. The device dissipation can be analysed in four parts:

a) Dissipation in the 'on' condition
b) Dissipation in the 'off' condition
c) Transient dissipation at device turn 'on'
d) Transient dissipation at device turn 'off'

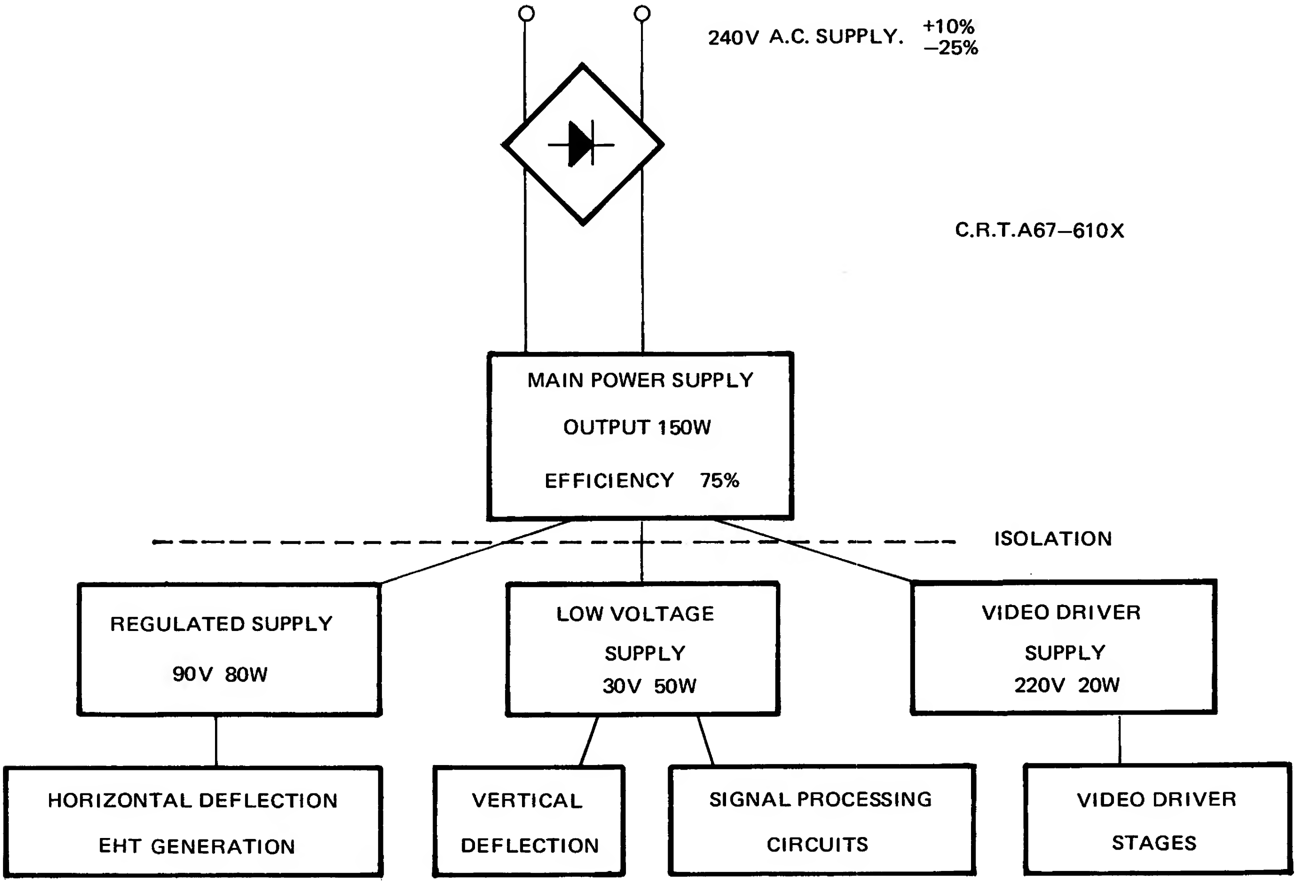

240V A.C. SUPPLY. +10% −25%
C.R.T.A67–610X
MAIN POWER SUPPLY
OUTPUT 150W
EFFICIENCY 75%
ISOLATION
REGULATED SUPPLY
90V 80W
LOW VOLTAGE
SUPPLY
30V 50W
VIDEO DRIVER
SUPPLY
220V 20W
HORIZONTAL DEFLECTION
EHT GENERATION
VERTICAL
DEFLECTION
SIGNAL PROCESSING
CIRCUITS
VIDEO DRIVER
STAGES

FIGURE 10. Block Diagram of Power Supply Requirements

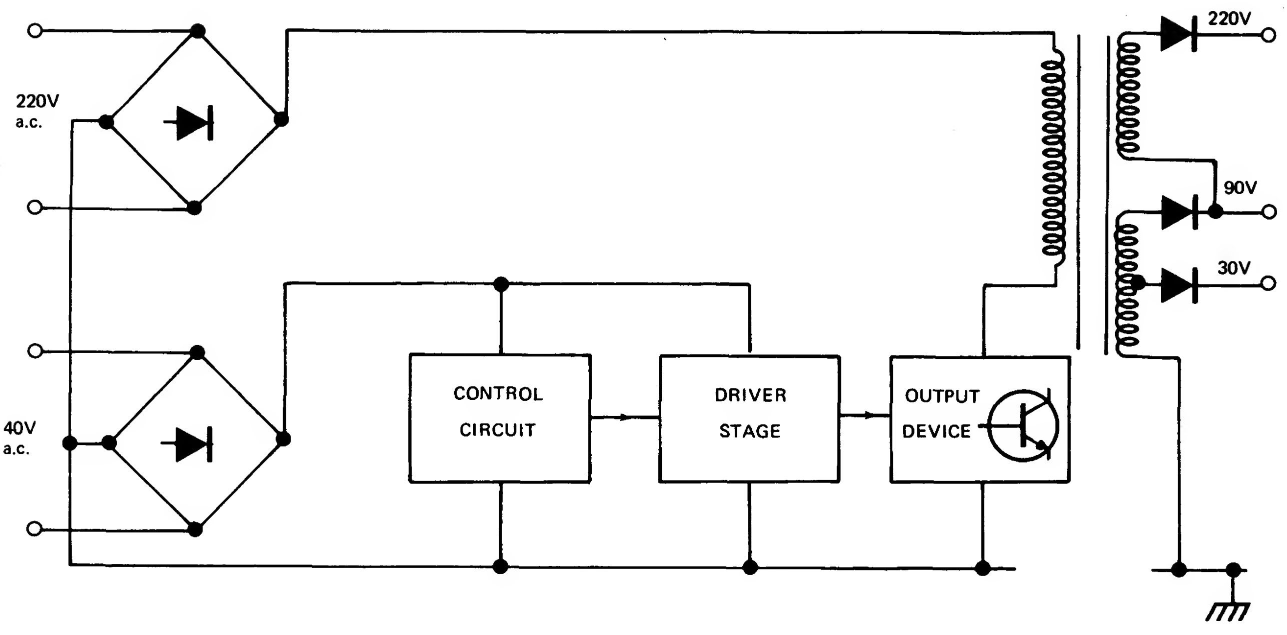


FIGURE 11. Power Supply Block Diagram

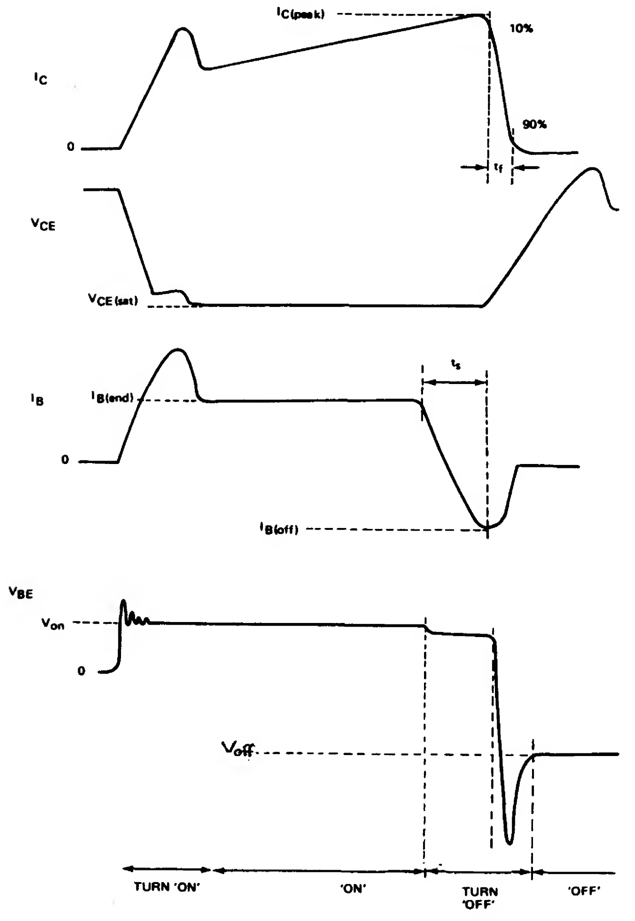


FIGURE 12. Typical Switching Waveforms of Output Transistor

Dissipation in the 'On' Condition: The device dissipation is minimised by ensuring that the base current is sufficient to maintain the transistor in saturation under worst case conditions, i.e. when the load on the supply is maximum and the a.c. supply voltage is low giving the highest peak collector current. Provided that the base current is sufficient for a device with the minimum specified gain in this condition, then the excess base current in other operating conditions can be tolerated.

Dissipation in the 'Off' Condition: The criterion here is to ensure that the maximum collector emitter voltage rating is not exceeded. A base emitter voltage of −1.5V, minimum applied in the 'off' condition ensures that maximum blocking is achieved. The worst case condition will occur at maximum a.c. supply input, and with high primary leakage inductance in the transformer, when a 'voltage clamp' circuit may be required to limit the peak voltage.

Transient Dissipation at Device Turn 'On': Dissipation is minimised by ensuring that the base current risetime is sufficiently fast to continually overdrive the device through the transitional period. This results in a fast rise in collector current. Overshoot on the collector current waveform is minimised by the use of fast rectifiers on the regulated supply rails. Dissipation is further reduced by providing overshoot on the base current waveform, as shown in Figure 12.

Transient Dissipation at Device Turn 'Off': Of the four categories listed, this is perhaps the most discussed. Optimised drive conditions tend to short collector current fall times, and efficient switching. However, drive conditions for the device cannot be kept at optimum in exactly the same way as, for instance, in horizontal deflection stages, since, as explained, the device will normally be overdriven in order that sufficient drive is applied in the worst case. Compensation for the resulting slower collector current fall times can be achieved by controlling the rate of rise of collector voltage in order to limit the turn 'off' dissipation.

The operating waveforms of the output transistor are shown in Figure 13 for normal a.c. supply voltage (240V) and in Figure 14 for low (180V) and high (265V) a.c. supply voltages. In all cases the operating frequency is 25kHz. Figure 15 shows typical collector emitter dissipation as measured on a multiplying oscilloscope – transient power dissipation at turn 'on' and turn 'off' are given on an expanded time scale. Figure 16 shows a typical variation in mean dissipation with a.c. supply voltage.

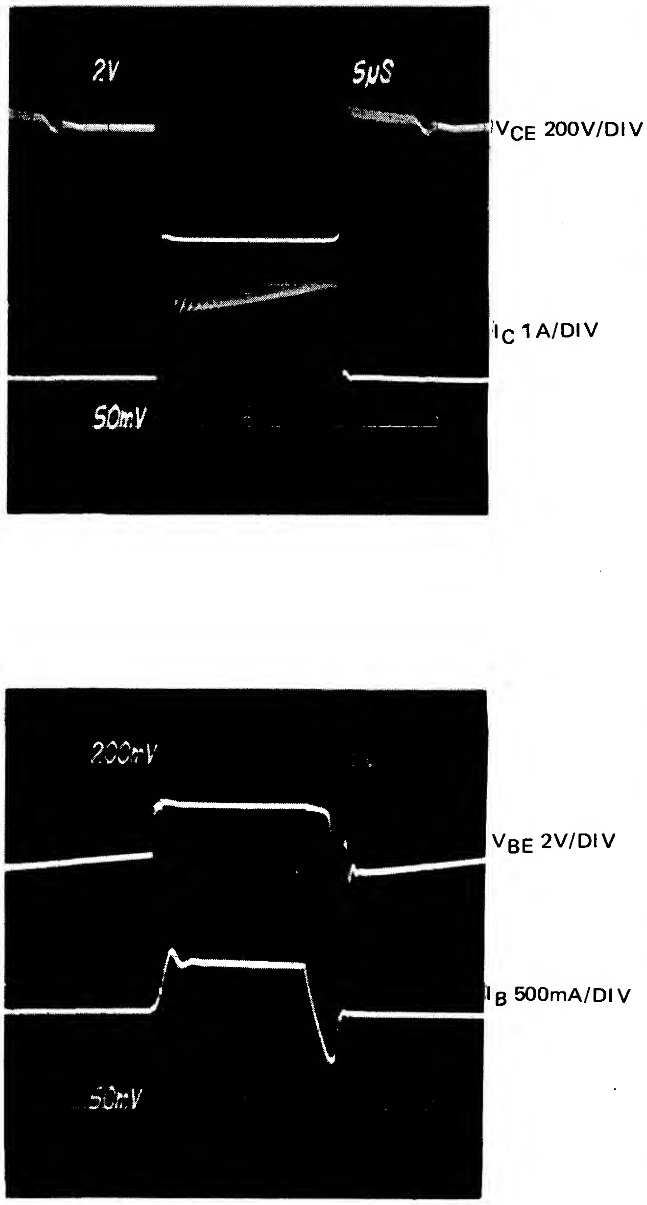


FIGURE 13. Output Transistor Operating Waveforms at Normal A.C. Supply Voltage

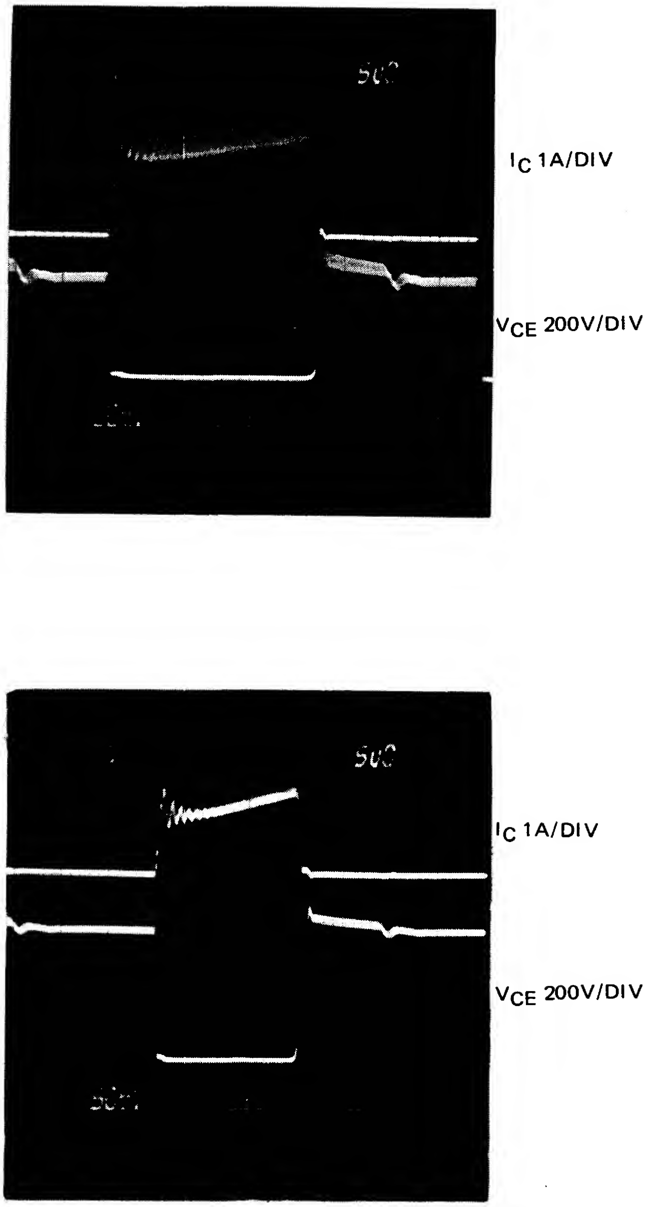


FIGURE 14. Output Transistor Operating Waveforms at Low and High A.C. Supply Voltages

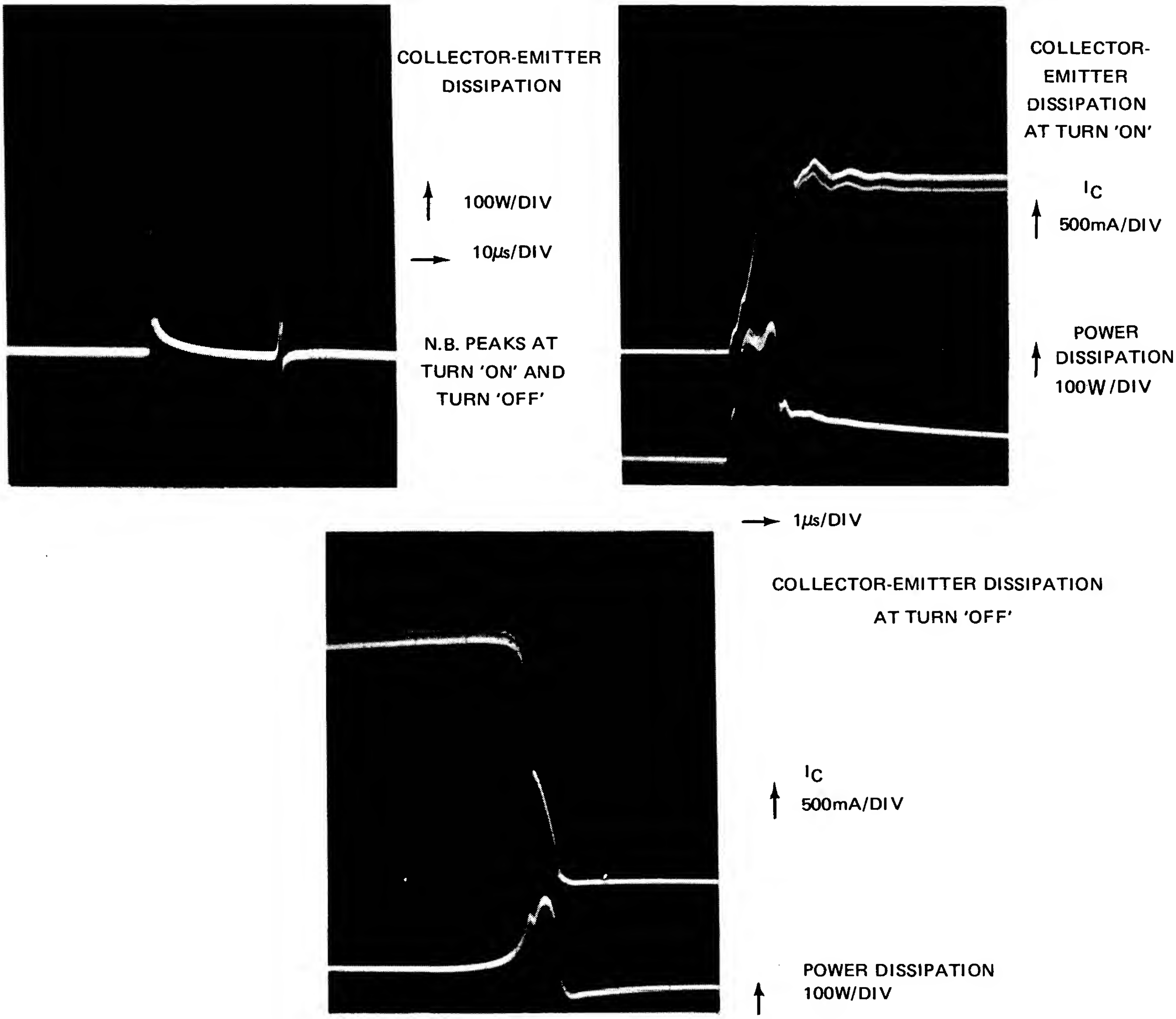


FIGURE 15. Output Transistor Typical Collector Emitter Dissipation

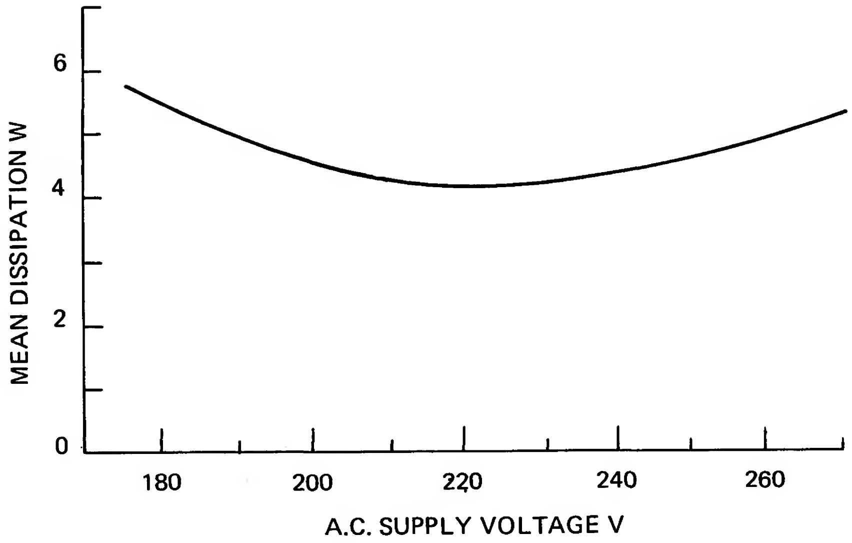


FIGURE 16. Variation in Mean Dissipation with A.C. Supply Voltage

The Driver Stage

The design of the driver stage must take into account circuit component and operating tolerances and the temperature dependance of transistor parameters, such as storage time. Figure 17 shows a circuit diagram of a suitable driver stage. In the 'on' condition driver transistor VT2 takes current from the supply through the primary of driver transformer T2. At turn 'off' the collector of transistor VT2 is clamped to the supply by diodes D1 and D2. Damping components C2, R2 prevent excessive ringing of the collector waveform. The energy stored in the transformer during the transistor conduction time is transferred to the secondary during the 'off' period. The components in transformer T2 secondary circuit, i.e. R3, C4 and the leakage inductance of the transformer shape the base current waveform of power transistor VT1.

Calculations: a) The secondary circuit:

The required $I_{B(end)}$ is 500mA for 2·5A peak I_C with a minimum device gain of 5 at V_{CE} = 5V. In order that $I_{B(end)}$ be independent of transistor parameters, resistor R3 is included. Assessment of the volt second area of the waveform shown in Figure 18, assuming a 1:1 mark space ratio, indicates equal positive and negative voltage swing on the secondary.

Taking $V_{off} = -3V$

$V_{on} = +3V$

The series resistor R3 $= (V_{on} - V_{BE})/I_{B(end)}$

$= 4\Omega$

assuming $V_{BE(sat)} = 1V$

The base emitter resistor, R4, suppresses transients picked up at the base terminal of transistor VT1, and must be mounted close to the device. Resistor R4 should not shunt more than 10% of the base current,i.e.

$R4 \geqslant V_{BE}/0.1\ I_{B(end)}$

$\geqslant 20\Omega$

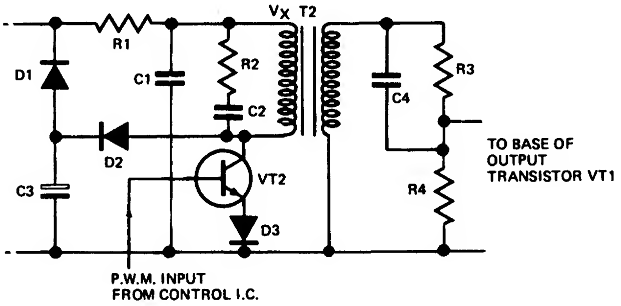
In practice a value of 100Ω for R4 provided sufficient damping. The transformer T2 secondary leakage inductance controls the rate of fall of base current at turn 'off' – this is tailored to the transistor drive requirements. For optimum drive, dI_B/dt at turn 'off' is 1·5A/μs.

Hence, $L_B = (V_{off} + V_{BE}) \times dt/dI_B$

$= 4/1{\cdot}5\mu H$

$= 2{\cdot}7\mu H$

Such a low value of leakage inductance is difficult to obtain in practice, but winding the secondary between halves of the primary minimises the value. Since, as mentioned in the power transistor section, the drive conditions are not always optimum the device normally being overdriven, a larger value of leakage inductance than the calculated value could be used. Although the correct solution, for fast switching, would be to increase V_{off}. Capacitor C4, bypassing resistor R3, provides overshoot on the base current waveform at turn 'on'. This helps to minimise transistor VT1 dissipation. Capacitor C4 also causes faster initial dI_B/dt at device turn 'off'.

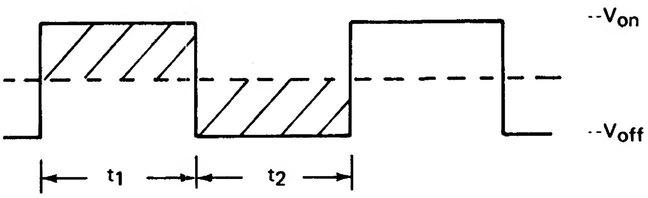

Vx
T2
R1
D1
C1
R2
C2
C4
R3
TO BASE OF OUTPUT TRANSISTOR VT1
D2
VT2
C3
R4
D3
P.W.M. INPUT FROM CONTROL I.C.

Components

R1	680Ω	C1	100nF	D1-3 1S921
R2	1k5Ω	C2	200pF	
R3	3Ω9	C3	10μF	
R4	100Ω	C4	1.5μF	VT2 BFR40

Transformer T2 Primary: 300 turns wound in two halves with the secondary sandwiched between them.
Inductance 35mH.
Secondary: 50 turns. Leakage inductance 2.7μH.
Core: F X 1238.

FIGURE 17. Driver Stage



$V_{on} \times t_1 = V_{off} \times t_2$ where period $\tau = t_1 + t_2$

FIGURE 18. Idealised Transformer T2 Secondary Voltage Waveforms

b) The primary circuit:

Driver transistor VT2 operates in antiphase with transistor VT1. This offers the advantage of active 'hold off' for VT1 both in normal running and start up conditions. The transformer turns ratio, n, determines the collector emitter voltage swing of VT2. Choosing n = 6

V_{CE} max. $= n(V_{on} + V_{off}) = 36V$

This voltage is fixed by capacitor C3 charged through diode D2. The voltage at the top end of the primary winding, V_X can be determined from the volt second area, Figure 19, to be 18V:

$$(V_{CE}\ \text{max.} - V_X) \times t_2 = (V_X - V_{CE(sat)}) \times t_1$$

For a 1:1 mark space ratio, $t_1 = t_2$

$$V_X = (V_{CE}\ \text{max.} + V_{CE(sat)})/2$$
$$\doteq 18\text{V}$$

An approximate value for the feed resistor R1 is given by:

$$R1 = (V_S - V_X) \times n/0.5 I_{B(end)}$$
$$= 890\Omega$$

In practice a lower value is used to compensate for circuit losses.

Capacitor C1 smoothes out high frequency ripple at the top end of the primary winding. The primary inductance of transformer T2 must be sufficiently high to prevent fall off in VT1 base current towards the end of its conduction time. High inductance also results in lower peak collector currents for VT2. The criterion for variation in I_B can be expressed:

$$L_p/n^2 \geqslant t_2 \times V_{on}/\Delta I_{B(end)}$$

where L_p/n^2 is the primary inductance referred to the secondary winding, t_2 is transistor VT1 conduction time, and $\Delta I_{B(end)}$ is the allowable variation in I_B.

$$L_p \geqslant 2{\cdot}16/\Delta I_{B(end)}\ \text{mH/A}$$

A primary inductance Lp = 35mH allows 12·3% variation in I_B, which is acceptable. The resulting peak collector current of transistor VT2 is 80mA, c.f. the initial current peak of 220mA which occurs as stored charge is removed from transistor VT1.

Initial current peak $\doteq I_{B(off)}/n$

Components C2, R2 across the primary of T2 are damping components which control the amount of overshoot on transistor VT1 base current and also on VT2 collector voltage.

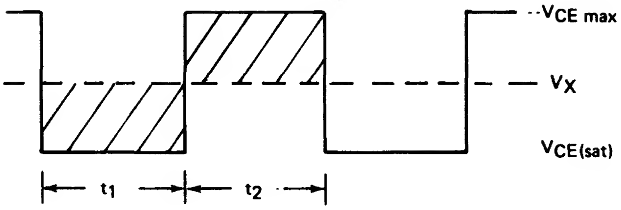


FIGURE 19. Idealised Transformer T2 Primary Voltage Waveforms

The Control Circuit

Integrated circuits have been developed specifically for the purpose of monitoring the output voltage and changing the mark space ratio to counteract any variation. An example of such an i.c. is the SN76548 designed for use with an external oscillator, such as the horizontal oscillator in a T.V. set (15·625kHz). This circuit has the following features:

a) An error amplifier to compare the regulated supply with a reference voltage.

b) A pulse width modulator circuit with output amplifier (open collector) and controlled pulse width at start up.

c) An internal temperature compensated reference voltage and self stabilised supply (i.e. it can be operated from an unregulated supply).

d) Over voltage and over current protection.

Another i.c. which can also perform the control function is the SN76549 which has the basic features of the SN76548, but includes in addition:

a) An internal oscillator, the frequency of which is fixed by external components, and which can be phase locked to an external signal.

b) A permanent cut out which shuts down the power supply after a preset number of operations of the trip circuits.

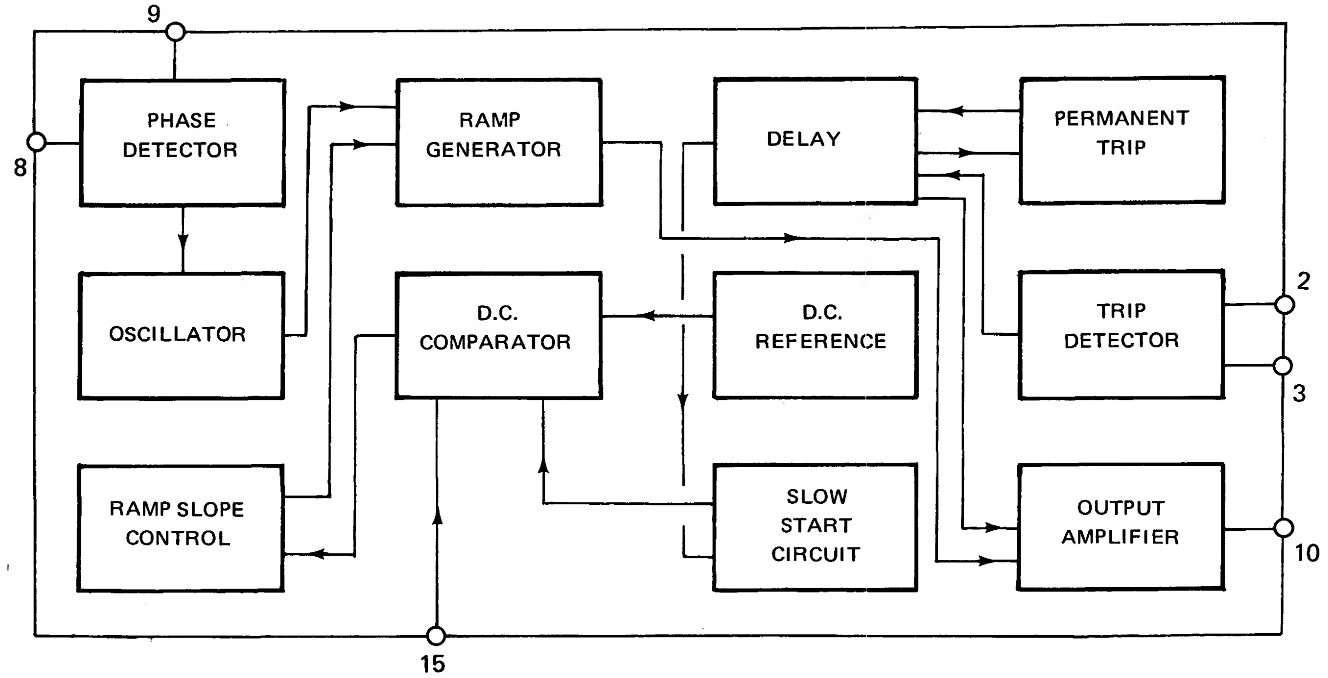

9
8
PHASE DETECTOR
RAMP GENERATOR
DELAY
PERMANENT TRIP
OSCILLATOR
D.C. COMPARATOR
D.C. REFERENCE
TRIP DETECTOR
2
3
RAMP SLOPE CONTROL
SLOW START CIRCUIT
OUTPUT AMPLIFIER
10
15

FIGURE 20. Control I.C. SN76549 Block Diagram

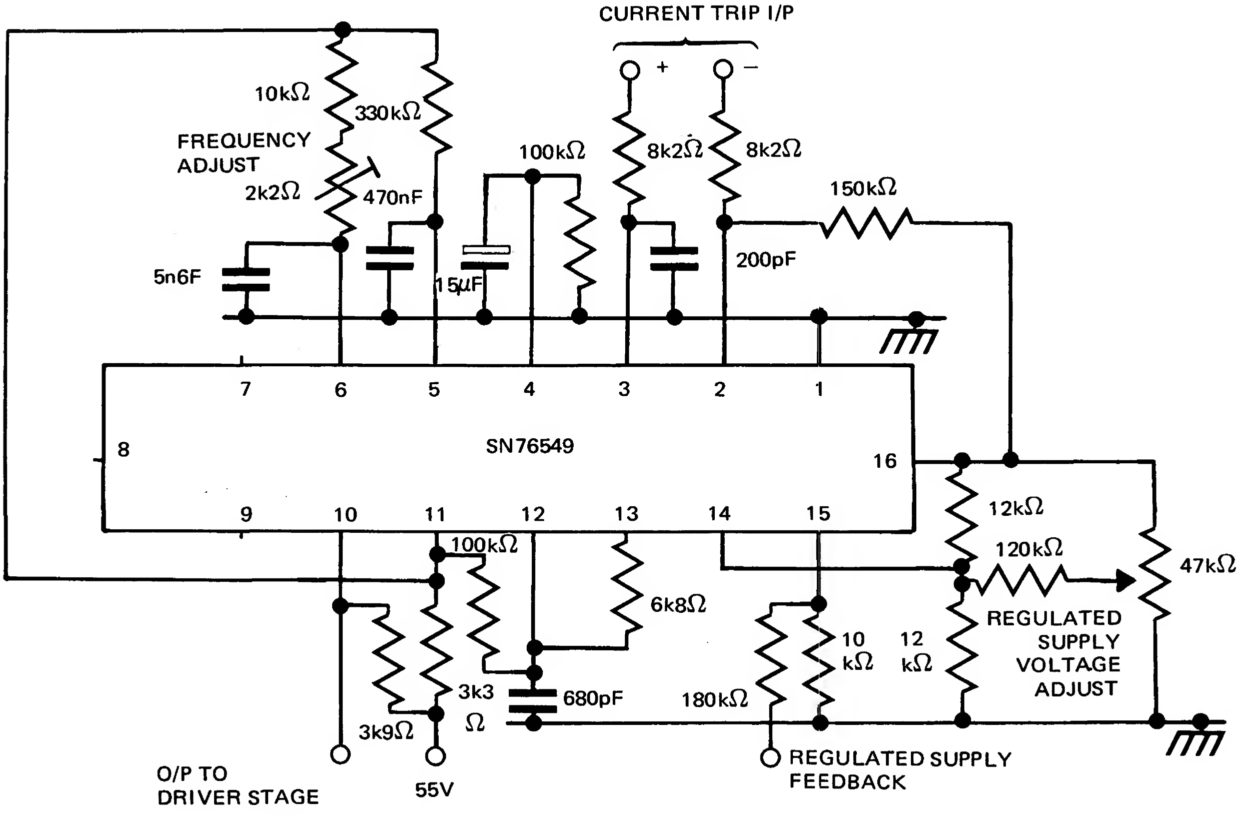

CURRENT TRIP I/P
+
−
10kΩ
330kΩ
FREQUENCY ADJUST
2k2Ω
470nF
100kΩ
8k2Ω
8k2Ω
150kΩ
5n6F
1 5μF
200pF
7
6
5
4
3
2
1
8
SN76549
16
9
10
11
12
13
14
15
12kΩ
120kΩ
47kΩ
100kΩ
6k8Ω
10 kΩ
12 kΩ
REGULATED SUPPLY VOLTAGE ADJUST
3k3 Ω
680pF
180kΩ
3k9Ω
O/P TO DRIVER STAGE
55V
REGULATED SUPPLY FEEDBACK

FIGURE 21. Control Circuit for the 25kHz Switched Mode Supply

Figure 20 gives a block diagram of the SN76549 and Figure 21 shows the circuit details for employing it as the control section of the switched mode supply operating at 25kHz.

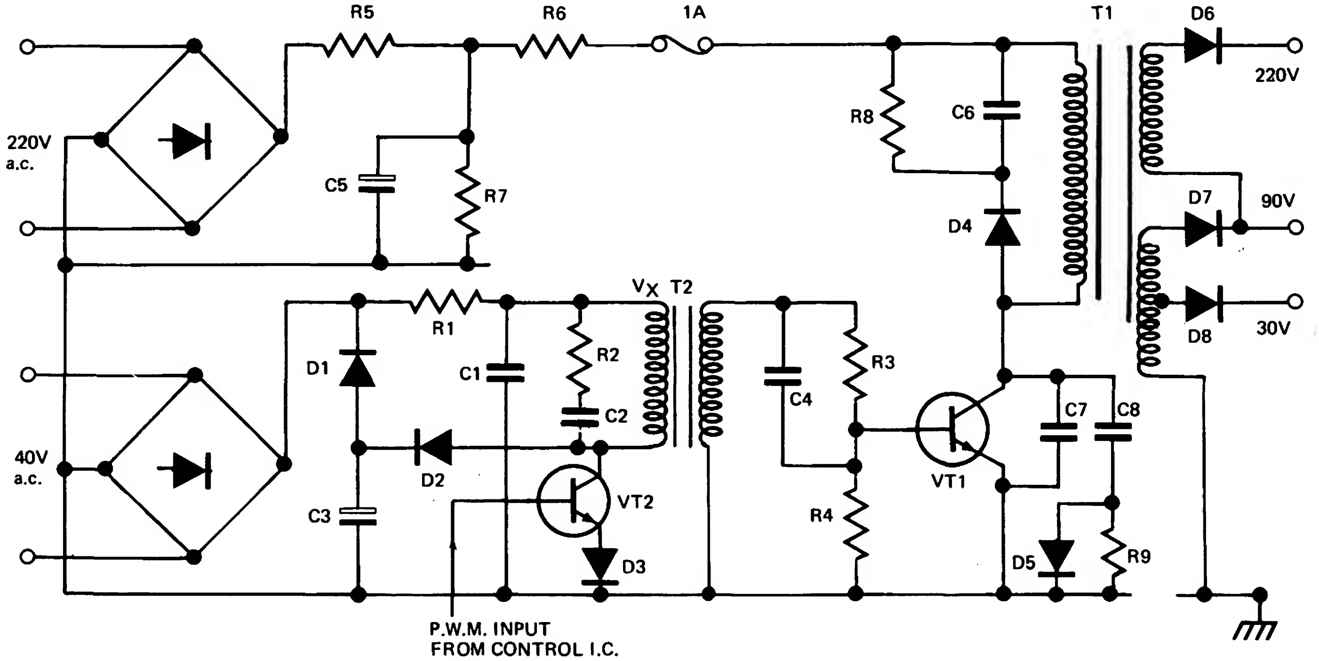
The Complete Circuit

The circuit diagram of the complete power supply (minus control section) is given in Figure 22. As shown it comprises of bridge rectifiers, the driver stage, the output device, the switched mode transformer T1 and associated rectifiers. The network across the collector emitter of the transistor VT1 controls the rate of rise of collector voltage at device switch 'off' in order to limit device dissipation. As the voltage rises, capacitor C8 charges through diode D5 and controls the rate of rise of voltage. When the rectifiers on the secondaries of transformer T1 start conducting, the voltage stops rising and the capacitor discharges through resistor R9 and continues to discharge during the following transistor conduction period. The second protection network, comprising diode D4, resistor R8 and capacitor C6 across the primary of transformer T1, is a voltage clamp circuit used to prevent the V_{CEX} rating of transistor VT1 being exceeded. Diode D4 should only conduct for a short period prior to conduction of the rectifiers on the secondaries, and consequently can be a low current type (e.g. BA248). The rectifiers on the secondary windings of transformer T1 are fast, soft recovery types with ratings to suit the application. The soft recovery characteristic reduces radiation at diode switch off. A detailed design of transformer T1 is given in the appendix.

Performance: The stability of the 90V supply was achieved to 2% over the specified input voltage range (180 to 265 Vac) and under full load conditions, 100Hz and 25kHz ripple on the 90V supply was of the order IV pk-pk at the nominal input voltage.

REFERENCES

1. M. J. Maytum and A. Lear, 'Driver Circuit Design Considerations for High Voltage Line Scan Transistors'; *IEEE Transactions,* Vol BTR-19, No. 2, May 1973.
2. *'Semiconductor Circuit Design';* Vol I, Chapter X, pp 83-128, April 1972.
3. Siferrit and Sirufer Material, *Transformers and Storage Units Data Book,* Siemens Aktiengesellschaft, 1969/70.



Drive Stage Components as Figure 17

C5	220µF	D4-D6	BA248	T1	As Text	R5	6Ω
C6	100nF	D7	BYW11-400	VT1	BU126	R6	10Ω 15W
C7	470pF	D8	BYW11-100			R7	330kΩ
C8	2n2F					R8	10kΩ
						R9	1k2Ω

FIGURE 22. Circuit Diagram of a Power Supply

APPENDIX

Design of the Transformer, T1

Specification: The load requirements on the secondary windings are as follows:

90V at 80W (0·9A)
30V at 50W (1·7A)
220V at 20W (0·1A)

A requirement for full isolation between primary and secondary windings has been assumed and led to the choice of a Siemens E55 ferrite core, type B66251 – A0000 – R026.

List of Symbols:

Symbol		Unit
B	Magnetic flux density	mT
H	Magnetic field strength	A/m
Φ	Magnetic flux	Wb
I	Magnetising current	A
μ_o	Permeability of free space $4\pi . 10^{-7}$	H/m
μ_r	Relative permeability	
Np	Number of primary turns	
A	Magnetic cross sectional area of the core	mm^2
l_e	Magnetic path length in the core	mm
V_e	Magnetic volume of the core	mm^3
l_g	Total length of air gap	mm
V_g	Volume of air gap	mm^3
L	Total magnetic path length	mm
P_o	Output power	W
τ	Period of the switching waveforms	μs

Transformer Dissipation:

Exposed core surface area	$7{\cdot}73 \times 10^3$ mm^2
Exposed winding surface area	$5{\cdot}90 \times 10^3$ mm^2
(Calculated from core and former dimensions)	

A figure of 300μW/mm^2 is assumed as the dissipation from a transformer operating at 40°C above ambient temperature.

So, the total power loss

= Exposed surface area (mm^2) x 300μW

= 4·1W

Assuming equal power loss from the core and the windings,

Core power loss $\hat{=}$ 2·05W

Working Flux Density:

Core loss/unit volume

= Total core power loss/core volume

= 48μW/mm^3

Tables for the core working at 25kHz and a temperature of 100°C show that:

Peak flux density, $\hat{B}$ = 100mT at 81μW/mm^3

As the core losses will be mainly due to hysteresis,

$\hat{B} \propto (\text{power loss})^{\frac{1}{2}}$ and so the peak working flux density,

$$\hat{B} = (48/81)^{\frac{1}{2}} \times 100\text{mT}$$
$$= 77\text{mT}$$

The Number of Primary Turns: Applying the fundamental magnetic relationship,

the applied voltage $V = Np \times A \times dB/dt$

gives $Np = V \times t/(2 \times \hat{B} \times A)$ 1

where t is the conduction time of the output transistor.

The worst case volt second product, V x t, occurs at high input voltage. From Figure 23,

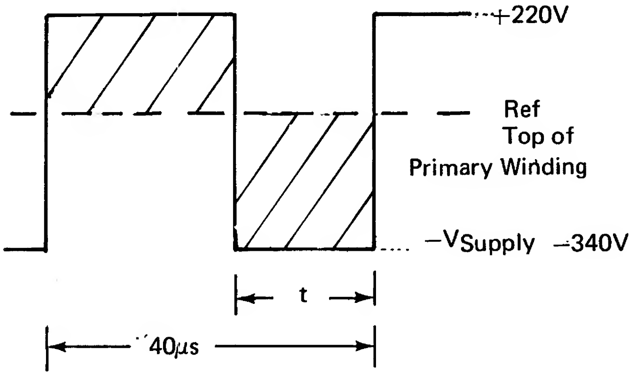


FIGURE 23. Idealised Transformer T1 Primary Voltage Waveforms

$$t \times 340 = (40 - t) \times 220$$
$$\therefore t = 110/7\mu s$$
$$V \times t = 110 \times 340 \times 10^{-6}/7 = 5{\cdot}2\text{mVs}$$
$$\therefore Np = 5{\cdot}2 \times 10^{-3}/2 \times 77 \times 10^{-3} \times 3{\cdot}54 \times 10^{-4}$$
$$= 96 \text{ turns}$$

The Air Gap: Manipulation of the formulae,

$B \doteqdot \mu_o\mu_r H$ and $H = NI/L$

gives:

$$\text{Magnetising current } I = 2 \times \hat{B} \times L/(\mu_o \times \mu_r \times Np)$$
$$= 2 \times \hat{B} \times (l_g + l_e/\mu_r)/(\mu_o \times Np)$$

...... 2

when an air gap is introduced into the magnetic circuit.

$$\text{The primary inductance } L_p = N_p \times d\Phi/dI$$
$$= N_p \times A \times dB/dI$$

since the total flux $\Phi = B \times A$

Substituting for dB/dI from equation (2) gives:

$$L_p = N_p \times A \times \mu_o \times N_p/(l_g + l_e/\mu_r)$$
$$= A \times \mu_o \times N_p^2/(l_g + l_e/\mu_r) \quad \ldots\ldots\ldots\ldots 3$$

For a large gap, $l_g > l_e/\mu_r$

$l_g > 54\mu m$

Taking l_g = 0·5mm results in L_p = 8·2mH on substitution into equation 3. This coincides with an A_L value (=L_p/N_p^2) of 890nH for approximately 0·5mm air gap from the core data.

Winding Design: The winding details are given in Table 1. The total winding area = 238mm^2. Allowing for isolation between windings and 4mm clearance at either end of the winding, the reduced winding area = 158mm^2.

Table 1 — Winding Details

	Primary	Secondaries		
		30V	90V	220V
Number of turns	96 2.29V/turn	14	40 total 26 on top of 30V supply	56 on top of 90V supply
Mean current A	0·7 includes allowance for inefficiency	2·7	1·0	0·1
S.W.G.	22	18 ≡3 strands of 22	22	34

N.B. The wire gauge is calculated assuming a maximum current density of 2·2A/mm^2.

A further reduction for the packing factor of the enamelled copper wire used gives; the effective winding area = 79mm^2.

The area is divided in proportion to the power loading on the windings. Details are given in Table 2.

Table 2 — Winding Area Division

	Load on the Winding W	Winding Area Available mm^2	Winding Area Used (details from Table 1) mm^2
Primary		39.5	38.4
30V 90V 220V	81 60 13	20.8 15.4 3.3	16.8 10.4 2.3
TOTAL	154	79.0	67.9

Thus the winding area of the core is adequate when allowance is made for isolation.

The primary winding can be sectionalized to give a worthwhile reduction in leakage inductance. This is done in proportion to the secondary winding loads. In this example the primary can be conveniently wound in two equal parts, as shown in Figure 24.

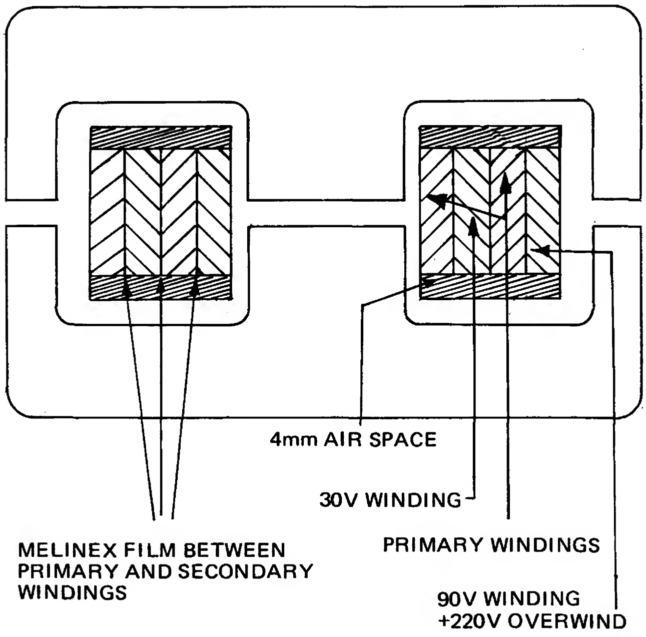

4mm AIR SPACE
30V WINDING
MELINEX FILM BETWEEN PRIMARY AND SECONDARY WINDINGS
PRIMARY WINDINGS
90V WINDING +220V OVERWIND

FIGURE 24. Switched Mode Transformer Winding Detail

VI TOUCH SWITCH POWER CONTROL

by

Jurek Budek

Mechanical switches, with their obvious disadvantages, are gradually being replaced by the more effective solid state devices. Of course, complete elimination of mechanical switching cannot occur when the requirement is for their high electrical isolation and power switching capability which solid state devices cannot provide. A touch switch control is a further step into solid state switching. With the help of interface circuitry, the power can be controlled by a simple touch. Lift control, selection of the television channels, and light control are typical examples of products already in use. By removing mechanical switching the reliability is improved and noise free operation obtained. Two types of touch switch are discussed – one is based on a f.e.t. technique and the other employing i.c.s. of the kind used in television. As touch switches circuits need only very small currents, milliamps, the inter-connections become very simple and the flexibility greater. An application where this is particularly useful is in conjunction with low voltage wiring systems. In these the idea is to eliminate the need to use power cabling to switches and to replace it by low voltage flat tape conductors and a centralised triac controlled distribution system. In repeat buildings, trunking, conduits and heavy cables can be eliminated and replaced by low voltage low current cables. Wiring is easier in confined spaces such as, for example, a hotel bedhead control which at present can contain a 'birds nest' of heavy cables. Since all switch wiring is done at low voltage there is less likelihood of electric shock, a point of particular importance in local authorities' schemes, old folks homes, hospitals and schools.

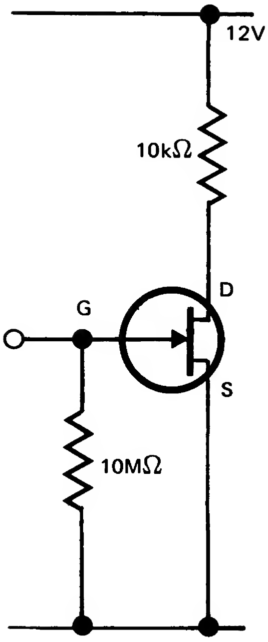


FIGURE 1. F. E. T. Circuit

USING FIELD EFFECT TRANSISTORS

General

If the drain of a field effect transistor[1] (f.e.t.) is connected to a 12V positive supply via a 10kΩ resistor, the source is to the negative, and there is a 10MΩ resistor between the gate and the negative, as shown in Figure 1, then, as the gate terminal is touched, 50Hz pick up volts will raise the drain potential, as shown in Figure 2. The drain voltage is normally 'low' at no gate volts and will go 'high' when the negative potential is applied to the gate. The 10MΩ resistor between the gate and the source maintains stable operation and by varying this value the sensitivity of operation can be controlled, i.e. the lower the value, the less sensitive becomes the device. Operation through 20-40 thou. thick plastic material can be achieved if required.

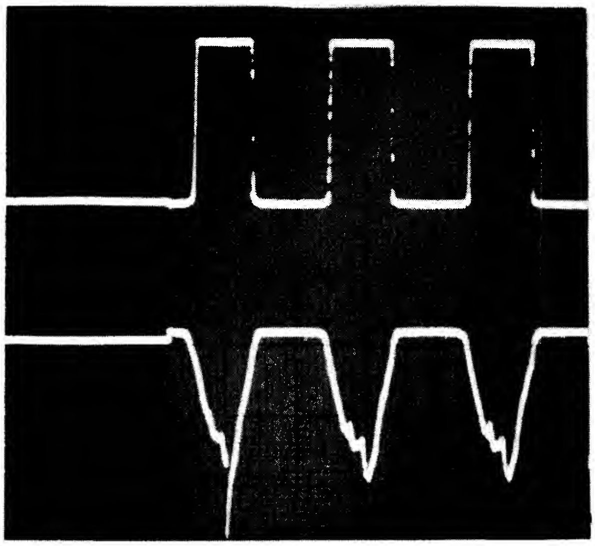


FIGURE 2. 'Pick-Up' Voltage Waveform

Touch Switch Circuit

Using the properties described above, the touch switch circuit shown in Figure 3 was designed. By touching the left hand (l.h.) plate, the drain of the f.e.t. will go 'high' turning 'on' thyristor Th1. Capacitor C1 will charge such that point A becomes negative and point B positive. On touching the right hand (r.h.) plate, thyristor Th2 will turn 'on', discharging capacitor C1, reverse biasing thyristor Th1 and thus turning it 'off'. Capacitor C1 then will reverse its polarity with point A now positive and point B negative. This operation is repeated each time the plates are touched in this sequence. Switching 'on' thyristor Th2 will energise the reed relay, RR, whose contacts are able to turn 'on' a triac, thyristor or anything else required within its current rating. The reed relay is used here to provide isolation – alternatively an optocoupler device could be employed. The gates of TIC44 thyristors are fairly sensitive requiring only a maximum of 200μA. Capacitors C2 and C3 prevent accidental triggering of the thyristors. The TIL209 light emitting diode (l.e.d.) will be lit when the reed relay is de-energised. (In a light control circuit this would be when the light is 'off' and thus would help to locate the switch in the dark).

The circuit shown in Figure 3 can be extended to operate from three touch plates the control, for example, a light to full or half brightness, as shown in Figure 4. The operation of this circuit is similar to that of Figure 3. Only one thyristor can be energised at a time.

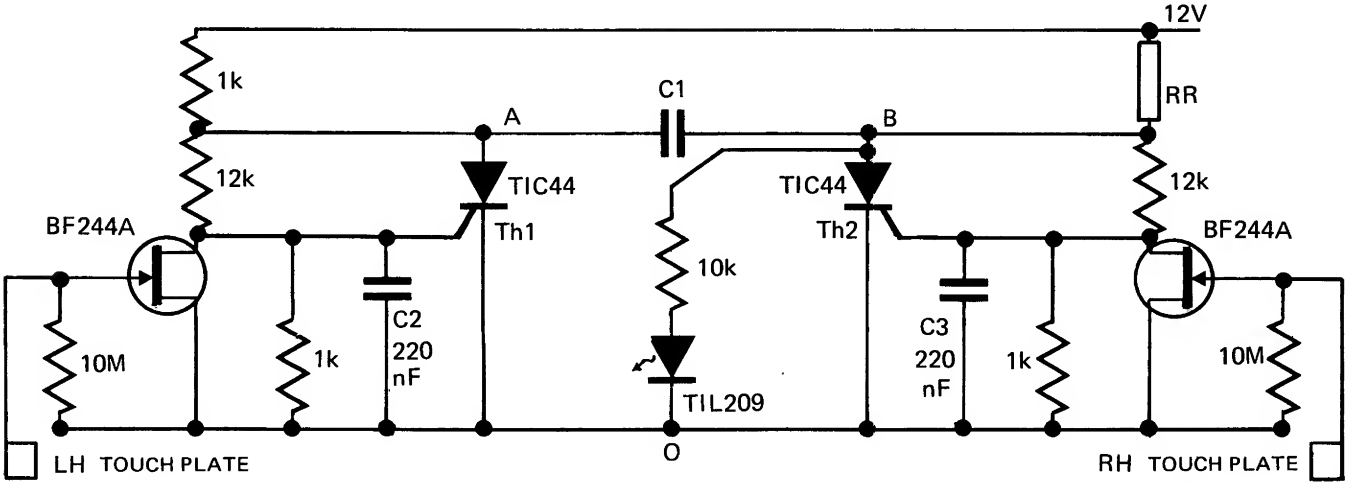

12V
1k
C1
A
B
RR
12k
TIC44
TIC44
12k
Th1
Th2
BF244A
BF244A
10k
C2
220
nF
C3
220
nF
10M
1k
1k
10M
TIL209
0
LH TOUCH PLATE
RH TOUCH PLATE

FIGURE 3. Basic F. E. T. Touch Switch

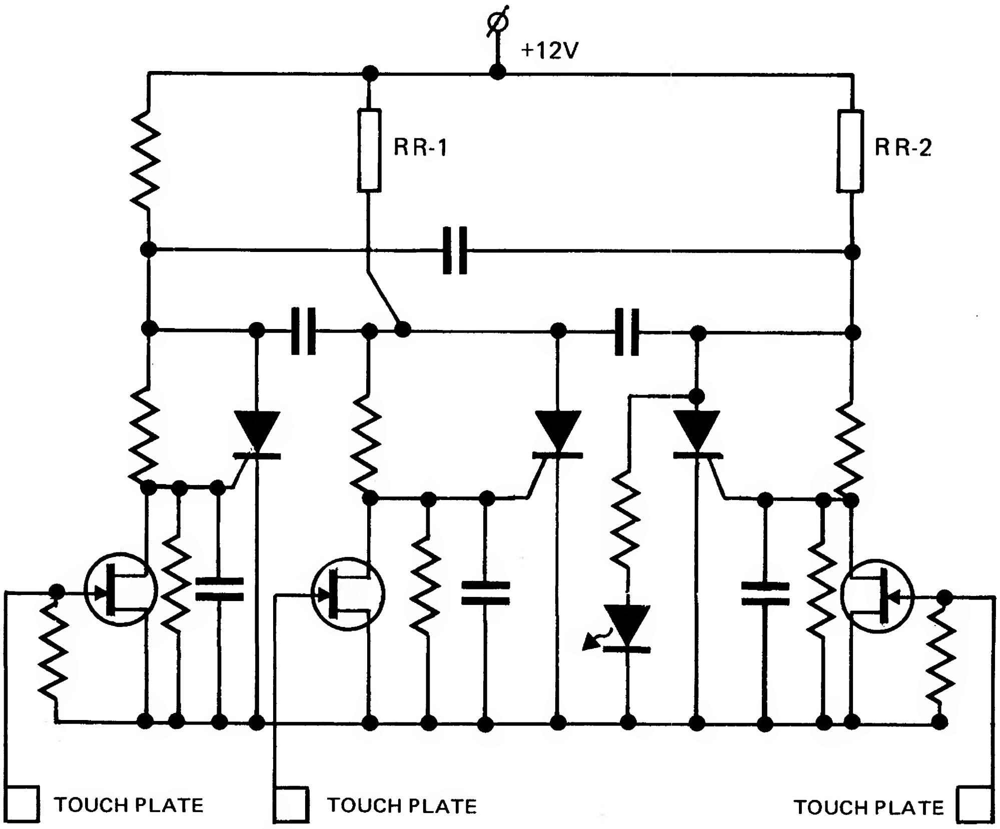

+12V
RR-1
RR-2
TOUCH PLATE
TOUCH PLATE
TOUCH PLATE

FIGURE 4. 12V Touch Switch with Three Touch Plates

A Low Voltage System with Touch Switches

A complete low voltage wiring system using the touch switch circuit(s) is shown in Figure 5. The system can be divided into two sections; the distribution box containing the power supply, reed relay(s), and power switching device(s); and the touch switch(es) which can be placed in various locations remote from the box. If the touch circuit is operated the reed relay RLA will be switched 'on' and, via contact RLA-1 and 470Ω resistor, will operate is associate triac thus switching 'on' the load, e.g. a lamp.[2] The interconnections between touch switches and box can be protected against accidential short circuits by limiting the fault current, either by including the 1kΩ resistor(s) or by the reed relay(s). Touch switches can be paralleled without additional circuitry, to control the same load. On switching on the a.c. supply, the load(s) will be in an 'off' state as no thyristors are turned 'on' and thus the reed relay(s) is de-energised.

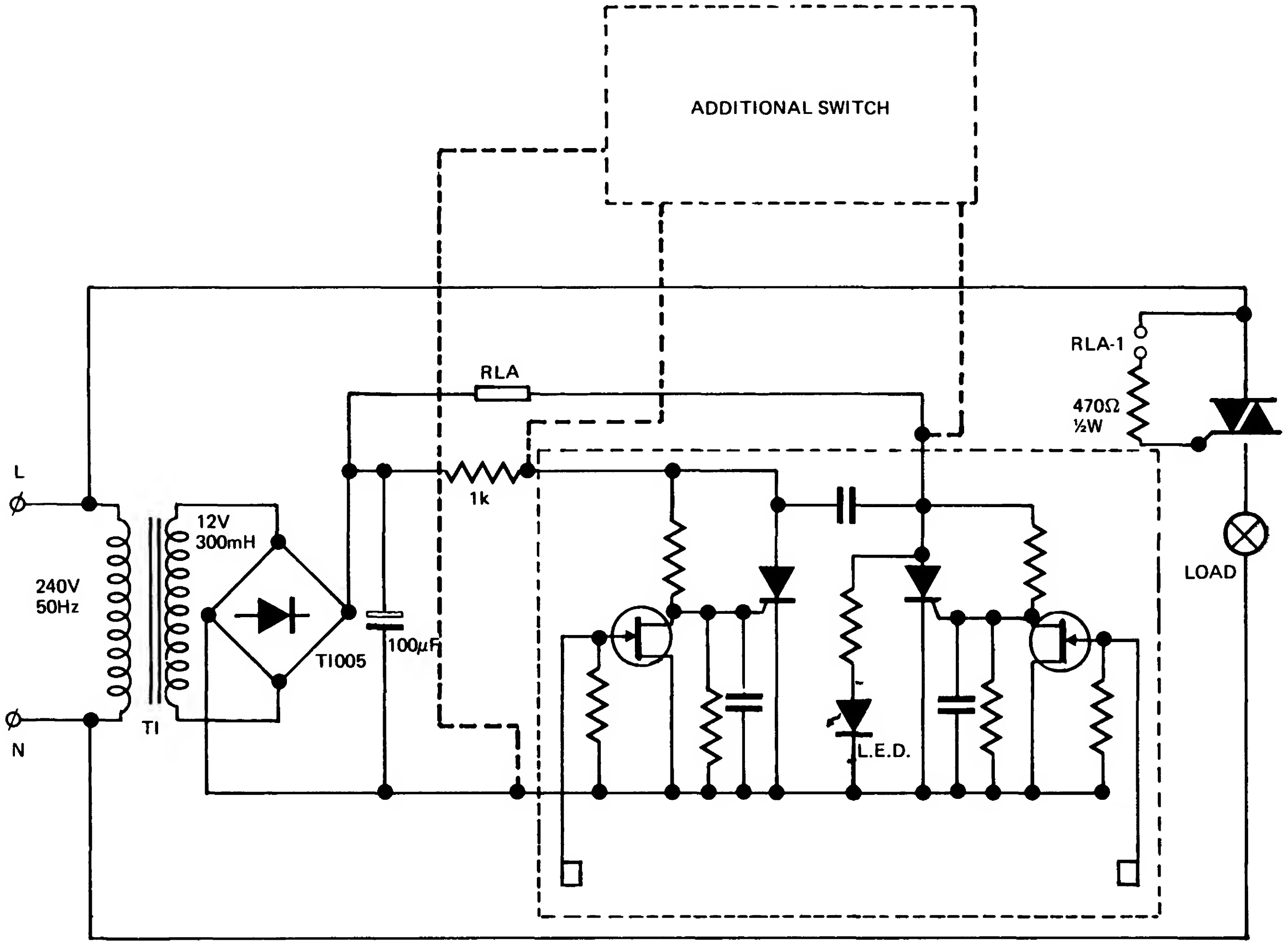


FIGURE 5. Complete F. E. T. Low Voltage Control Circuit

USING INTEGRATED CIRCUITS

Device Description

A number of i.c.s have been specially developed for touch/sense control particularly for use in television applications, but also useful, as will be seen, for other consumer and industrial applications. These consist of three digital circuits and an analogue circuit. The digital i.c.s detect the touch input, memorize the selected input, and then provide two outputs, one to drive an analogue part and a further high current output which could drive l.e.d.s or indicator bulbs. The analogue i.c. provides direct drive for numerical indicator tubes or neon indicators and selects one of four analogue inputs and feeds it to the output.

Digital I.C.s: The two basic digital i.c.s are the SN16861AN/NG 'mother' device and the SN16862AN expander device. The 'mother' device has four channels, and, by using the expander, these can be extended by blocks of four up to sixteen channels.

The internal block diagram of a digital device is shown in Figure 6. The signals from the touch plates are taken to the SENSE AMPLIFIERS INPUTS S1 to S4. The sense amplifiers select the appropriate 'thyristor' latch and turn the previously 'on' latch 'off' in the 4-bit register memory. The outputs of the 4-bit memory drive the CHANNEL SELECT OUTPUTS Q1 to Q4 and BAND SWITCH OUTPUTS B1 to B4 (S1 is the input for Q1 and B1, S2, for Q2 and B2, etc.). The selected output goes 'high' (i.e. greater than 13V from a 15V supply rail) all other outputs being 'off' or in the high impedance state. The constant current source is not present in the '862 expander device. The '861NG has the inbuilt facility that on providing the supply V_{CC} to the i.c., channel 1 is automatically selected. (For this preset to work correctly the V_{CC} slew rate between 3 and 8V should not be greater than 200V/s). The CASCADE outputs are connected together when the '862 expander i.c.s are used.

Analogue I.C.: An internal block diagram of the SN16848N analogue i.c. is shown in Figure 7. On receiving the digital signals on the CHANNEL SELECT INPUTS D1 to D4 the appropriate low drift, low offset, analogue switch is activated routing the voltage on the appropriate ANALOGUE INPUT A1 to A4 to the common ANALOGUE OUTPUT line A5. At the same time the appropriate display driver is switched 'on' so that a current 'sink' at the correct DISPLAY output N1 to N4 will operate the numerical or neon indicator. In cascading '848s the ANALOGUE OUTPUTs are connected together and with only one EMITTER FOLLOWER LOAD.

Channel Change System: A block diagram of a typical channel change system is shown in Figure 8 using two '862 expander i.c.s and three '848 analogue switch i.c.s with the '861 'mother' i.c..

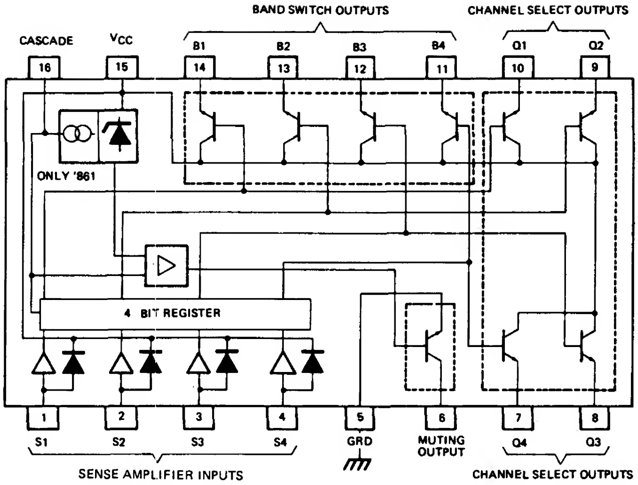

BAND SWITCH OUTPUTS
CHANNEL SELECT OUTPUTS
CASCADE
VCC
B1
B2
B3
B4
Q1
Q2
16
15
14
13
12
11
10
9
ONLY '861
4 BIT REGISTER
1
2
3
4
5
6
7
8
S1
S2
S3
S4
GRD
MUTING OUTPUT
Q4
Q3
SENSE AMPLIFIER INPUTS
CHANNEL SELECT OUTPUTS

FIGURE 6. Internal Block Diagram of SN16861/2NG

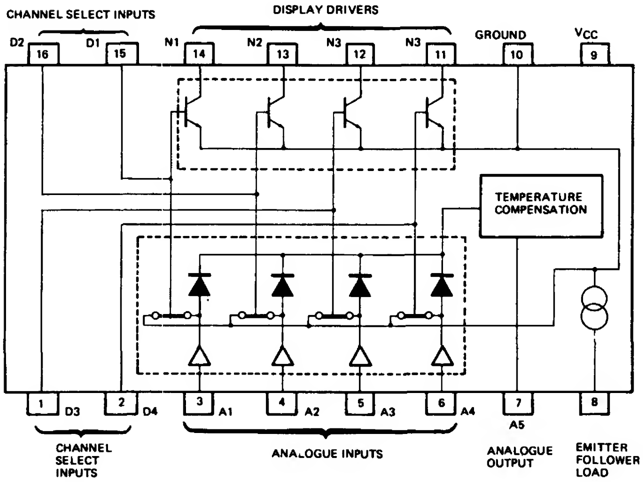

CHANNEL SELECT INPUTS
DISPLAY DRIVERS
D2
D1
N1
N2
N3
N3
GROUND
VCC
16
15
14
13
12
11
10
9
TEMPERATURE COMPENSATION
1
2
3
4
5
6
7
8
D3
D4
A1
A2
A3
A4
A5
CHANNEL SELECT INPUTS
ANALOGUE INPUTS
ANALOGUE OUTPUT
EMITTER FOLLOWER LOAD

FIGURE 7. Internal Block Diagram of SN16848N

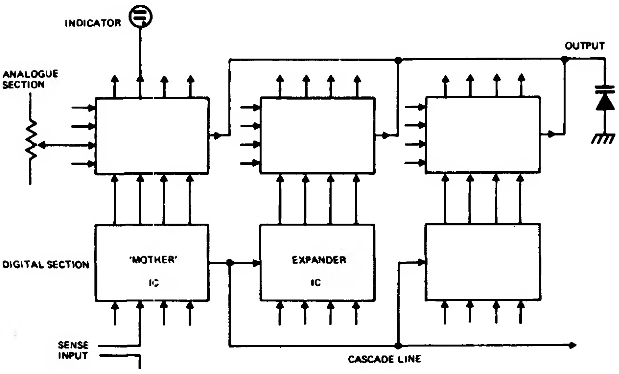

INDICATOR
OUTPUT
ANALOGUE SECTION
DIGITAL SECTION
'MOTHER' IC
EXPANDER IC
SENSE INPUT
CASCADE LINE

FIGURE 8. Block Diagram of a Channel Switching System

A Low Voltage System Using I.C. Touch Circuits

A low voltage wiring system can be controlled simply and effectively by using the SN16861NG i.c. working by capacitive discharge pick up, rather than more common bridging/impedance mode. Figure 9 shows the components needed for setting a 'high' or 'low' potential on the B2 BAND SWITCH OUTPUT. On supplying power to V_{CC}, the potential on B1 BAND SWITCH OUTPUT is 'high' due to the internal preset facility at switch 'on' and, as therefore B2 is 'low', there is no supply to the reed relay and it is not energised. On touching the plate connected to S2 SENSE AMPLIFIER INPUT, B1 goes 'low' and B2 goes 'high' and the reed relay is energised. Unused SENSE AMPLIFIER INPUTS 3 and 4 are connected to V_{CC} to ensure that they are non operative. 330pF capacitors are connected from INPUTS 1 and 2 to V_{CC} to lessen the sensitivity thus altenuating any 'pick up' signals present on the sensing leads. Accidential switching, caused by any voltage transients on the supply, is avoided by connected a 100nF capacitor between V_{CC} and ground.

The oscillograph in Figure 10 shows the attenuated continuous 'pick up' voltage before and after the touch time. The lower trace shows the change from 'low' to 'high' on B2 at the instant of touch; note the changeover occurs on the negative cycle of the 'pick up' voltage.

Figure 11 shows the complete low voltage wiring circuits. As the i.c. has a recommended supply voltage of between 11 and 18V, there is an addition of a 680µF smoothing capacitor and 15V zener diode, when compared with the f.e.t. circuit of Figure 5. To protect the wiring between say, the distribution box and touch plates, against a short circuit 82Ω 2W resistors are included. The i.c. could most simply be mounted behind a blank standard switch panel.

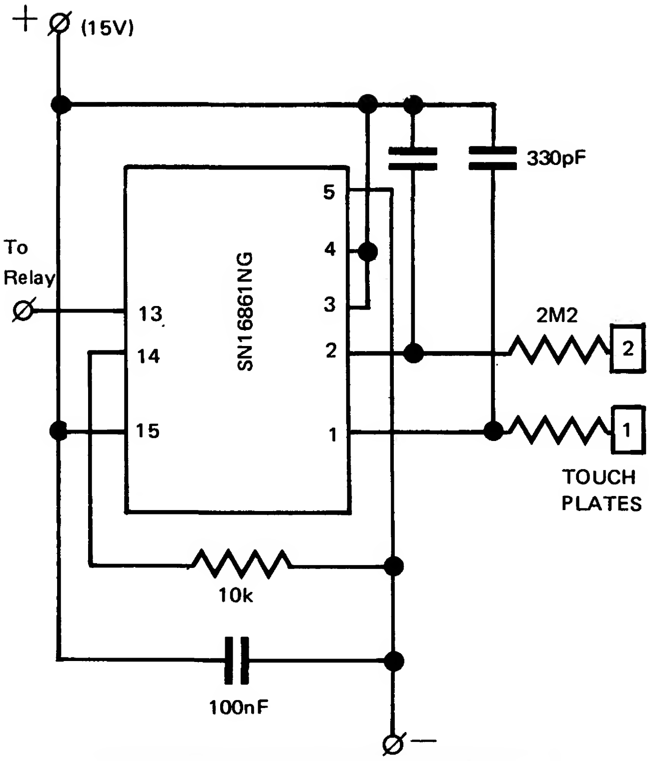

+ Ø (15V)
To Relay
Ø
SN16861NG
13
14
15
5
4
3
2
1
330pF
2M2
2
1
TOUCH PLATES
10k
100nF
Ø—

FIGURE 9. Standard Touch Switch

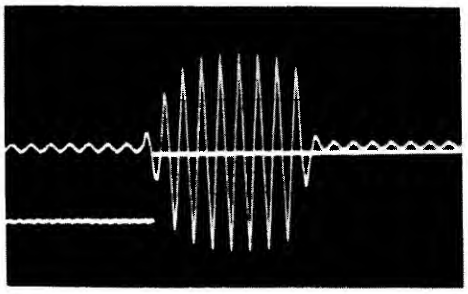


FIGURE 10. Attenuated 'Pick-Up' Voltage Waveform

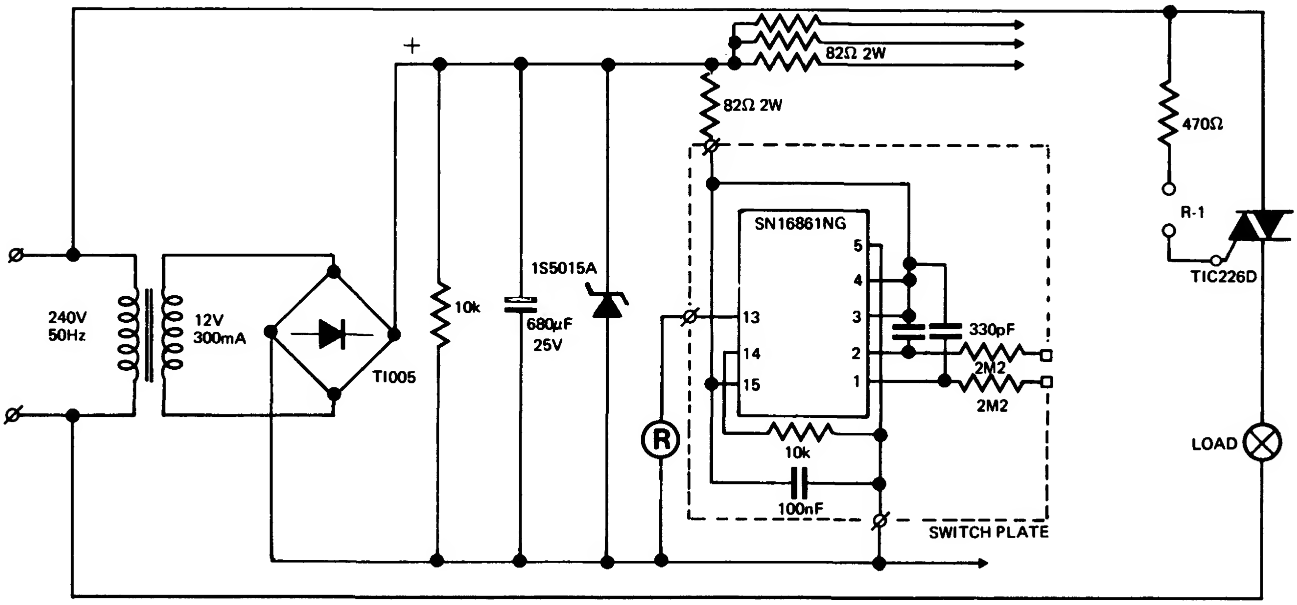

Ø
Ø
240V 50Hz
12V 300mA
T1005
+
10k
1S5015A
680µF 25V
82Ω 2W
82Ω 2W
SN16861NG
5
4
3
2
1
13
14
15
330pF
2M2
2M2
R
10k
100nF
Ø
Ø
SWITCH PLATE
470Ω
R-1
TIC226D
LOAD

FIGURE 11. Complete I. C. Controlled Low Voltage Circuit

Paralleling: With i.c.s paralleling is not the simple arrangement as mentioned with f.e.t.s; 50Hz 'pick up' on the wires to the touch buttons prevents dual controlling with i.c.s on the sensing side. One way of overcoming the problem is to add to one touch switch (the master) an exclusive OR gate as shown in Figure 12. Current can only flow in this arrangement when the outputs from the two i.c. B2 OUTPUTS are at different levels, and thus either switch can be used for control.

3 Lamp Control: By exploiting all the inputs and outputs of the '861 i.c., three relays and thus lamps or other relay loads, can be controlled as shown in Figure 13. The arrangement can be varied; a combination of 'a' and 'b' gives individual control of three lamps by touching one of four plates. A typical application of this type of control could be in a home where control of three individual lamps in different parts of the room is required. The combination of 'c' and 'b' offers dimming facilities. By touching button '2', relay A will energise switching on lamp A. By touching button '3' the B3 OUTPUT will go 'high' turning 'on' relay B and, via a diode, relay A. Button '4' will raise the potential at the B4 OUTPUT switching 'on' relay C and relays B and A via corresponding diodes. Hence all three lamps will be switched 'on'. A suitable place to control the level of light in this way could be the centre lamps in a sitting room.

Using Long Interconnections: If the touch switches must be several meters, say, from the voltage supply e.g. in a house, then additional components are required to boost the sensitivity. The switching occurs on the negative excursion of the 'pick up' voltage. Thus to make switching most sensitive the power supply must be raised with respect to earth. One method of achieving this is shown in Figure 14 using a resistor and a capacitor. Here the negative line of the low voltage system will oscillate up to approximately 30V peak as shown in the oscillographs of Figure 15. The second trace shows that the output voltage goes 'high' at a potential positive to earth.

Heating Element Control

The combination of an '862 i.c. connected in parallel with an '861 to give eight outputs provides an ideal arrangement for proportional control of heating elements such as, for instance, the electric rings of a cooker. Figure 16 shows the circuit components for providing the sensing and control section of the system. On switching on power, the '861 i.c.'s internal arrangements ensure that its B1 OUTPUT is 'high' and its B2 to B4 and the OUTPUTS of the '862 i.c. are all 'low'. Thus the light emitting diode (l.e.d.) corresponding to the no power,) position say, will be lit. Touching any one of the pads, connected to the S2 to S4 SENSE AMPLIFIER INPUTS of the '861 and S1 to S4 INPUTS of the '862 will cause the corresponding OUT-

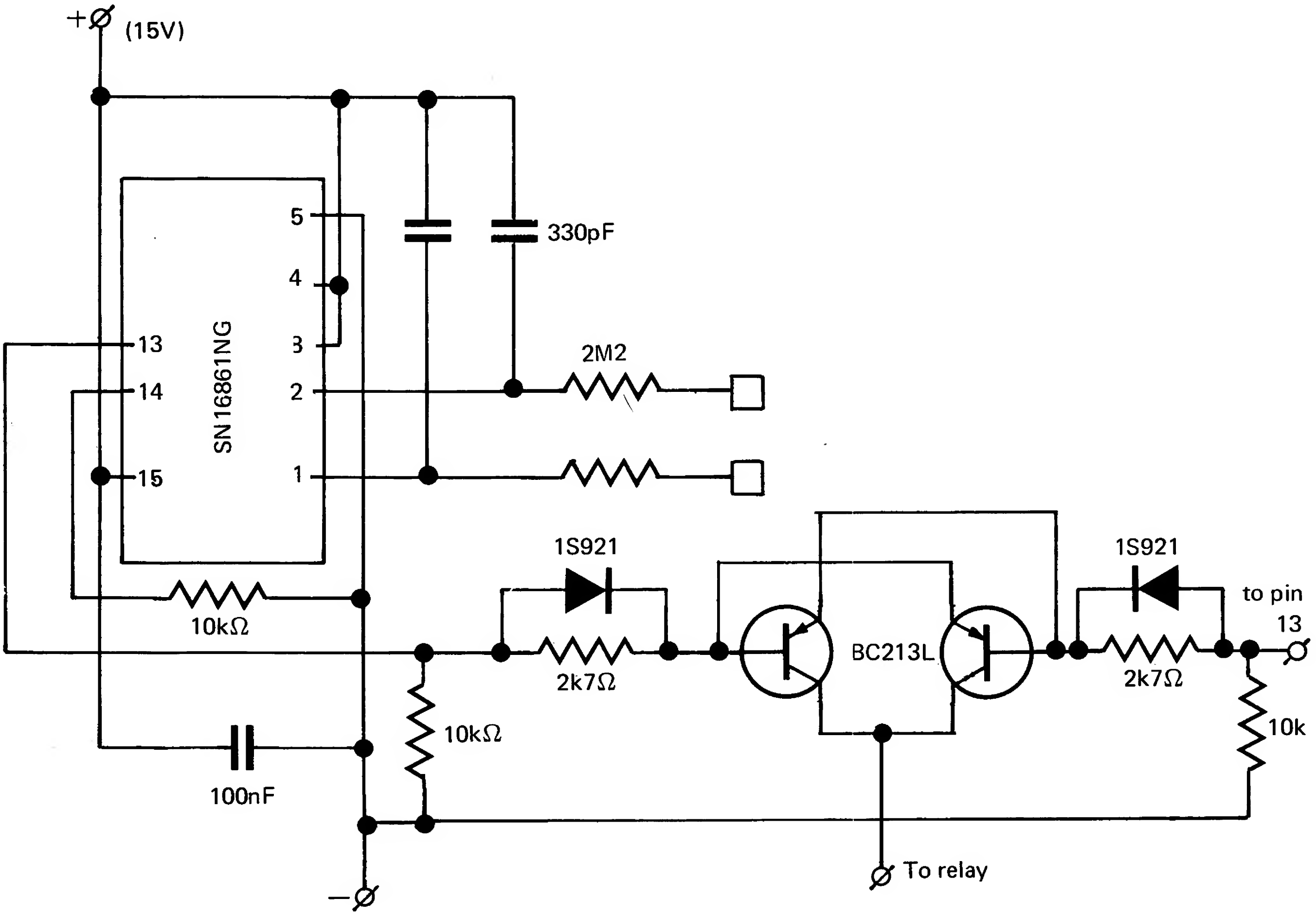


FIGURE 12. Master Touch Switch for Parallel Connection

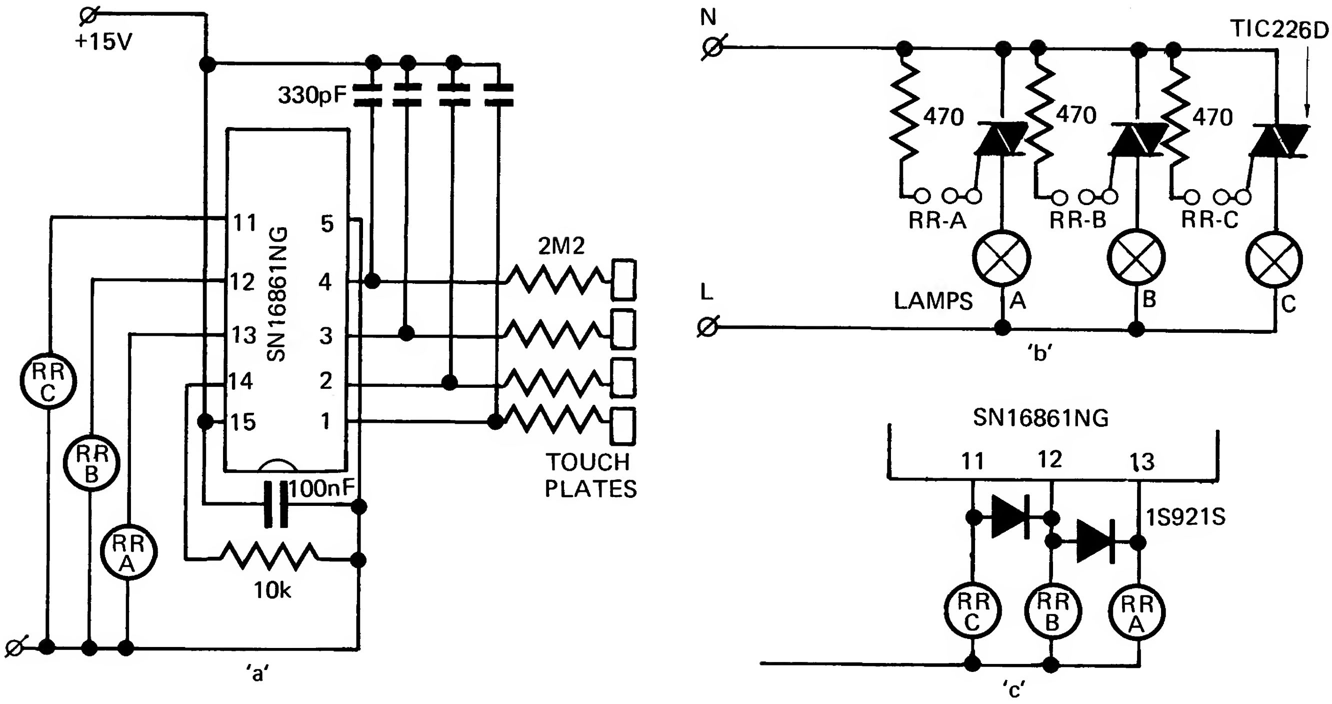

+15V
330pF
SN16861NG
11
12
13
14
15
5
4
3
2
1
2M2
TOUCH PLATES
100nF
10k
RR C
RR B
RR A
'a'
N
L
TIC226D
470
470
470
RR-A
RR-B
RR-C
LAMPS
A
B
C
'b'
SN16861NG
11
12
13
1S921S
RR C
RR B
RR A
'c'

FIGURE 13. Three Lamp Control Circuit

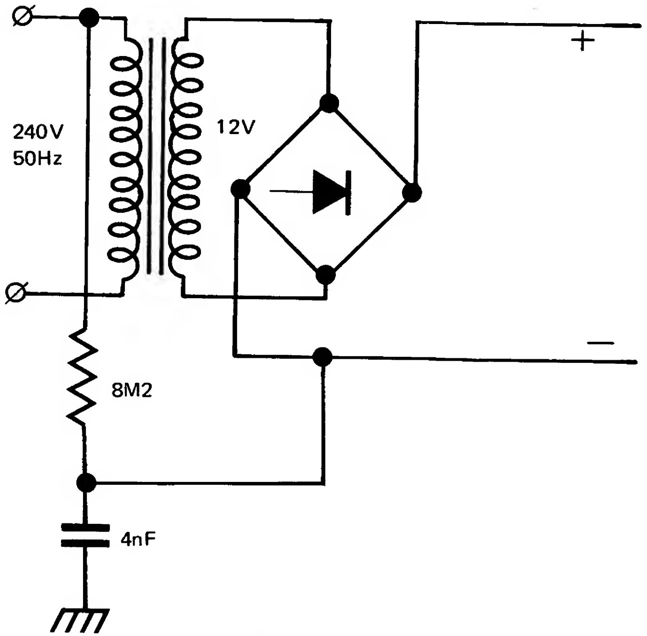
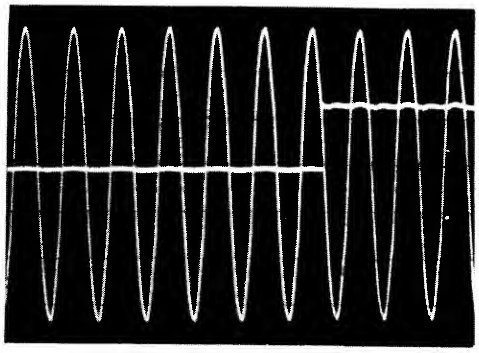

240V
50Hz
12V
+
−
8M2
4nF

FIGURE 14. Booster Circuit



FIGURW 15. Boosted 'Pick-Up Voltage Waveform

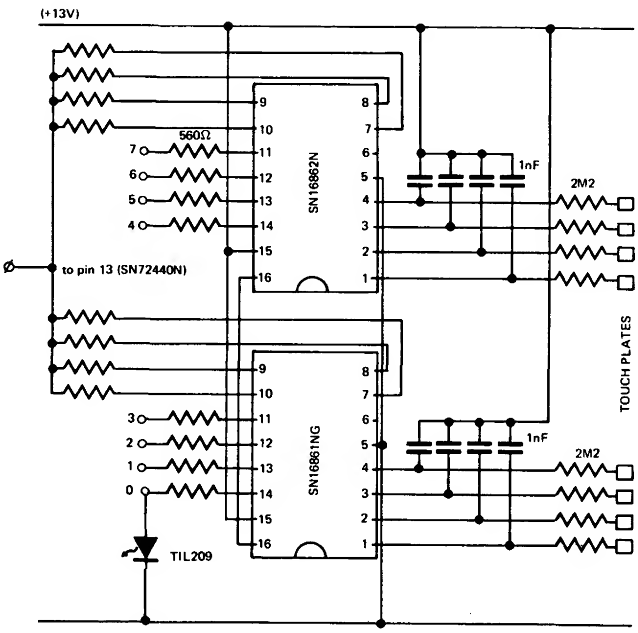
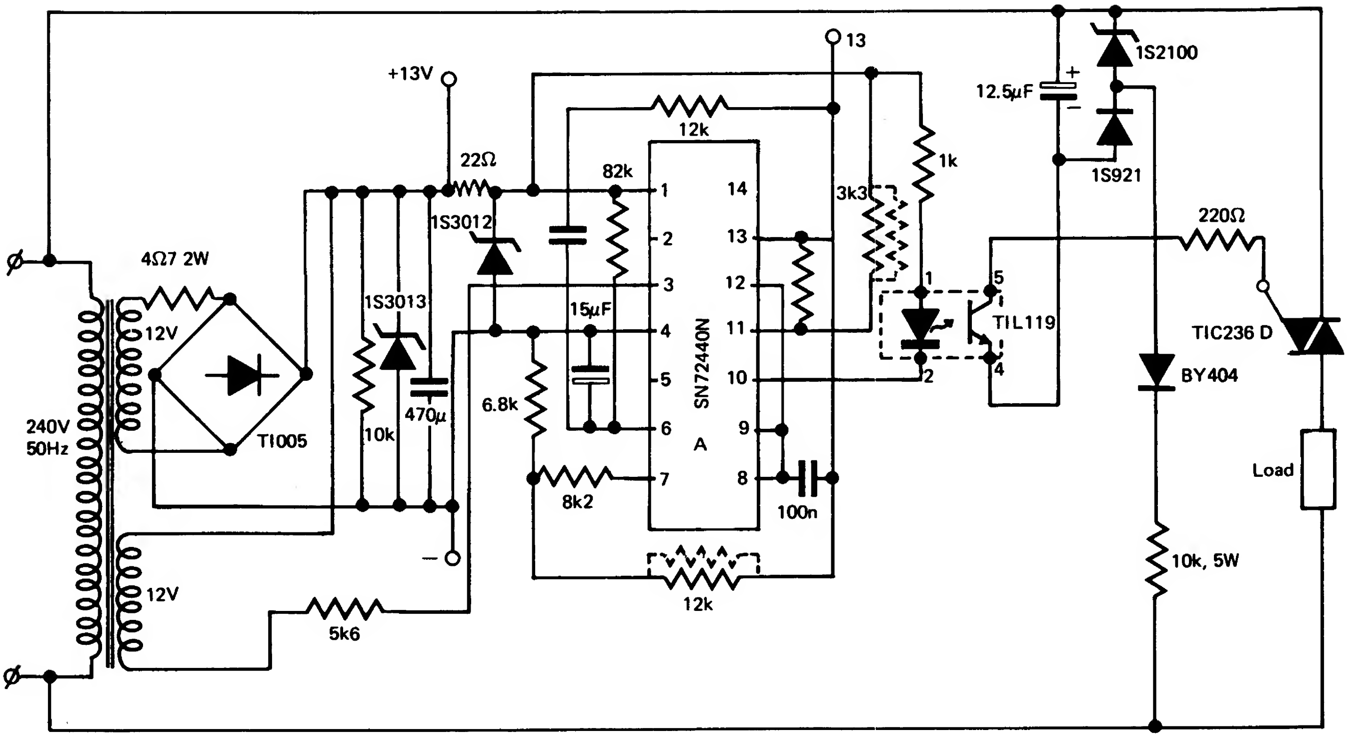

(+13V)
560Ω
7
6
5
4
3
2
1
0
SN16862N
SN16861NG
to pin 13 (SN72440N)
TIL209
1nF
1nF
2M2
2M2
TOUCH PLATES
9
10
11
12
13
14
15
16
8
7
6
5
4
3
2
1

FIGURE 16. Sensing and Control Section



+13V
13
22Ω
12k
82k
1S3012
1S3013
15μF
4Ω7 2W
12V
T1005
240V
50Hz
10k
470μ
6.8k
8k2
SN72440N
A
1
2
3
4
5
6
7
14
13
12
11
10
9
8
100n
12k
12V
5k6
3k3
1k
12.5μF
1S2100
1S921
220Ω
TIL119
TIC236 D
BY404
Load
10k, 5W

FIGURE 17. Power Section

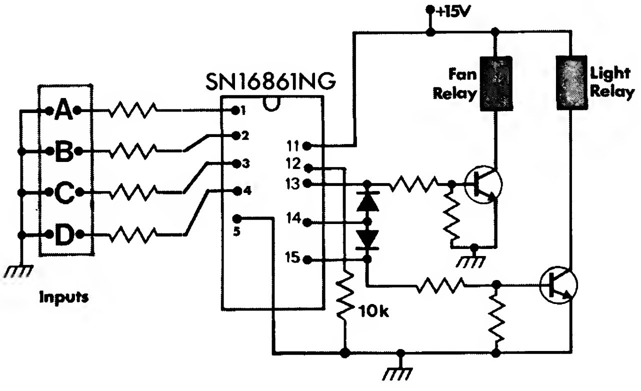
PUTS (B2 to B4 and B1 to B4) to go 'high' and light its associated l.e.d.. At the same time the corresponding CHANNEL SELECT OUTPUT will provide an output to the following power control circuit. (The value of each series impedance will depend on the setting, or heating effect, required, 1 to 7 say).

The power control circuit is shown in Figure 17. The basic component is the SN72440 zero cross detector i.c.[3]. Here this i.c. does not obtain its power from the mains supply, but from a 12V system as shown. In order to prevent any half waving a hysteresis loop consisting of two resistors, a3k3Ω and 15kΩ, is connected to the i.c.. As this, by itself, would restrict the range of 'burst firing' control, hysterics reset components are added (a 12kΩ resistor in series with a 2μ2F unpolarised capacitor). Thus the range of control is extended from its original 35 to 75%, to 2% to 98%. Isolation is provided by a TIL119 optocoupler using, as shown, its own derived power supply.

This system, needing only 6 wires carrying only mAs to control, say, four heating elements, is ideal for remote control. Thus the touch pads could be flush mounted at a convenient place away from the cooker. Alternatively indication of the 'on' heating element and its setting could be achieved by using numerical displays.

Light/Fan Control

Figure 18 shows the arrangement using an '861 i.c. for controlling the switching of a light and/or fan. On switching power on or bridging A, B1 OUTPUT (pin 14) is 'high' and the other BAND SWITCH OUTPUTS are 'low'. Therefore both transistors are 'off' and both fan and light are 'off'. Bridging B causes B2 OUTPUT (pin 13) to go 'high' and turn 'on' the transistor supplying current to operate the fan relay. Bridging C causes the B3 OUTPUT (pin 12) to go 'high' and, as both transistors have base current via the diodes, they will switch on both the fan and light relays. Finally bridging D will cause the B4 OUTPUT (pin 11) to go 'high' providing current for the transistor operating the light relay.



+15V
SN16861NG
A
B
C
D
Inputs
1
2
3
4
5
11
12
13
14
15
Fan Relay
Light Relay
10k

FIGURE 18. Light/Fan Control

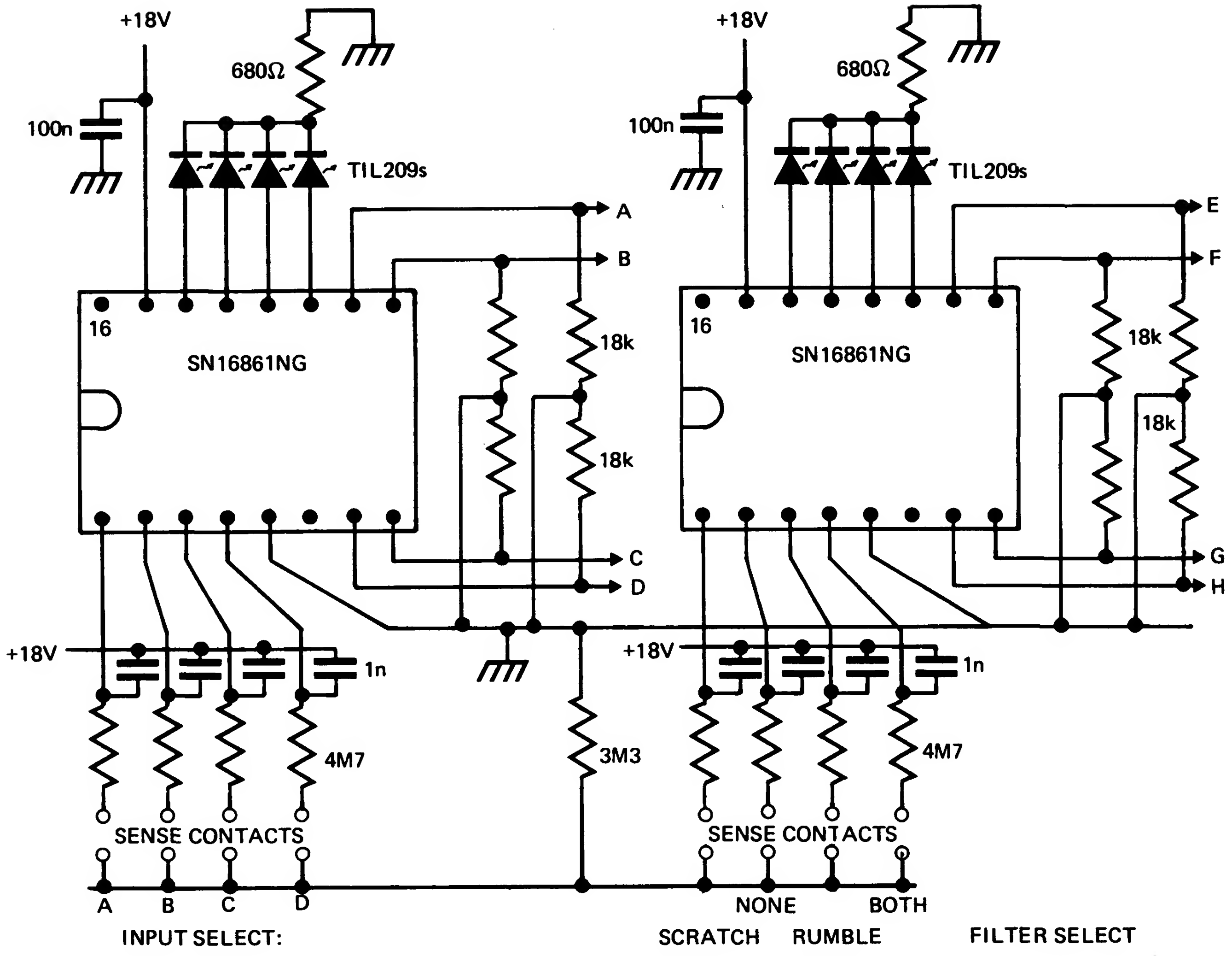

+18V
680Ω
100n
TIL209s
A
B
16
SN16861NG
18k
18k
C
D
+18V
1n
4M7
3M3
SENSE CONTACTS
A
B
C
D
INPUT SELECT:
+18V
680Ω
100n
TIL209s
E
F
16
SN16861NG
18k
18k
G
H
+18V
1n
4M7
SENSE CONTACTS
NONE
BOTH
SCRATCH
RUMBLE
FILTER SELECT

FIGURE 19. Two 4-Channel Selection Circuit

Function Control for Audio Amplifiers

The '861 i.c. can be used in audio amplifiers to generate signals to drive gating circuits such as those required for function or filter selection. Figure 19 shows the arrangement of two '861s to provide two 4-channel selectors. Signals from the CHANNEL SELECT OUTPUTS drive the gating circuits directly. Each BAND SWITCH OUTPUT has an associated TIL209 l.e.d. to indicate the selected function or filter. An 18V supply is used to enable the gating circuits to handle as large an audio signal as possible (3V r.m.s). The 100nF decoupling capacitors on the supply lines are important as they prevent interaction between the two '861 i.c.s. (These should be situated close to the actual i.c.).

Figure 20 shows the basic function selection circuit. One of the diodes is held in forward bias by the potential at the CHANNEL SELECT OUTPUT of the '861. The other three diodes are reverse biassed and prevent the passage of signals at other inputs. A high input impedance buffer stage, using transistor VT1, must follow the diode switch in order to minimise distortion.

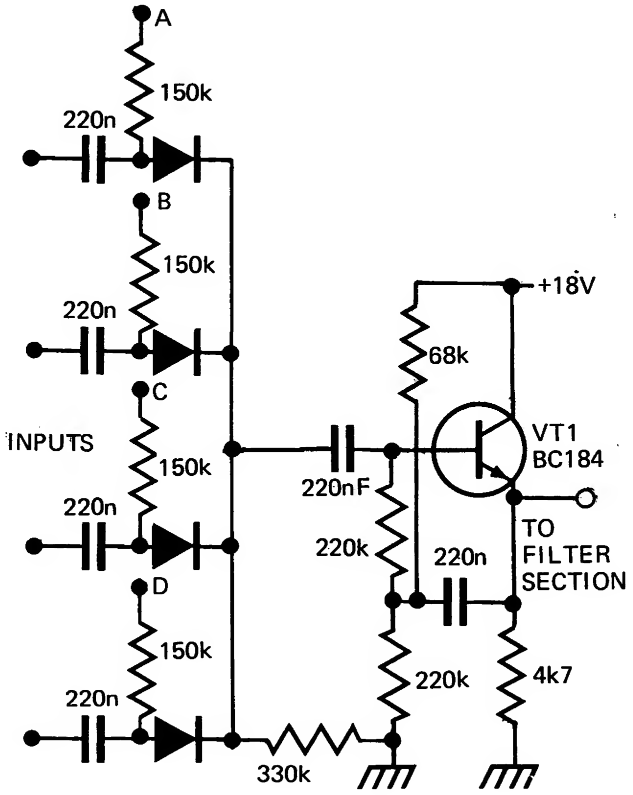

A
150k
220n
B
150k
220n
C
INPUTS
150k
220n
D
150k
220n
330k
+18V
68k
VT1
BC184
220nF
220k
220n
TO FILTER SECTION
220k
4k7

FIGURE 20. Function Selection Circuit

Figure 21 shows the filter selection circuits, i.e. scratch, rumble, rumble and scratch, or bypass. There are conventional two pole filters^4 and give a 12dB/octave 'roll off' at 40Hz and 10kHz as shown by the measured performance curve shown in Figure 22. The output from one of the filters is selected by a further diode switch with its associatedt buffer, identical to that used in Figure 20.

Such a system allows the front panel control to be a great distance from the signal circuits, eliminated the need long long lengths of coaxial cables.

A Static 8-Channel Touch Control Circuit

Selection of one of the 8 channels is accomplished with one '861 i.c. and one '862 i.c. in cascade as shown in Figure 23. The CHANNEL SELECT OUTPUTS are fed to two '848s which in turn route the voltage from one of the control potentiometers to their common output. The '848 i.c. is also used, in this circuit, to drive high voltage gas discharge indicators. Alternatively the 2 times 4 BAND SWITCH OUTPUTS from the '861 i.c. and '862 i.c. can be used to energise l.e.d. s as described in previous applications. This would also eliminate the need for a high voltage supply, although a regulated supply to the '848 i.c.s and the potentiometers is still required.

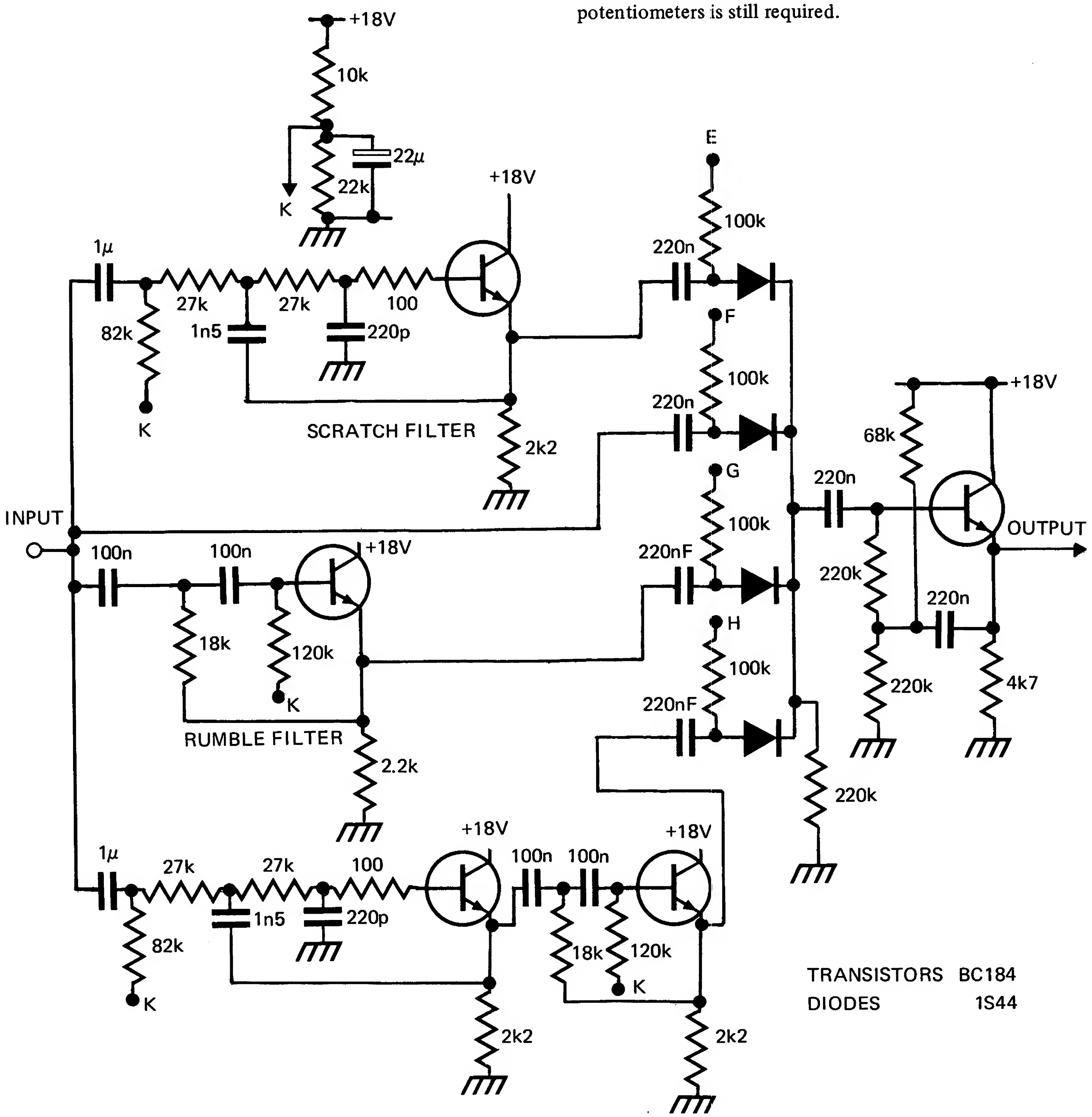

+18V
10k
22μ
22k
K
1μ
27k
27k
100
82k
1n5
220p
SCRATCH FILTER
2k2
INPUT
100n
100n
18k
120k
RUMBLE FILTER
2.2k
82k
2k2
100n 100n
18k
120k
2k2
E
F
G
H
100k
220n
220nF
68k
220k
4k7
OUTPUT
TRANSISTORS BC184
DIODES 1S44

FIGURE 21. Filter Selection Circuits

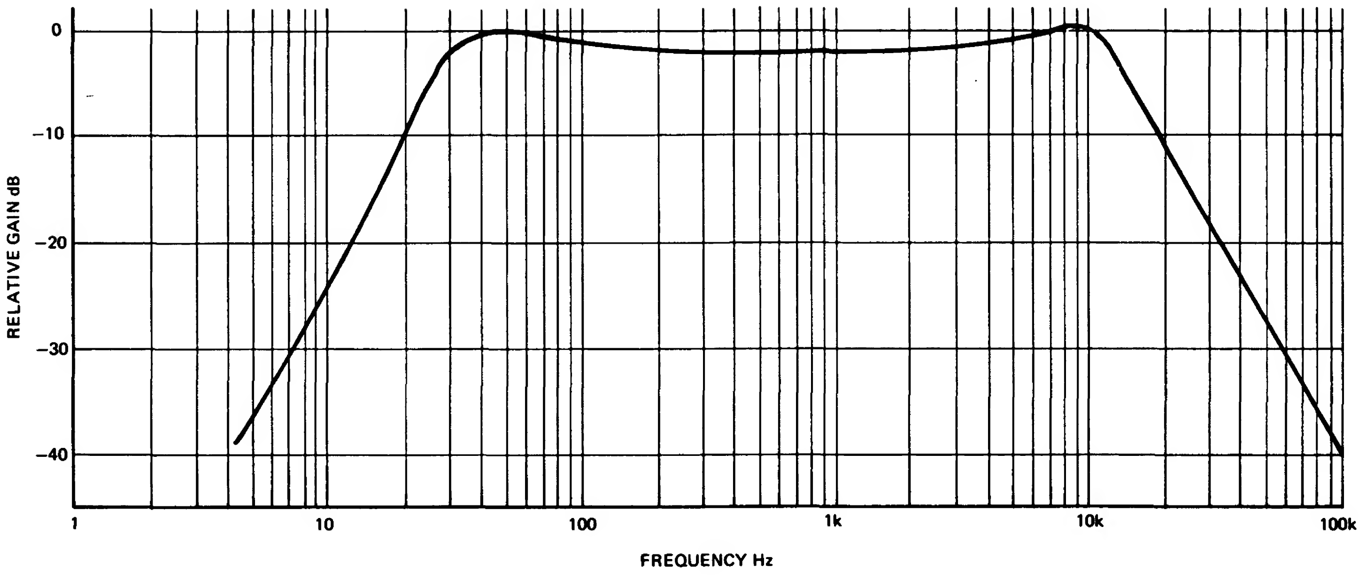
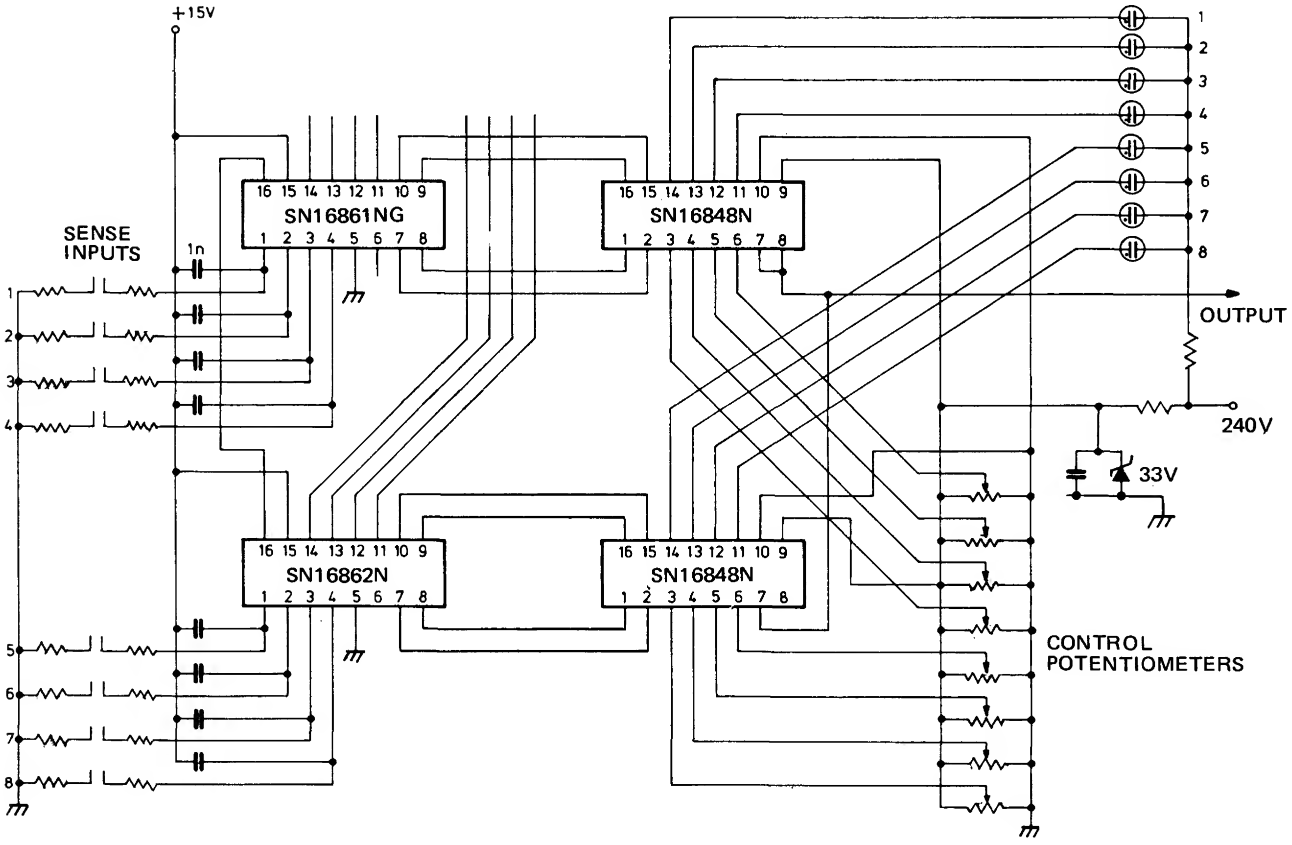


FIGURE 22. Rumble and Scratch Filter Response



+15V
SENSE INPUTS
1n
SN16861NG
SN16848N
SN16862N
SN16848N
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
1
2
3
4
5
6
7
8
OUTPUT
240V
33V
CONTROL POTENTIOMETERS

FIGURE 23. Static 8-Channel Touch Control Circuit

Dynamic and Static Selection Circuit

The circuit for an 8-channel dynamic and static selection circuit is shown in Figure 24. When the stepping switch is closed the next channel in sequence is selected. This is achieved as follows: if any output (1-7) has been selected the capacitor feeding the next CHANNEL SELECT INPUT will have charged up. The cascade line is taken 'low' for a short time when the stepping switch is closed. This prevents any CHANNEL SELECT OUTPUT being 'high', so a transition is coupled to the next CHANNEL SELECT INPUT via the capacitor which has been previously charged. The loop cannot be closed by taking output 8 back to input 1 or oscillation takes place. If no channel is selected after the stepping switch is closed the voltage on the cascade line rises to 6V. (It is normally at about 3V when a channel is selected) and after a short time, the transistor is turned on selecting channel 1.

The cycle can be shortened by preventing capacitive coupling taking place after the required number of steps, e.g. taking point X to ground.

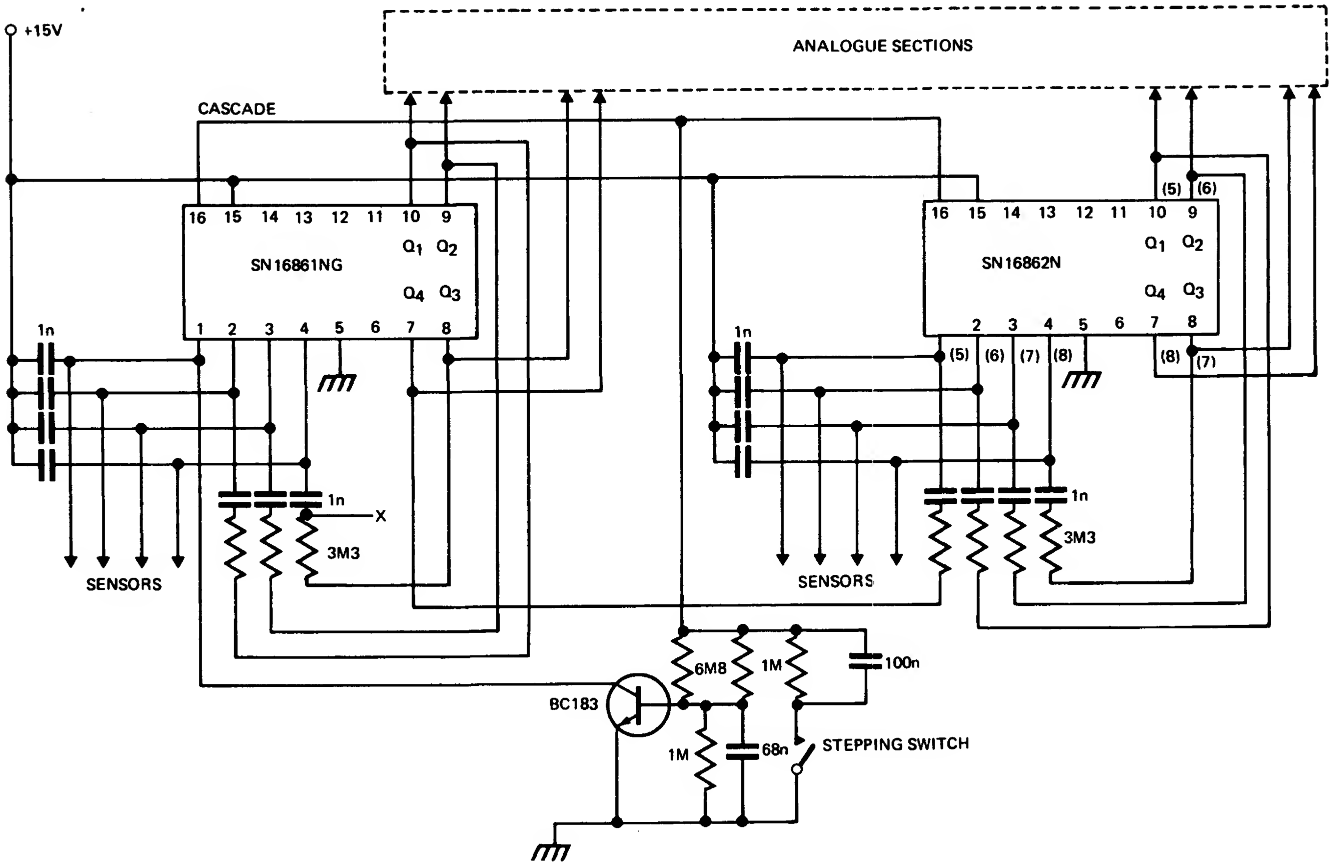
REFERENCES

1. C. F. G. Delaney, *Electronics for the Physicist,* Penguin Books, Harmondsworth, Middx., 1969.
2. *Semiconductor Circuit Design,* Volume I, Texas Instruments Ltd, pp 17, April 1972.
3. *Semiconductor Circuit Design,* Volume III, Texas Instruments Ltd, pp 107-111, April 1974.
4. *Semiconductor Circuit Design,* Volume II, Texas Instruments Ltd, pp 138-139, April 1973.

ACKNOWLEDGEMENTS

The low voltage wiring system is subjected to a patent submission by Simplex Wiring Systems Limited of Liverpool. Thanks are due to them for permission to include the system in this chapter.

The function control circuits for audio amplifiers were designed and explained by Jonathan Dell.



+15V
ANALOGUE SECTIONS
CASCADE
16 15 14 13 12 11 10 9
Q1 Q2
SN16861NG
Q4 Q3
1 2 3 4 5 6 7 8
1n
1n
X
3M3
SENSORS
16 15 14 13 12 11 10 9
(5) (6)
Q1 Q2
SN16862N
Q4 Q3
2 3 4 5 6 7 8
(5) (6) (7) (8)
(8) (7)
1n
1n
3M3
SENSORS
6M8
1M
100n
BC183
1M
68n
STEPPING SWITCH

FIGURE 24. Dynamic and Static Selection Circuit

VII PSYCHEDELIC LIGHTS CONTROL

By
Jurek Budek

A bizarre form of power control but, perhaps, an interesting one, is the operation of psychedelic lights, i.e. light responding directly to sound. In essence, in a 'psychedelic' light system, sound controlled modulators convert bass, middle and treble frequencies into corresponding bursts of light; thus adding a new 'visual' dimension to the beat of the music. This is achieved by taking a signal from across the loudspeaker terminals and feeding it into a filter circuit whose output provides pulses which correspond to the sound spectrum–bass, middle and treble and any combinations of these three channels. These pulses then pass through an interface circuit and energise appropriate triacs[1] which, in turn, switch (or control) the lamps.

CIRCUIT DESCRIPTION

Zero Voltage Switching

As stated, the lights are turned on and off by utilising a triac, rather than two thyristors connected back to back, thus controlling the positive and negative cycle of the supply voltage. Recapping[2], whereas the thyristor requires a positive gate to cathode voltage and will turn on only when the anode voltage is positive with respect to the cathode, triacs will turn on when the gate voltage polarity is the same as voltage between mt2 and mt1 (main terminal 2 and 1), i.e. positive for the positive half cycle and negative for the negative half cycle. In addition a triac will turn on with the gate negative with respect to the mt1 terminal for either polarity of mt2. It is the latter factor which accounts for the techniques used in the circuits to be discussed in this chapter. Triacs used in a phase control mode produce considerable radio frequency interference (r.f.i.) due to the step change in current. The noise thus generated is spread by means of conduction through the wiring system or by radiation. Suppressing r.f.i. becomes more difficult and expensive as the load increases. Uncontrolled switching of 'psychedelic' lamps on and off will have a similar effect and will also introduce additional noise in the loudspeakers. A simple solution to this problem is to arrange the switching so that it always takes place at the point where the mains supply voltage crosses zero, as shown in Figure 1. This technique is called 'zero voltage switching' or 'burst firing'.[3] In this way isolated numbers of half or full cycles will pass through the lamps and thus avoid step change in currents, which also has the additional advantage of increasing the life of the lamp.

Figure 2 shows a circuit used to generate the pulses at the point of zero voltage crossing. Transistor VT1, whose base is connected to the unsmoothed supply from the bridge rectifier D1-4, is on most of the time. However, each time the mains voltage crosses zero, its base voltage is taken below the holding on voltage and it thus turns off, giving positive pulses on its collector. In order to reduce the loading on transistor VT1, transistor VT2 has been added. Positive pulses appear as an output across resistor R each time the mains voltage crosses the zero point.

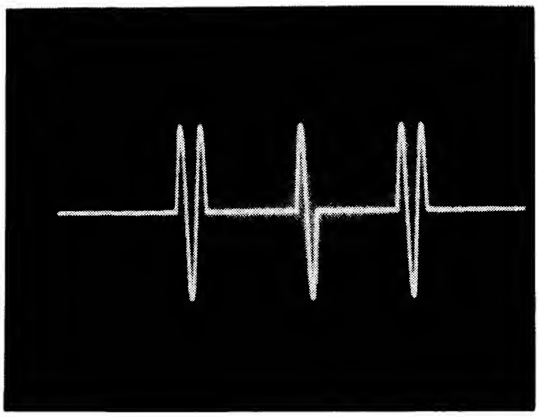


FIGURE 1. Waveform Depicting Zero Voltage Switching.

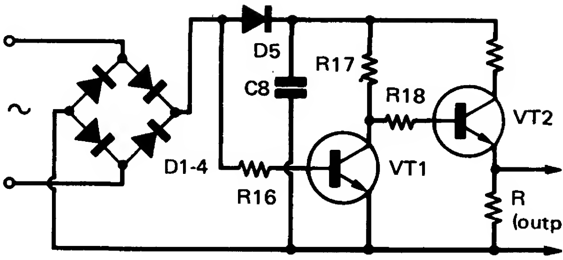


FIGURE 2. Zero Voltage Crossing Circuit.

Filters

In order to control the lamp switching which respect to the frequency bands, a circuit is required which will separate out the low, middle and high frequencies from the voltage waveform appearing at the terminals of a loudspeaker. A typical voltage waveform appearing at this point is shown in Figure 3. Various types of filters could be employed; e.g. a resistor/capacitor network for high and low pass filters and an inductor/capacitor network for middle frequencies. Here, however, integrated circuit (i.c.) operational amplifiers are employed in a positive fixed-gain configuration, as the active filter element[4], and resistors and capacitors as passive elements. By choosing suitable component values a sharp separation between bass, middle and treble frequencies can be obtained.

The shape of the filter response is determined by the damping ratio (ζ), the lower this is, the sharper the cut-off. There is a 'peaking' effect, but this is of no importance in this application. Critical damping actually occurs when $\zeta = 1/2^{1/2} = 0.707$ but in order to reduce the sharpness, this value is reduced to 0.5 in the practical filter circuits. From the equations for this form of filter element[4], the component values are calculated for the three types of filter required, i.e. low pass, band pass and high pass.

Musically oriented readers will recall the 'unisono' note played on the oboe during the orchestra's tuning-up time, just before the concert begins. This note is middle 'A' with a frequency of 440Hz; a frequency which has been chosen as the centre frequency for the middle band-pass filter in this design. Cut-off frequency for the low pass filter has been chosen to be around 200Hz and that of the high pass filter (treble) about 1kHz.

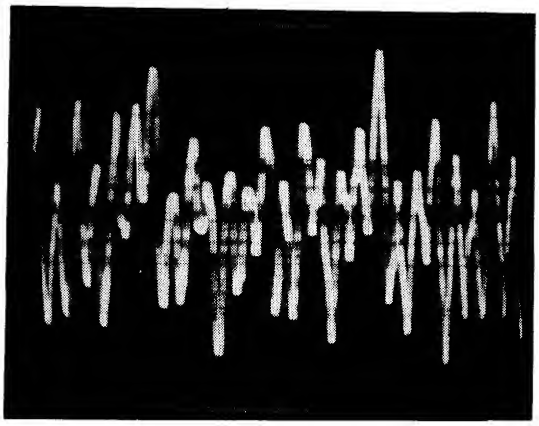


FIGURE 3. Typical Music Voltage Waveform.

Based on the above assumptions, a complete filter has been developed with the component values as shown in Figure 4. (Some of the component values differ from the figures obtained using the formulae in order to improve the separation between the various frequency ranges.) The input to the filter circuit has been limited to 5V peak to peak by using two 5V zener diodes, ZD1 & ZD2, connected back to back. The 10kΩ potentiometer, VR1, also added at the input to the filter circuit allows the voltage level at

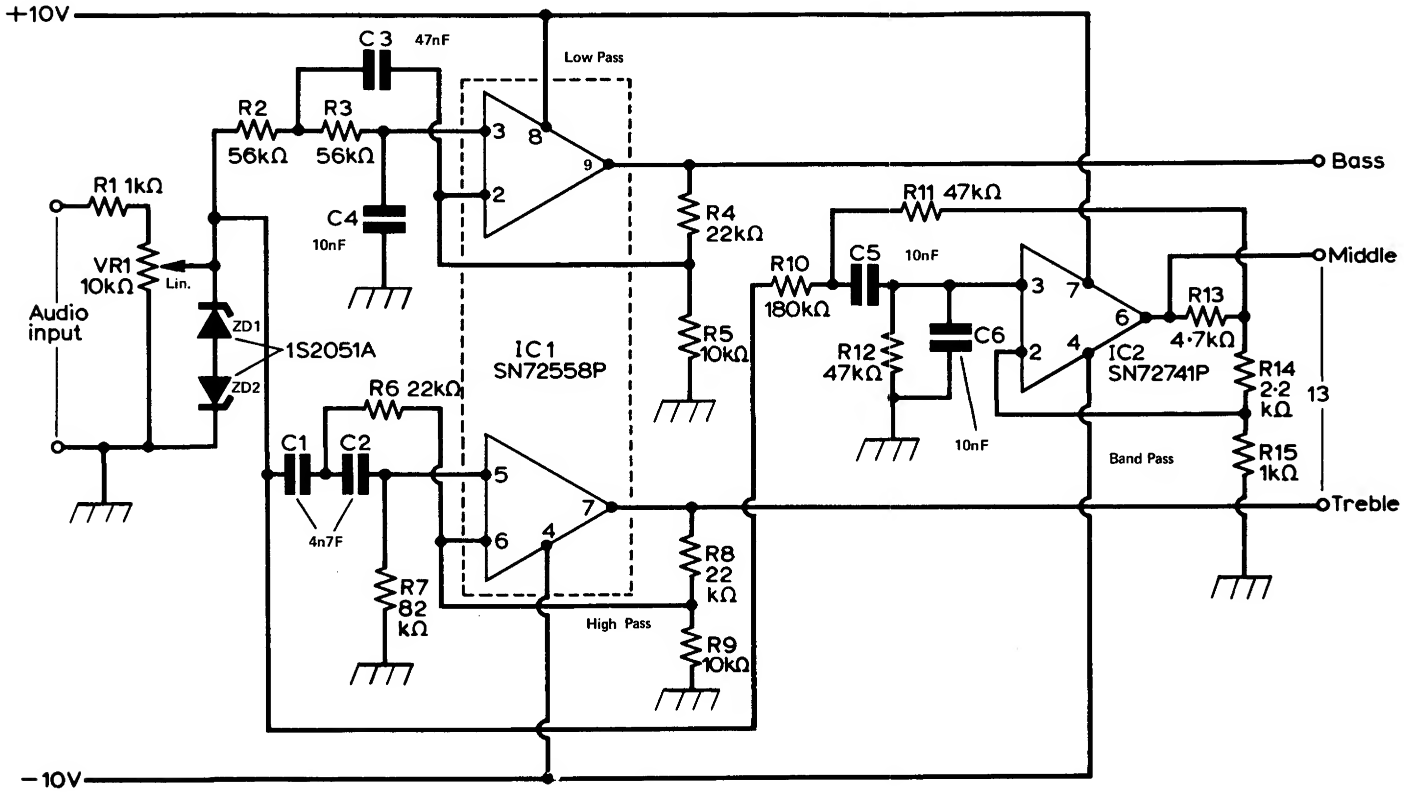

+10V
−10V
C3 47nF
Low Pass
R2
R3
56kΩ
56kΩ
3
8
9
2
R1 1kΩ
VR1
10kΩ
Lin.
Audio
input
C4
10nF
ZD1
ZD2
1S2051A
IC1
SN72558P
R4
22kΩ
R5
10kΩ
R6 22kΩ
C1
C2
4n7F
5
6
7
4
R7
82
kΩ
R8
22
kΩ
R9
10kΩ
High Pass
Bass
R11 47kΩ
R10
180kΩ
C5 10nF
R12
47kΩ
C6
10nF
3
7
6
2
4
IC2
SN72741P
R13
4·7kΩ
R14
2·2
kΩ
R15
1kΩ
13
Band Pass
Middle
Treble

FIGURE 4. Complete Filter Circuit.

which the lamps are switched to be controlled. In this way it is possible to establish the best effect for 'soft' or 'party' type music. As the amplifiers used have a voltage gain of unity, the output voltage of the high and low pass filters can never be more than the input voltage. In order to achieve voltage gain so that sufficient output can be obtained to drive the interface circuit at low volume levels, the basic circuit must be modified. This involves reducing the proportion of output voltage from the amplifier that is used as feedback to the filter capacitors and resistors, and is achieved by the use of a resistive potential divider at the output of the amplifier, as is shown. The resistor ratio determines the gain of the filter in the pass-band.

Figure 5 shows output voltage response of the three filters plotted against frequency for a peak input signal of 0.5V. The triacs turn on their corresponding lamps at filter output voltages equal to and higher than 1.5V.

Figures 6a to 6d show four oscilloscope photographs. In each instance the four traces were taken simultaneously (i.e. they have a common time axes). In the oscillograms the top trace corresponds to the voltage at the loudspeaker terminal. The other three traces were taken at the outputs of the respective filters. Figure 6a was taken at a time when the treble frequency was predominant. In Figure 6b the middle frequency is the strongest signal, while in Figure 6c it is the bass Figure 6d shows some interesting combinations of all three frequencies. The middle frequencies predominate at the beginning of the trace, then the treble takes over at the centre of oscillogram and towards the end of the trace it is the turn of the bass to predominate.

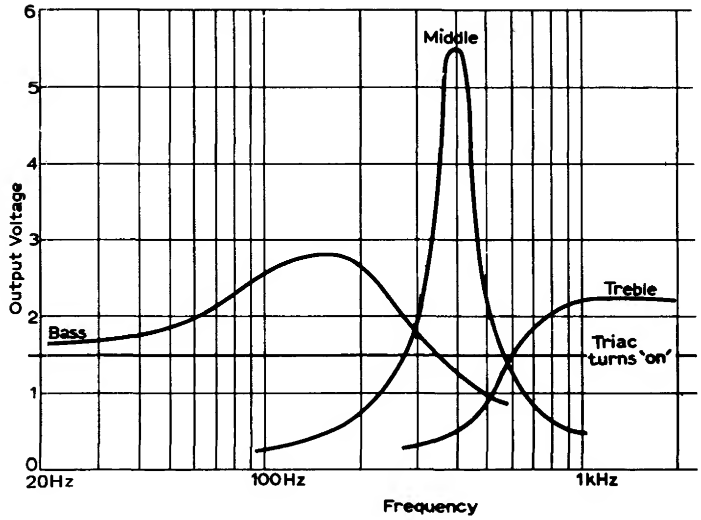
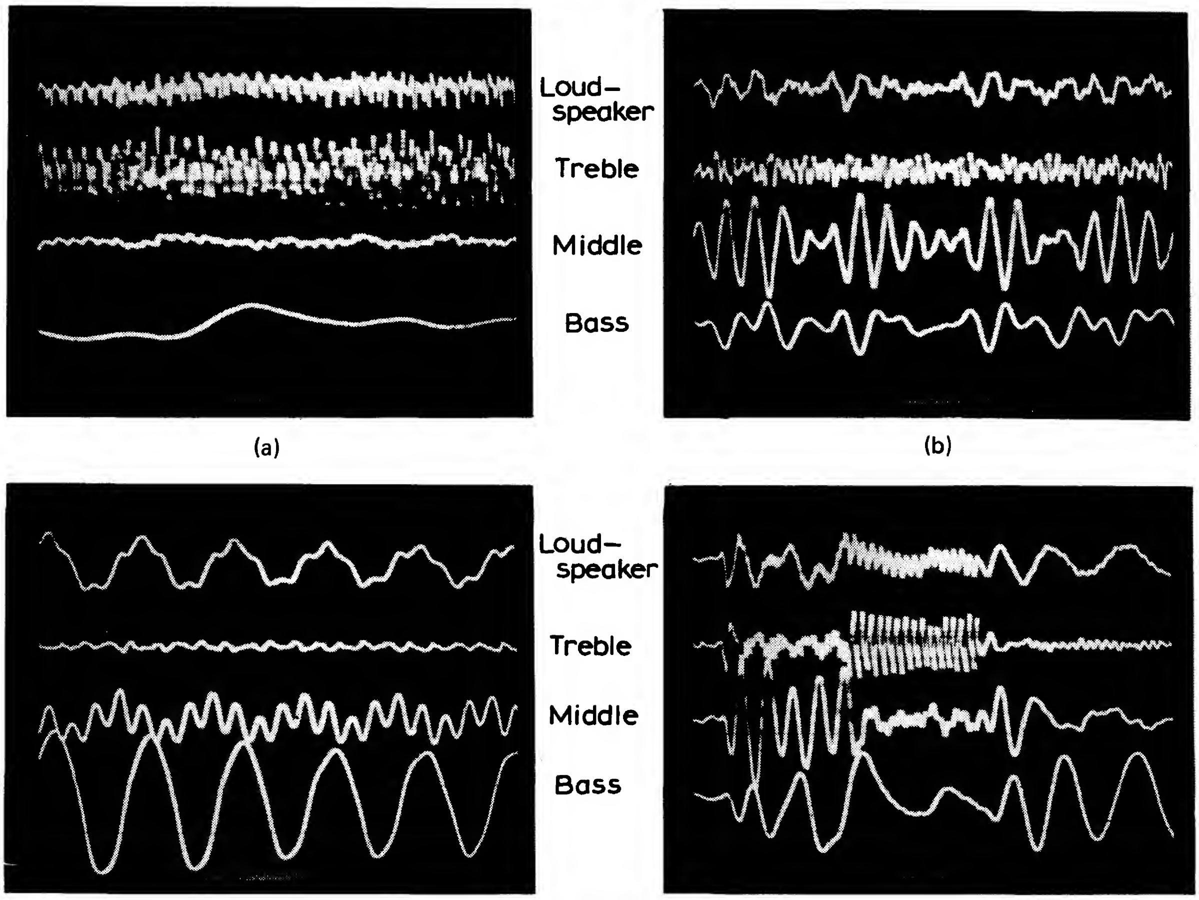


FIGURE 5. Output Voltage Frequency Response of the Filter Circuit.



(a) (b)

(c) (d)

FIGURE 6. Filter Circuit Waveforms.

Control Unit and D.C. Supplies

Figure 7 shows the circuit which operates the flashing lights according to the frequency ranges. Switch S4 controls the mains supply to the unit. When the a.c. mains power is on the gallium arsenide device LP4 lights. A smoothed d.c. supply for transistors VT1 to VT4 is obtained from a single phase bridge D1-4, resistor R30, diode D5 and capacitor C8. The ±10V power supply for the filter circuit is taken from zener diodes ZD7, ZD8 and capacitors C9 and C10. As described previously, the zero voltage crossing pulses are generated at the collector terminal of transistor VT1. These pulses turn on transistors VT2, VT3 and VT4 via base resistors R18, R20 and R22. When a voltage signal from the filter circuit appears at the input terminals, the corresponding thyristors Th1, Th2 or Th3 will turn on allowing pulses to be present at the respective gate of triacs Tr1, Tr2 or Tr6 which turn them and thus their lamps on. Pulse transformers T1, T2 and T3 are used only for electrical isolation. Zener diodes ZD3, ZD4 and ZD5 limit the thyristors gate voltages to 3.3V in the positive direction and to under 1V during the negative half cycles. Facilities are provided for 'by-passing' the psychedelic control by closing switches S1, S2 or S3 to allow the lamps to be used as normal lights. Note that the three triacs are best mounted on a common heat-sink, which is then at the supply line voltage, i.e. 240V.

A suggested component layout and printed circuit board is given for the complete circuit, i.e. filters, control, and power supplies, in Figure 8(a). Figure 9 is a full size board. The latter is also suitable for the modified version described later whose component layout is shown in Figure 8(b).

INTERCONNECTION

Unit Arrangement

The equipment ideally consists of two units. One unit to contain the control for the psychedelic lights, the filter circuits and the necessary power supply. (It is advisable, but not essential, that this unit is located near to the 13A power socket and amplifier.) The second unit to be mobile and consist of three colour lamps, the bass frequencies 'presented' by the red lamps, middle frequencies by the green lamps and treble frequencies by the blue lamps, say, mounted on a panel with a five core flexible cable attached to it. This unit could be hung on the wall, left on the table, or placed in some other convenient position.

The power control unit is capable of supplying three of these lamp units in parallel, each with its three coloured 100 watt lamps, i.e. a total power capability of 3 X 300 watts. Each lamp unit can have a six way terminal block for interconnecting as shown in later figures.

The equipment is suitable for either mono or stereo record playing. In the case of the stereo system, the lights will flash in accordance with the signals appearing at the terminals of one of the speakers. However, for stereo enthusiasts who wish to use two units, this interconnecting arrangement is given later.

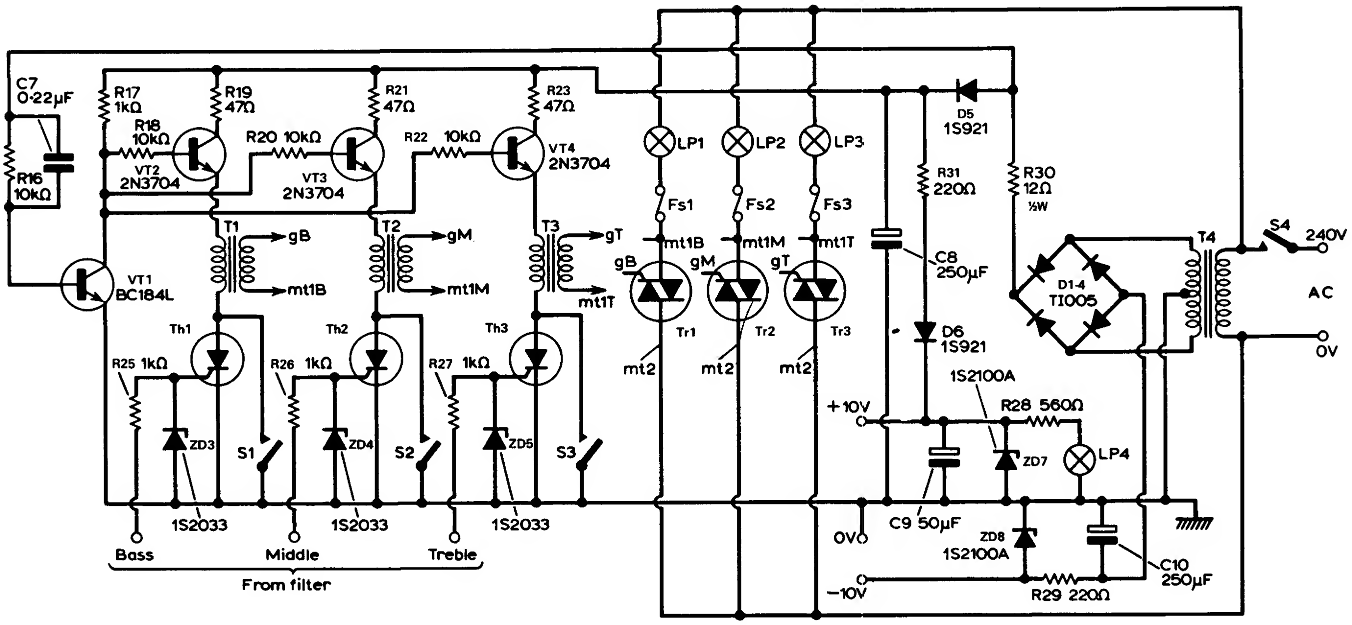
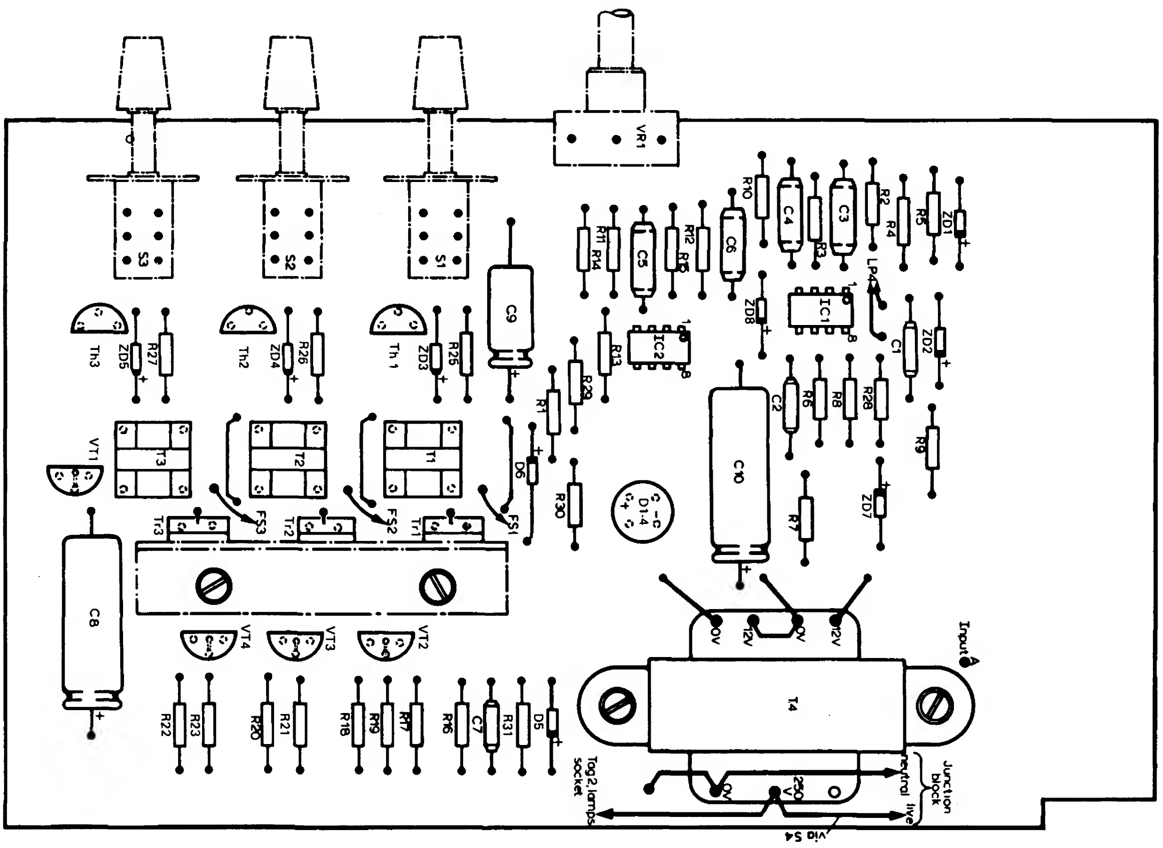
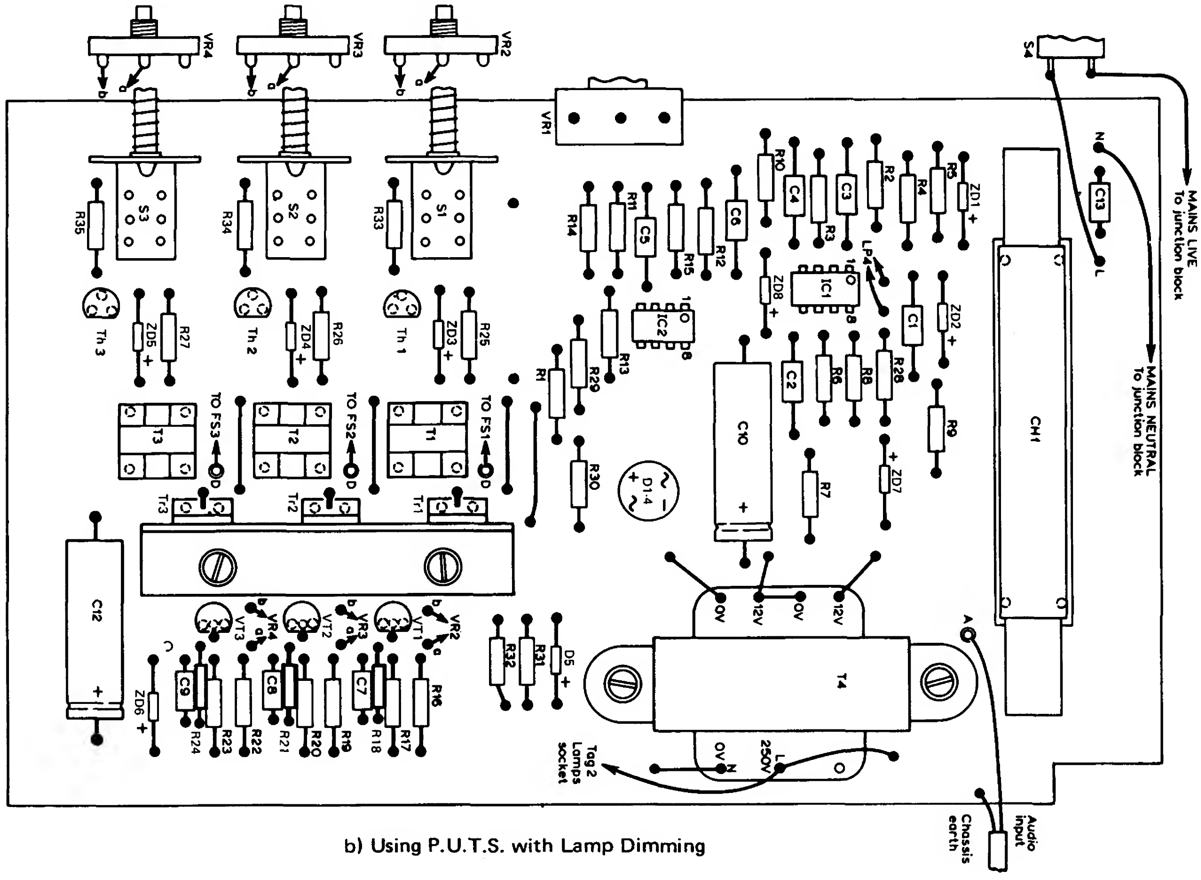

C7
0·22μF
R16
10kΩ
R17
1kΩ
R18
10kΩ
VT2
2N3704
R19
47Ω
R20 10kΩ
VT3
2N3704
R21
47Ω
R22 10kΩ
R23
47Ω
VT4
2N3704
VT1
BC184L
T1
gB
mt1B
T2
gM
mt1M
T3
gT
mt1T
Th1
Th2
Th3
R25 1kΩ
R26 1kΩ
R27 1kΩ
ZD3
ZD4
ZD5
S1
S2
S3
1S2033
1S2033
1S2033
Bass
Middle
Treble
From filter
LP1
LP2
LP3
Fs1
Fs2
Fs3
mt1B
mt1M
mt1T
gB
gM
gT
Tr1
Tr2
Tr3
mt2
mt2
mt2
D5
1S921
R31
220Ω
R30
12Ω
½W
C8
250μF
D6
1S921
D1-4
TI005
T4
S4
240V
AC
0V
1S2100A
R28 560Ω
+10V
ZD7
LP4
0V
C9 50μF
ZD8
1S2100A
C10
250μF
−10V
R29 220Ω

FIGURE 7. Zero Voltage Switching Control Unit.



VR1
S1
S2
S3
Th1
Th2
Th3
ZD1
ZD2
ZD3
ZD4
ZD5
ZD7
ZD8
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R25
R26
R27
R28
R29
R30
R31
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
IC1
IC2
LP4
D1-4
D5
D6
T1
T2
T3
Tr1
Tr2
Tr3
FS1
FS2
FS3
VT1
VT2
VT3
VT4
T4
0V
12V
250V
Input
Junction block
neutral
live
via S4
Tag 2, lamps socket

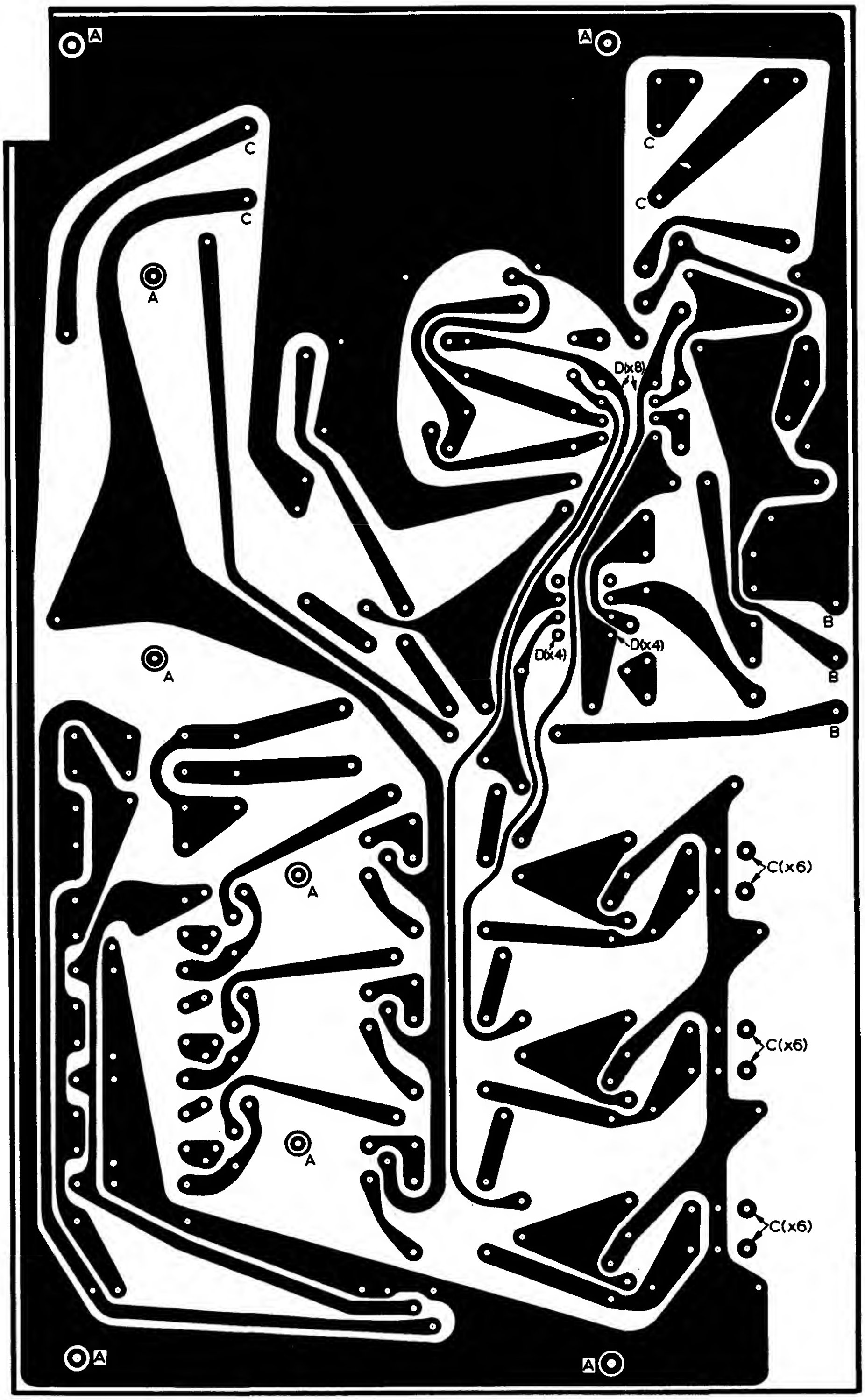
a) Using Transistors in Zero Crossing Section



VR1
VR2
VR3
VR4
S1
S2
S3
S4
R33
R34
R35
Th 1
Th 2
Th 3
ZD1
ZD2
ZD3
ZD4
ZD5
ZD6
ZD7
ZD8
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C12
C13
IC1
IC2
LP4
D1-4
D5
T1
T2
T3
Tr1
Tr2
Tr3
TO FS1
TO FS2
TO FS3
VT1
VT2
VT3
T4
0V
12V
250V
CH1
N
L
MAINS LIVE To junction block
MAINS NEUTRAL To junction block
Tag 2 Lamps socket
Audio input
Chassis earth

b) Using P.U.T.S. with Lamp Dimming

FIGURE 8. Complete Component Layout.


A
A
C
C
C
C
A
A
D(x8)
B
D(x4)
D(x4)
B
B
A
C(x6)
C(x6)
A
C(x6)
A
A

HOLE DATA

8 holes 'A' 5/32" dia

3 holes B 1.8mm dia

22 holes C 1.3mm dia

16 holes 'D' 1/32" dia

All other holes 1.0mm

FIGURE 9. Printed Circuit Board–Copper Side.

Mono. Connections

Figure 10 shows the connections for a single lamp unit. The five core cable is terminated with a plug suitable for connecting to the control unit. Connected thus, the three lamps will flash in accordance with frequency ranges present in the music.

Figure 11 shows a triple unit arrangement, where each unit is connected in the same way as shown in Figure 10. Here, however, the overall light level is increased and flexibility of lamp (100W each maximum) positioning is allowed, each lamp unit maintaining its three frequency range response.

Figure 12 gives another arrangement, using three lamp units, which is basically similar to that shown in Figure 11, except that here each lamp unit will flash according to one frequency range.

The interconnections between speaker, amplifier and control units are also straightforward. Simply connect a DIN plug on the leads from the speaker and plug this into the control unit. Then plug in the cable from the control unit, now terminated with a DIN plug, into an amplifier, e.g. as described in Volume II.[5] This should be done while all power is switched off. The amplifier should be connected via the control unit to a suitable loudspeaker before switching on.

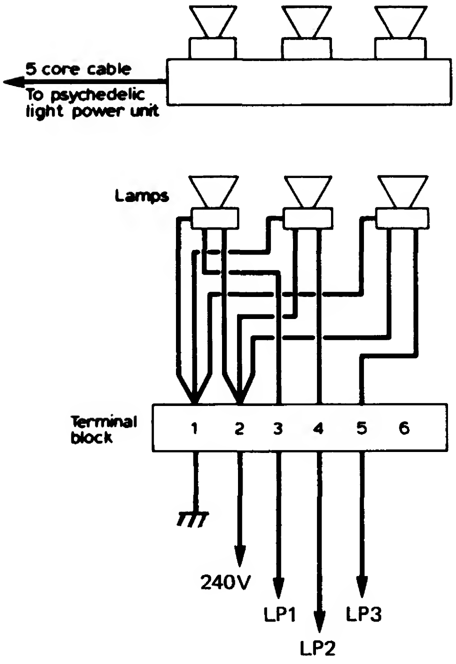

5 core cable
To psychedelic light power unit
Lamps
Terminal block
1
2
3
4
5
6
240V
LP1
LP2
LP3

FIGURE 10. Simplest Interconnection Arrangement.

Stereo Connections

The arrangement for a stereo system is also simple. Two control units and two lamp sets are required. A three

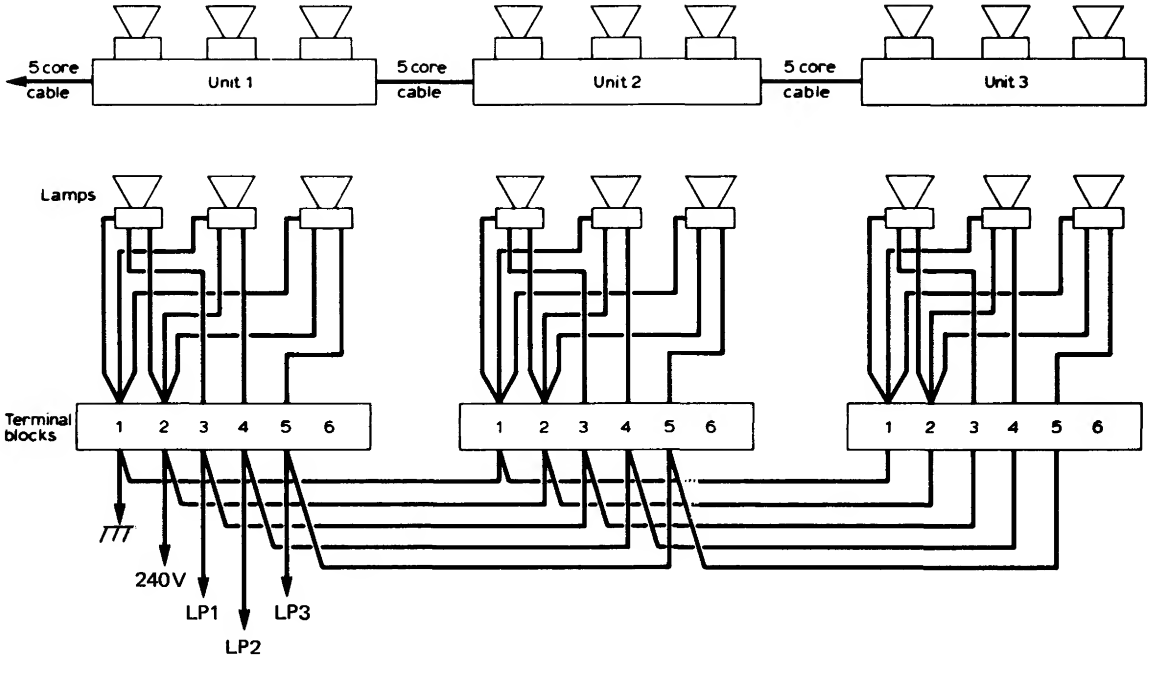

5 core cable
Unit 1
5 core cable
Unit 2
5 core cable
Unit 3
Lamps
Terminal blocks
1
2
3
4
5
6
1
2
3
4
5
6
1
2
3
4
5
6
240V
LP1
LP2
LP3

FIGURE 11. Three Lamp Banks Interconnection–One Control Unit.

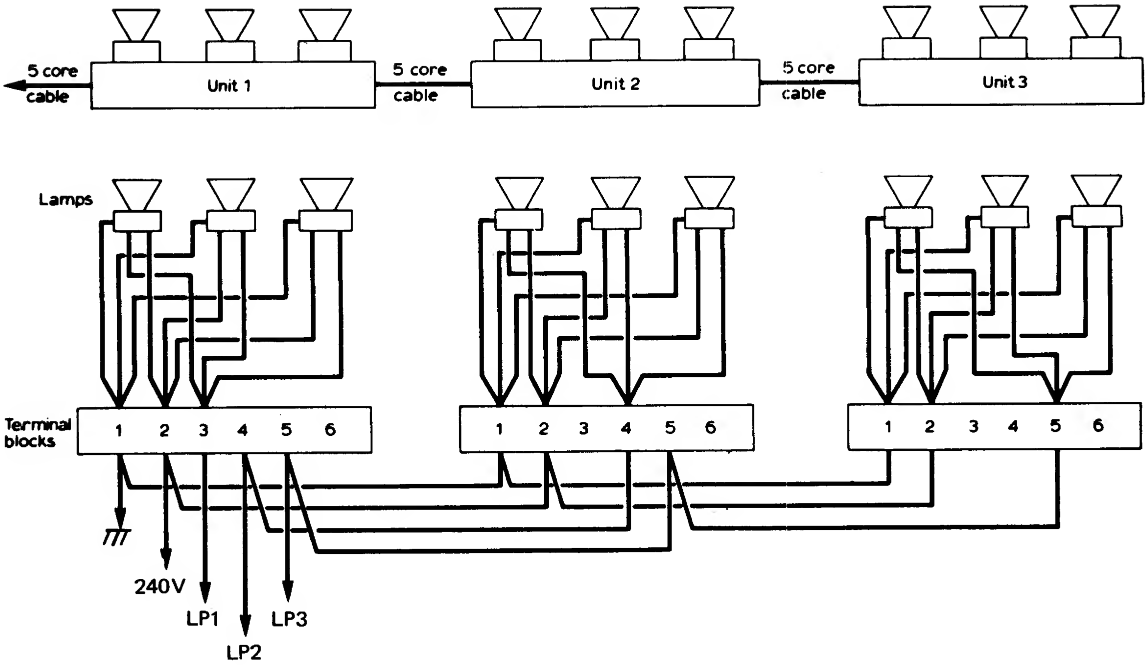


FIGURE 12. One Frequency Range Control of Three Lamp Banks.

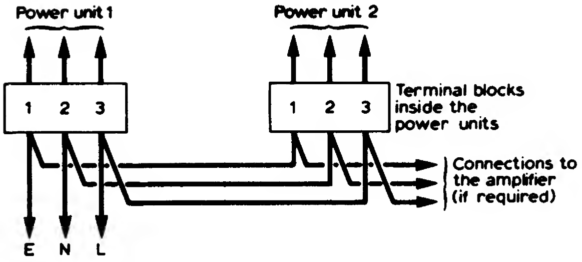

Power unit 1
Power unit 2
1 2 3
1 2 3
Terminal blocks inside the power units
Connections to the amplifier (if required)
E N L

FIGURE 13. Stereo System Two Control Unit Interconnection.

core cable from a 13A socket is connected to the terminal board of control unit 1. From the same terminal board the second three core cable is connected to control unit 2 as shown in Figure 13. The advantage of this arrangement is obvious, i.e. only one 13A plug is used for both control units. If required, the power supply to the amplifier can also be taken from the terminal board of control unit 2 as shown in Figure 13, thus achieving further simplification.

The interconnections between the control units, amplifier and speakers are similar to that described for the mono system but duplicated. Connect one speaker DIN plug into control unit 1 and then plug in the cable from it into the amplifier socket. This is repeated for the second speaker and control unit.

The effectiveness of the association of the light and music can be further improved if the lamps are placed near the speaker from which they are actuated. It is extremely effective when standing each lamp unit on or behind each speaker cabinet and projecting the lights up the walls behind.

LAMP DIMMING

Variation of the light intensity can readily be incorporated into the system by phase controlling the triacs.[2] One of the simplest ways of doing this is to use the programmable unijunction transistor relaxation oscillator circuit (as described in Chapter III). The oscillation can be synchronized to the mains by using the circuit shown in Figure 14. Here the output voltage from the bridge is clipped by the zener diode ZD6 so that only the lower section of the half sinewaves are applied to the p.u.t. circuit. The anode voltage of the p.u.t. drops to zero each time the line voltage crosses zero, so that capacitor C7 is discharged completely to zero every half cycle and charges again at the beginning of a next half cycle at the rate determined by the values of (R16 + VR2) and itself. By varying the resistance of the potentiometer VR2 the charge rate is varied so that the position of the pulses with respect to the supply voltage moves in time. (With the potentiometer in its minimum i.e. zero resistance position, the p.u.t. oscillator circuit may latch 'on'. This is not detrimental in this application, however, as a single pulse to fire the triac will be obtained before the latching occurs, and the circuit is reset each time the line voltage crosses zero).

Figure 15 shows typical triac gate voltage pulses and the corresponding voltage waveform across the load.

Circuit Modifications

In order to incorporate lamp dimming the filter circuit shown in Figure 4 and the power supply, and lamp control sections of Figure 7 remain the same. The modifications to the zero voltage switching system of Figure 7 are shown in Figure 16, i.e. the addition of zener diode ZD6 and resistor R32, and the replacement of the transistor circuits by the p.u.t. circuits.

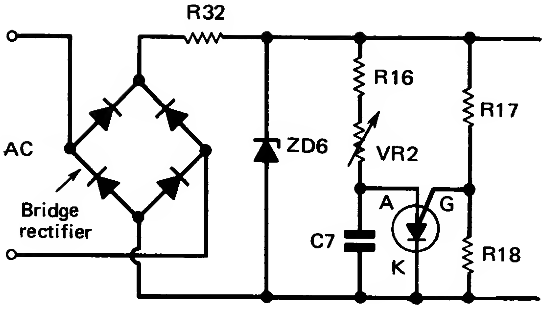

R32
AC
Bridge rectifier
ZD6
R16
VR2
R17
A
G
C7
K
R18

FIGURE 14. Mains Synchronization of P.U.T. Oscillator Circuit.

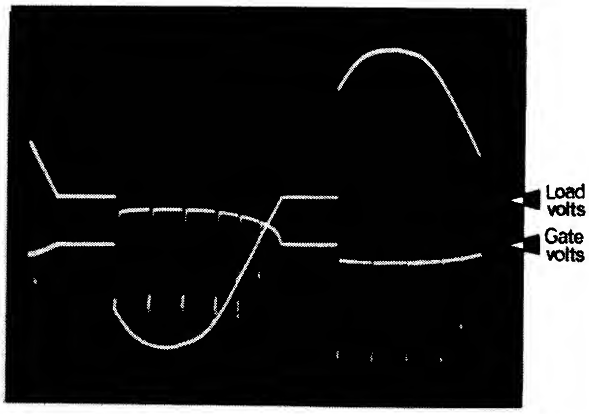


FIGURE 15. Lamp Dimming Waveforms.

The unit is suitable for either mono or stereo record playing in the same manner as described earlier. The flashing of the light can be controlled at various light intensity levels by means of the potentiometers corresponding to Bass, Middle and Treble frequencies. Closing of the switches S1, S2 and S3 here allow the psychedelic control to be 'by-passed' and the lamps to be used as ordinary lamp dimmers. As mentioned a possible p.c.b. is shown in Figure 8(b) – the copper side of the p.c.b. shown in Figure 9 being also suitable for this version.

Radio Interference Suppression

Radio frequency interference problems caused by the introduction of phase control can become acute and difficult to suppress to an acceptable level. Many circuits and equipment such as radios, hi-fi amplifiers, etc. are sensitive to these voltage transients and the results are generally unpleasant noises in the speakers and/or causing malfunction of the semi-conductor circuits. Each time a phase controlled triac fires in a mainly resistive load, such as lamps, the load current rises in less than a few microseconds from the zero value to its maximum. Thus some kind of r.f.i. suppression is really required if lamp dimming is incorporated into the system. The suppression filter used in this system is very simple, inexpensive and quite effective. It is suitable for total loads up to 900W, and consists of one bifilar wound ferrite core filter choke CH1 and 0.1μF capacitor, C13 added to the input of the circuit, as shown in Figure 16. The normal symmetrical currents generate magnetic fields which are self cancelling. However, asymmetrical currents, caused by radio frequency interference, are attenuated.

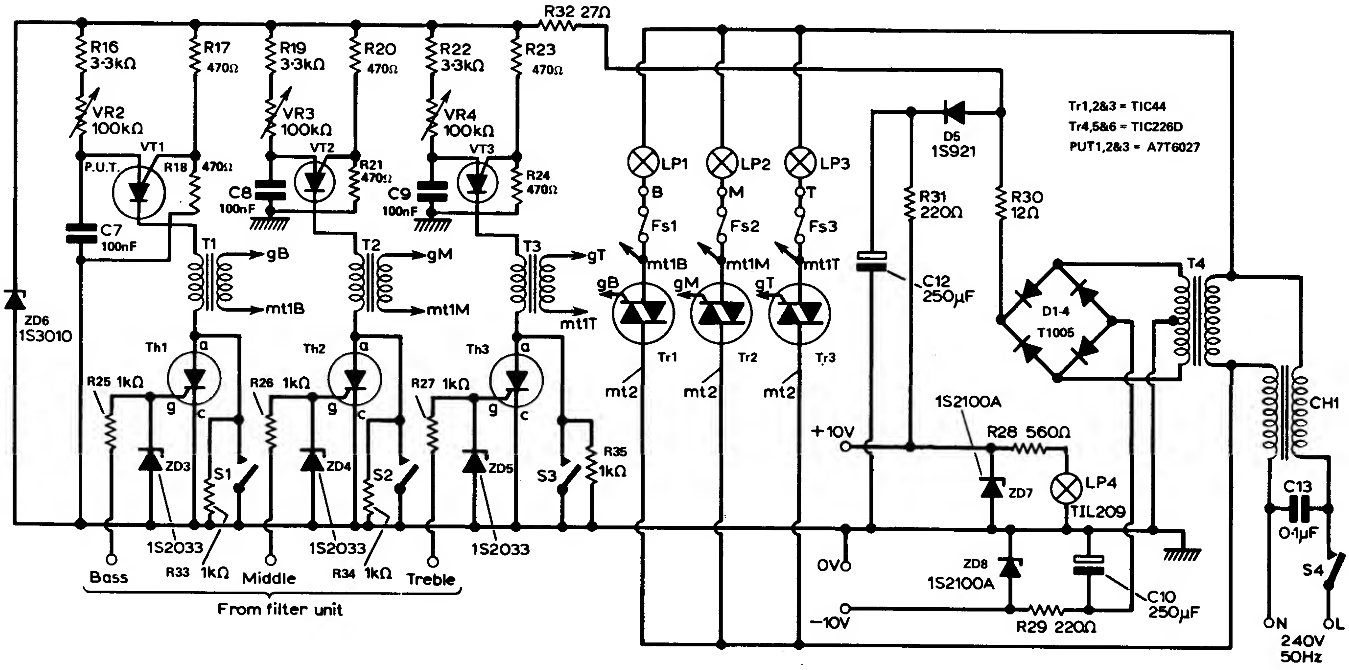

R32 27Ω
R16 3·3kΩ
R17 470Ω
R19 3·3kΩ
R20 470Ω
R22 3·3kΩ
R23 470Ω
VR2 100kΩ
VR3 100kΩ
VR4 100kΩ
VT1
VT2
VT3
P.U.T.
R18 470Ω
R21 470Ω
R24 470Ω
C7 100nF
C8 100nF
C9 100nF
T1
T2
T3
gB
mt1B
gM
mt1M
gT
mt1T
ZD6 1S3010
Th1
Th2
Th3
a
g
c
R25 1kΩ
R26 1kΩ
R27 1kΩ
ZD3
ZD4
ZD5
S1
S2
S3
R35 1kΩ
1S2033
1S2033
1S2033
Bass
R33 1kΩ
Middle
R34 1kΩ
Treble
From filter unit
LP1
LP2
LP3
B
M
T
Fs1
Fs2
Fs3
Tr1
Tr2
Tr3
mt2
Tr1,2&3 = TIC44
Tr4,5&6 = TIC226D
PUT1,2&3 = A7T6027
D5 1S921
R31 220Ω
R30 12Ω
C12 250μF
D1-4 T1005
T4
1S2100A
R28 560Ω
+10V
ZD7
LP4 TIL209
0V
ZD8 1S2100A
–10V
R29 220Ω
C10 250μF
CH1
C13 0·1μF
S4
N
L
240V 50Hz

FIGURE 16. Modifications to Control Circuit to Incorporate Lamp Dimming.

REFERENCES

1. *Semiconductor Circuit Design*, Vol. I, Texas Instruments Ltd., Chapters I, II & III, April 1972.

2. *Semiconductor Circuit Design*, Vol. I, Texas Instruments Ltd., pp. 1-7, April 1972.

3. *Semiconductor Circuit Design*, Texas Instruments Ltd., Vol. I, pp. 22-28, April 1972, and Vol. III, pp. 107-112, April 1974.

4. *Semiconductor Circuit Design*, Vol. II, Texas Instruments Ltd., pp. 138-139, April 1973.

5. *Semiconductor Circuit Design*, Vol. II, Texas Instruments Ltd., pp. 159-172, April 1973.

SECTION 2.

DIGITAL PROCESSING TECHNIQUES

VIII MICROPROCESSORS

by
Peter van Cuylenburg

The heart of any data processing system is the central processing unit, c.p.u. This is the portion where all calculations and logic operations are performed. The advent of a compact block of electronic functions which is sufficient to execute the required actions has caused a revolution in this and other areas of electronics and led to the introduction of a new word, i.e. microprocessors. The concept, though only developed in the last few years, has already produced a diversity of implementations. Microprocessors can be 4 or 8 bit 'one chip' machines (with promises of 16 bit word lengths to come); expandable 4 (and 2) bit slice devices; large, but slow 'number-crunching' chips; or built from an 'off-the-shelf' logic family. The different types of processor are examined in detail later in this chapter.

MICRO-COMPUTER CONCEPTS

Microcomputers have evolved as this ability of semiconductor manufacturers to put more and more logic into a given chip area has increased. It is now possible to incorporate in a single chip most of the logic required to produce an arithmetic logic unit (a.l.u.) similar to those used in minicomputers and hitherto requiring several hundreds of t.t.l. integrated circuits. This a.l.u., with the necessary control circuitry, becomes the c.p.u. or microprocessor. A microcomputer is merely a collection of circuits forming a complete system, of which the microprocessor is the nucleus. The quantity and nature of the support circuits in the microcomputer vary with types of microprocessor and applications, but will typically include program memory, data memory, input/output devices and clock generators. Figure 1 shows these elements connected together in a typical configuration. To a certain extent the support circuits are a separate, less complex subject since they are usually existing programmable read only memories (p.r.o.m.s), random access memories (r.a.m.s), latches etc., or developments thereof to suit a particular microprocessor. It is the diversity of microprocessor types which is a subject in itself.

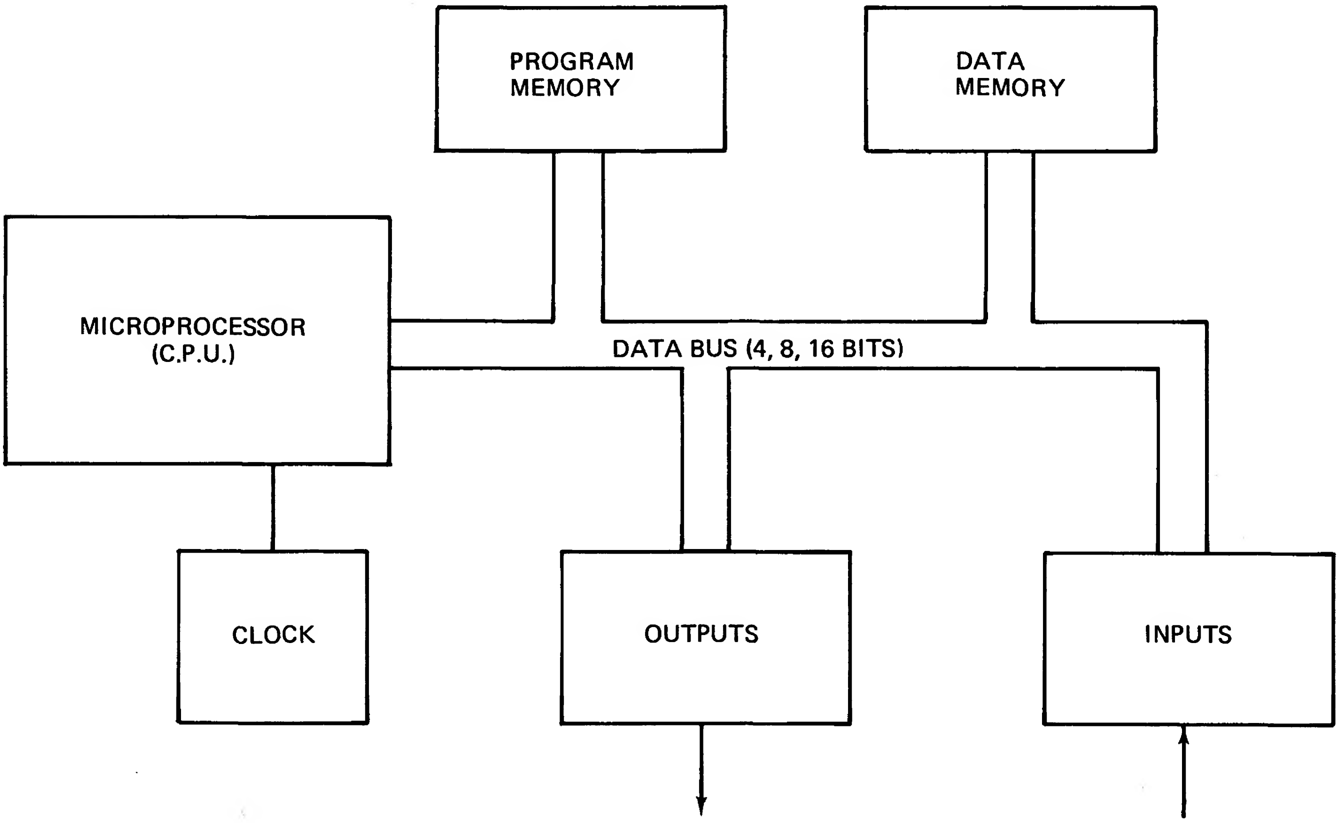


FIGURE 1. Typical Microcomputer Configuration

MICRO-PROCESSORS

Microprocessors differ in both software and hardware respects. If the microprocessor has a fixed instruction set it must either conform with an existing software system of compilers, assemblers, editors etc., or have its own system produced. Alternatively, it may be microprogrammable, in which case it can be used to emulate any existing microcomputer and therefore use that microcomputers software.

Software Considerations

The diagram of microprocessor programming levels in Figure 2 shows all the levels of operation of a conventional microprocessor. A program written in a high level language is compiled (either in a host-computer or a microcomputer development system) into a machine code listing of binary instructions. In minicomputer terminology this would be called an object code; in microcomputer terminology these instructions are now being referred to as macro-instructions to distinguish them from the lower level of micro-instructions. Alternatively to the high level language/compiler approach the program may be written in lower level assembly language and assembled (again by host computer or microcomputer development system) into the binary instruction listing. This latter approach gives a more efficient binary program but requires more programming skill and longer writing time.

Thus there is a list of binary instruction words which is held in the microcomputers program memory, usually a p.r.o.m.. These instruction words are usually 8 bits wide, but may be 4 or 16 bits in certain systems. In an 8 bit system it is common to have macro-instructions consisting of more than one 8 bit byte, where one byte is the address of an operand referred to in the instruction. Each of these binary instructions is used to address a starting location in the micro-instruction r.o.m. This r.o.m. is driven by the sequencer so that a given 8 bit macro-instruction produces a fixed sequence of n micro-instruction words. The number and width of the words vary depending on the power and flexibility of the a.l.u. contained in the microprocessor and the complexity of the macro-instruction being executed. The macro-instruction decoder circuit, which may be either a programmable logic array (p.l.a.) or a r.o.m. decodes the micro-instructions into logic conditioning outputs which condition the various elements of the a.l.u. to carry out the required operation.

There are of course many ways of partitioning the logic which implements all these functions. The architecture may be 'sliced' vertically to give 2- or 4-bit slices or horizontally to give 'microprogrammable' c.p.u.s. The decision on where to slice the architecture will depend on the technology used to fabricate the microprocessor, and on the flexibility and performance required.

Microprogramming

The relationship between a macro-instruction in the program r.o.m. and the corresponding function carried out by the a.l.u. is governed by the micro-instruction r.o.m. In earlier large scale integration (l.s.i.) microprocessors the micro-instruction r.o.m. was integrated with the sequencer and decoder onto the c.p.u. chip, and was pre-programmed with a standard fixed micro-instruction set. This meant that only software designed for that micro-instruction set could be used, and has led to the development of complete software back-up systems for m.o.s. microprocessors. Later bipolar microprocessors have sliced across the architecture and produced c.p.u. chips which require external p.r.o.m.s for the micro-instruction r.o.m. This has opened up a new dimension for users because the micro-instruction r.o.m. can be microprogrammed by one user to fit any existing software and therefore emulate any existing machine. Some later m.o.s. c.p.u.s offer mask microprogrammability, where the customer's microprogram is incorporated into the c.p.u. during the manufacturing processes, but this does not have the flexibility of the external microprogram r.o.m. and is only suitable for volume users.

Types

There are now four main groups of microprocessor types representing different approaches to the partitioning of the microcomputer logic with different technologies. The four groups are as follows:–

Group 1: The n-channel m.o.s. 'traditional' type of microprocessor with sequencer, micro-instruction r.o.m. and decoder all included on the c.p.u. chip. This type of microprocessor, of which the TMS8080 is an example, usually operates with an 8 bit data bus and requires minimum peripheral circuitry to produce a microcomputer system. Typically external r.a.m. and r.o.m. chips are required for data and program memory respectively, and a number of data input/output ports. Main differences between microprocessors in this group are interrupt capability, memory accessing and the degree of compatibility between the microprocessor and its support circuitry. The machine cycle time for microprocessors in this group is about 2μs although some early devices have cycle times up to 12μs. Figure 3 shows the typical organisation of a Group 1 microprocessor.

Group 2: The 2- or 4-bit slice microprocessor elements use bipolar technologies and 'slice' the architecture of the Group 1 microprocessors both vertically and horizontally. This produces fast 2 or 4-bit a.l.u.s with most of the registers of the Group 1 type, but requiring a separate microprogram r.o.m. and sequencer. As mentioned earlier, the external microprogram r.o.m. can be programmed to convert any existing binary program into the micro instructions used by the c.p.u. An example of the 4 bit slice microprocessor, which is discussed later in the chapter, is the SBP0400. This device is made with integrated injection logic (i.i.l.), a technology explained in a later chapter.[1] The use of i.i.l. has made possible the production

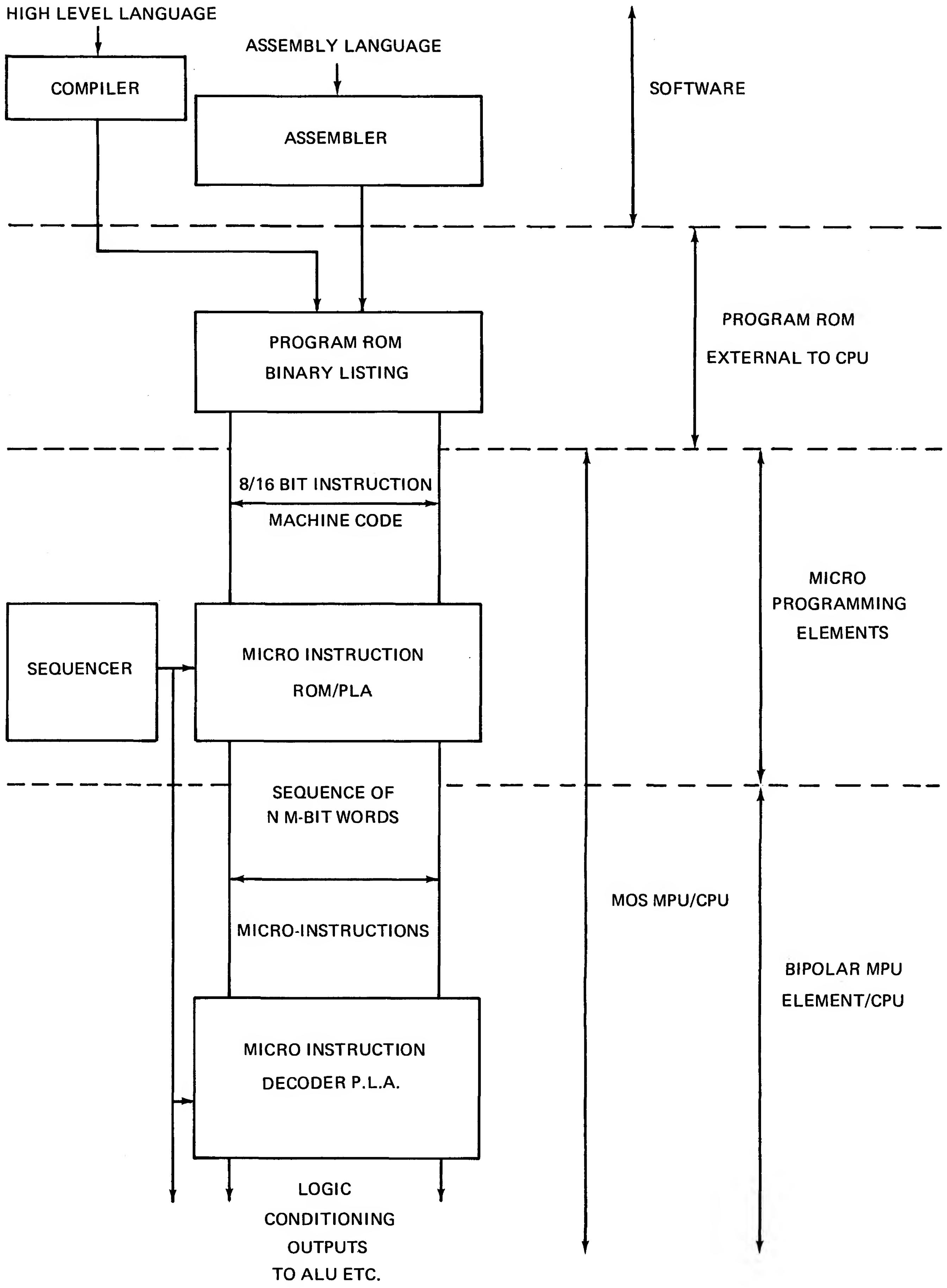

HIGH LEVEL LANGUAGE
COMPILER
ASSEMBLY LANGUAGE
ASSEMBLER
SOFTWARE
PROGRAM ROM
BINARY LISTING
PROGRAM ROM
EXTERNAL TO CPU
8/16 BIT INSTRUCTION
MACHINE CODE
MICRO
PROGRAMMING
ELEMENTS
SEQUENCER
MICRO INSTRUCTION
ROM/PLA
SEQUENCE OF
N M-BIT WORDS
MICRO-INSTRUCTIONS
MOS MPU/CPU
BIPOLAR MPU
ELEMENT/CPU
MICRO INSTRUCTION
DECODER P.L.A.
LOGIC
CONDITIONING
OUTPUTS
TO ALU ETC.

FIGURE 2. Microprocessor Programming Levels

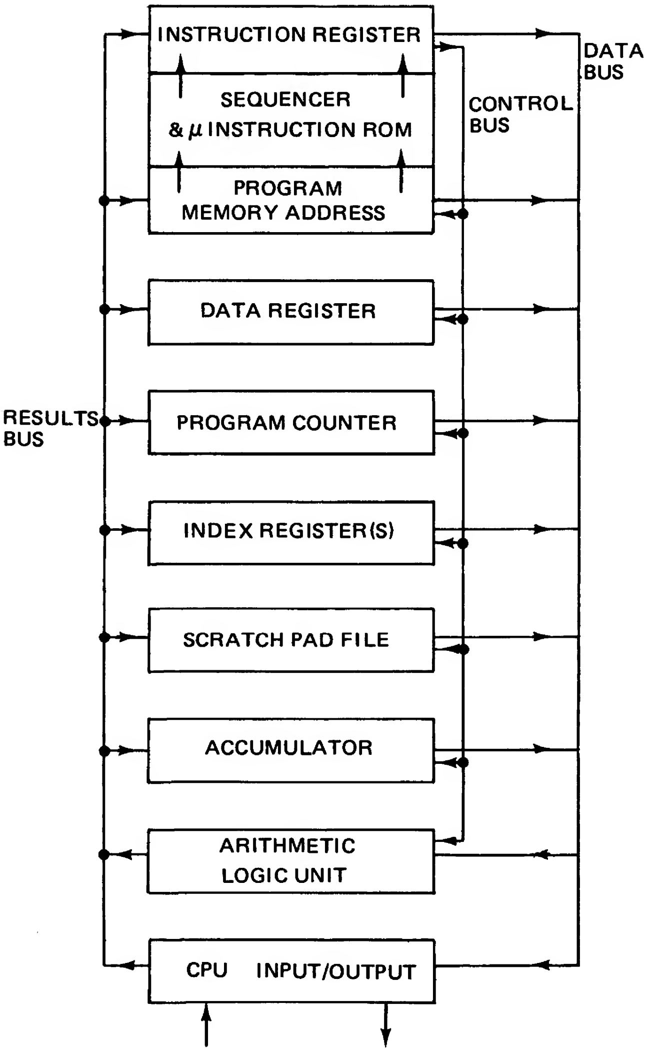


FIGURE 3. Typical Organisation of a Group Microprocessor

of a fast microprocessor element with low power dissipation and a comprehensive repertoire of 459 one-clock micro-instructions. The microprogramming technique can be used to make the device emulate any existing 4, 8 or 16 bit microprocessor, and to use the software back-up applicable to that microprocessor.

Group 3: This group of microprocessor types consists of those which are made up from existing 'off-the-shelf' logic families, primarily from Schottky t.t.l. devices which offer extremely high speeds of operation. In fact it is usually a complete microcomputer system which is made up rather than a microprocessor, and the boundaries between the c.p.u. and the rest of the system become less well-defined. The 'raison d'etre' of the Schottky chip set microcomputers is of course, their speed. This is considerably better than existing m.o.s. and bipolar microprocessors, although the i.i.l. technology has the potential of approaching Schottky speeds. The other great advantage of this type of microprocessor is that it can be designed specifically for a particular purpose and can therefore offer an economy of functions unattainable by a general purpose microprocessor. A Schottky microcomputer is described in the next chapter.

Group 4: This final group of 'microprocessor' types covers single-chip devices where the program r.o.m., data r.a.m. and input/output circuitry are included on the same chip as the c.p.u. Obviously these are fixed program devices because the user's macro-instruction program is mask-programmed into the device during manufacture. A degree of mask-microprogrammability is also offered, and in the case of the TMS1000 described later, the same gate mask also defines the output formating logic, enabling the user to specify any 8 bit output code. Because of the mask programming the use of this type of microcomputer is restricted to volume (>5k per year) production systems. In this type of application, for example intelligent terminals, flow metering systems, printer or copier control, vending machines–in fact all types of industrial control systems–the single chip microcomputer provides a far more economic solution than the use of a general purpose microprocessor whose capability would not be fully utilised. The cost of Group 4 type would be an order of magnitude lower than the cost of a Group 1 type of microcomputer system.

Choice

The choice of microprocessor type for a particular application follows the traditional considerations of performance (cycle time) flexibility (microprogrammable or not), number of chips, cost, development time and expertise required etc. For a high volume production requirement the one-chip microcomputer is the obvious choice on a cost basis, unless the greater computing power of a multi-chip system is necessary. If the flexibility of a microprogrammable system is necessary then the 4 bit slice approach is virtually mandatory. Where size, i.e. minimum chip count, is important the m.o.s. Group 1 type of microprocessor is the best choice, but where high speed is the overriding requirement the Schottky chip set is the only solution.

Table 1 gives a comparison of some of the important parameters of each of the four groups of microprocessor types.

Table 1. Parameter Comparison Microprocessor Types

	Schottky t.t.l.	**SN74 S481**	**SBP 0400**	**TMS 8080**	**TMS 1000**
Description	Chip Set	4-Bit Slice Super A.L.U.	4-Bit Slice Processor Element	Fixed Instructn Set μP	One Chip Micro-computer
Size Bits	8	4	4	8	4
Speed ns	6,150	70	700	2,000	15,000
Instructions	100	60+	459	80+	43
Technology	S.t.t.l.	S.t.t.l.	i^2.l.	n.m.o.s.	p.m.o.s.
Expandable	–	Yes	Yes	No	Operates Serially on 4-Bit Bytes

A 4-BIT SLICE MICROPROCESSOR ELEMENT

Organisation

The organisation of a device such as the SBP0400 is shown in Figure 4. A key feature of this device, which is apparent from the organisation diagram, is the full parallel access to all main highways: the DATA-IN and DATA-OUT BUSES, the ADDRESS-OUT BUS and the 9-Bit OPERATION SELECT WORD (microinstruction) bus. This coincides with the typical microcomputer organisation which has results, control and data buses, and avoids the necessity for multiplexing data into and out of the device. The major elements of the device are the operation select word transformation p.l.a. and the associated pipeline register, the two 4-bit working registers, the 8-word by 4-bit register file, and a.l.u., and the internal bus multiplexers. Table 2 gives a functional description of all inputs and outputs.

Data Registers: All registers on the device are implemented with edge-triggered or master-slave D-type static latches and data is made available on all register outputs at the positive going clock edge. The working register (w.r.) is a 4-bit master-slave register, which functions as an accumulator during iterative arithmetic operations or as a temporary holding register for intermediate operands. It acts as an operand source for the a.l.u., via the B multiplexer ('B' MUX) port, and for the ADDRESS-OUT BUS. The w.r. can be driven from either the DATA-IN or DATA-OUT BUS. Shifting of the w.r. data is accomplished by using the data-out multiplexer ('DO' MUX) as shown in Figure 5. At each end of the w.r. there are bi-directional serial input outputs ($\overline{\text{WRLFT}}$ and $\overline{\text{WRRT}}$) which are used for shifting the data around cascaded devices. A second 4-bit register is known as the extended working register. This is implemented in the same way as the w.r. and used as a temporary holding register during address deviations and as a w.r. extension during operations where double-length operands are present. It acts as an operand source for the a.l.u. (via the B multiplexer port) and for the ADDRESS-OUT BUS, and can be driven from the DATA-OUT BUS. Functional storage is provided by the register file (RF0-RF7). This is a set of 8 by 4-bit D-type parallel input/output registers, which are individually addressable under control of the operation register. The register file is

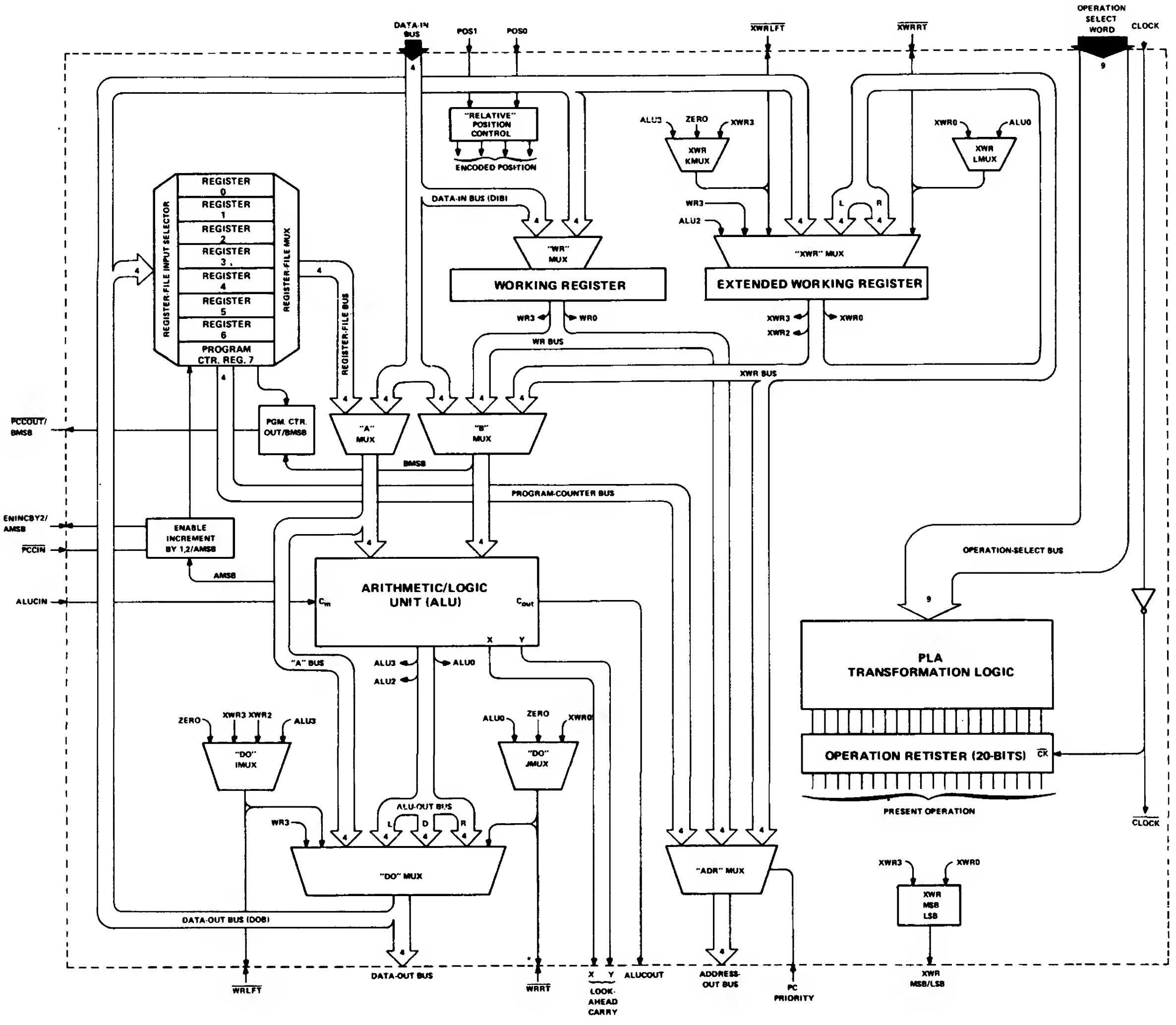

DATA-IN BUS
POS1
POS0
XWRLFT
XWRRT
OPERATION SELECT WORD
CLOCK
4
9
"RELATIVE" POSITION CONTROL
ENCODED POSITION
DATA-IN BUS (DIB)
ALU3
ZERO
XWR3
XWR KMUX
XWR0
ALU0
XWR LMUX
WR3
ALU2
L
R
"WR" MUX
WORKING REGISTER
"XWR" MUX
EXTENDED WORKING REGISTER
WR3
WR0
WR BUS
XWR3
XWR2
XWR0
XWR BUS
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
PROGRAM CTR. REG. 7
REGISTER-FILE INPUT SELECTOR
REGISTER-FILE MUX
REGISTER-FILE BUS
PCCOUT/ BMSB
PGM. CTR. OUT/BMSB
"A" MUX
"B" MUX
BMSB
PROGRAM-COUNTER BUS
ENINCBY2/ AMSB
PCCIN
ENABLE INCREMENT BY 1,2/AMSB
AMSB
ALUCIN
ARITHMETIC/LOGIC UNIT (ALU)
C_{in}
C_{out}
X
Y
"A" BUS
ALU3
ALU0
ALU2
OPERATION-SELECT BUS
PLA TRANSFORMATION LOGIC
OPERATION RETISTER (20-BITS)
CK
PRESENT OPERATION
CLOCK
ZERO
XWR3 XWR2
ALU3
"DO" IMUX
ALU0
ZERO
XWR0
"DO" JMUX
ALU-OUT BUS
WR3
L
D
R
"DO" MUX
"ADR" MUX
XWR3
XWR0
XWR MSB LSB
DATA-OUT BUS (DOB)
WRLFT
DATA-OUT BUS
WRRT
X Y
LOOK-AHEAD CARRY
ALUCOUT
ADDRESS-OUT BUS
PC PRIORITY
XWR MSB/LSB

FIGURE 4. Organisation of the SPB0400 4-Bit Microprocessor

Table 2. Functional Description of Inputs and Outputs

PIN NUMBER	PIN NAME	PIN FUNCTION	INPUT, OUTPUT, OR INPUT/OUTPUT
1	D1	2-bit, "D" field of the Operation-Select Word.	Input
2	D0		Input
3	S2	3-bit, "S" field of the Operation-Select Word designates, in general, a particular RF as an operand source/destination.	Input
4	S1		Input
5	S0		Input
6	$\overline{\text{XWRLFT}}$	Bidirectional I/O, low active, shift accommodation for the XWR. Receives double-precision right-shift data; outputs double-precision left-shift data. Becomes XWRLFT (high active) internally.	Bidirectional Input/output
7	$\overline{\text{XWRRT}}$	Bidirectional I/O, low active, shift accommodation. Receives double-precision left-shift data; outputs double precision right-shift data. Becomes XWRRT (high active) internally.	Bidirectional Input/output
8	XWR MSB/LSB	MSB of the XWR if in the most-significant 4-bit-slice position (MSP) and LSB if in the least-significant 4-bit slice position (LSP)	Output
9	$\overline{\text{WRRT}}$	Bidirectional I/O, low active, shift accommodation for ALU output data. Receives left-shift data. Outputs right-shift data. Becomes WRRT (high active) internally.	Bidirectional Input/output
10	$\overline{\text{WRLFT}}$	Bidirectional I/O, low active, shift accommodation for ALU output data. Receives right-shift data; outputs left-shift data. Becomes WRLFT (high active) internally.	Bidirectional Input/output
11	ALUCIN	Receives, high active, ALU ripple carry-in data.	Input
12	DOB0	4-bit, parallel, high active, data-out bus. (DOB3 → DOB0)	Output
13	DOB1		Output
14	DOB2		Output
15	DOB3		Output
16	DIB3	4-bit, parallel, high active, data-in bus. (DIB3 → DIB0)	Input
17	DIB2		Input
24	DIB1		Input
25	DIB0		Input
18	$\overline{\text{PCCIN}}$	In all position, directs the program counter to increment by 1 or 2, depending on the level applied to ENINCBY2, on the next low-to-high clock transition.	Input
19	$\overline{\text{PCCOUT}}$/ BMSB	In any position but MSP, $\overline{\text{PCCOUT}}$ is the program counter output applied to the next more significant package $\overline{\text{PCCIN}}$. In the MSP, outputs the MSB of the "B" bus.	Output
20	GND	Common or ground terminal	Supply common
21	POS0	Directs internal and input/output end-conditions required to define the relative position of each SBP0400 when a number is cascaded to implement > 4-bit word lengths. See double-precision shift data flow.	Input
22	POS1		Input
23	ENINCBY2/ AMSB	In the least-significant 4-bit slice position (LSP), ENINCBY2 = H in conjunction with $\overline{\text{PCCIN}}$ = L directs the PROGRAM COUNTER to increment by a displacement of 2 on the next clock. In the most-significant 4-bit slice position (MSP), outputs the MSB of the "A" BUS.	Bidirectional Input/output (LSP) (MSP)
26	CLOCK	Clock	Input
27	INJECTOR 1	One of two supply current sources. Connect to pin 40.	Supply input
28	AOB3	4-bit, parallel, high active, address-out bus (AOB3 → AOB0)	Output
29	AOB2		Output
31	AOB1		Output
32	AOB0		Output
30	PC PRIORITY	Selects program counter to the address-out bus (high active). Overrides internal direction of address-out bus.	Input
33	X	ALU carry-propagate	Output
34	Y	ALU carry-generate	Output
35	ALUCOUT	Outputs, high active, ALU ripple carry-out data	Output
36	OP3	This 4-bit, "OP" field of the Operation-Select Word designates in general, 1 of 16 ALU functions.	Input
37	OP2		Input
38	OP1		Input
39	OP0		Input
40	INJECTOR 2	One of two supply current sources. Connect to pin 27.	Supply input

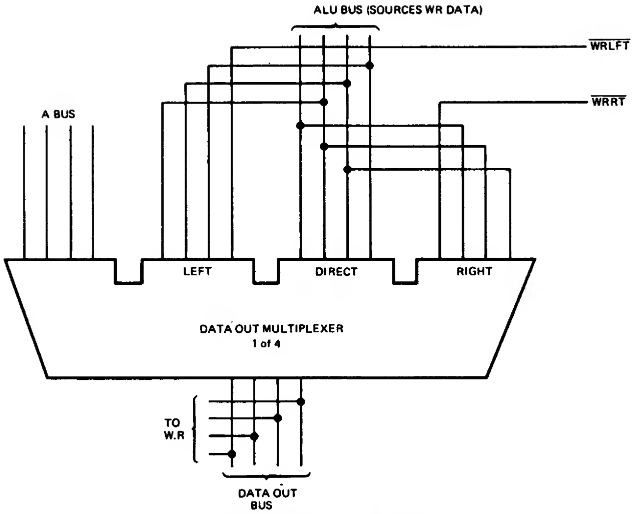

ALU BUS (SOURCES WR DATA)
WRLFT
WRRT
A BUS
LEFT
DIRECT
RIGHT
DATA OUT MULTIPLEXER
1 of 4
TO W.R
DATA OUT BUS

FIGURE 5. Data-Out Multiplexer

used for temporary storage of source data needed in current processor routines. Data from the register file is available to the DATA-OUT BUS, and w.r. either via or bypassing the a.l.u.. The RF7 location of the register file has the added capability of performing as a program counter (p.c.). In addition to the fully presetable capability of the other registers the p.c. can be incremented either by 1 or 2 at the positive clock edge. A 'low' at the $\overline{\text{PCCIN}}$ input enables incrementing, while a 'low' or 'high' at the ENINCBY2/AMSB input makes the increment 1 or 2 respectively. The p.c. register RF7 has an additional special capability in that there is a 4-bit wide highway directly connecting it to the address-out multiplexer ('ADR' MUX). When a P. C. PRIORITY input is applied to the address multiplexer the contents of the p.c. are forced onto the ADDRESS-OUTPUT BUS regardless of any other instruction being carried out.

The A.L.U.: The 4-bit parallel binary a.l.u. provides the arithmetic/boolean or operand combination/modification mechanism. According to the current instruction, the a.l.u. will perform either one of eight arithmetic or one of eight logical operations on either or both of the two operands sourced through the A ('A' MUX) and B multiplexers. The operations and the sources and destinations of the operands are all defined by the OP and S bits of the operation select word. The A input port of the a.l.u. has access to the DATA-IN BUS and register file while the B input port has access to the DATA-IN BUS and the working and extended working registers. The a.l.u. has both ripple carry in (ALUCIN) and ripple carry out (ALUCOUT) connections, as well as X and Y carry-generate and carry-propagate outputs. When the X and Y outputs are used in conjunction with SN74S182 look-ahead carry generators the a.l.u. add/subtract times are significantly improved over the times when only ripple-carry techniques are employed. Only one 'S182 is required to provide look-ahead carry generation over a cascaded system of from 2 to 4 SBP0400s, as shown in Figure 6. A second level of look-ahead carry generation can be employed for a system of up to 64 bits.

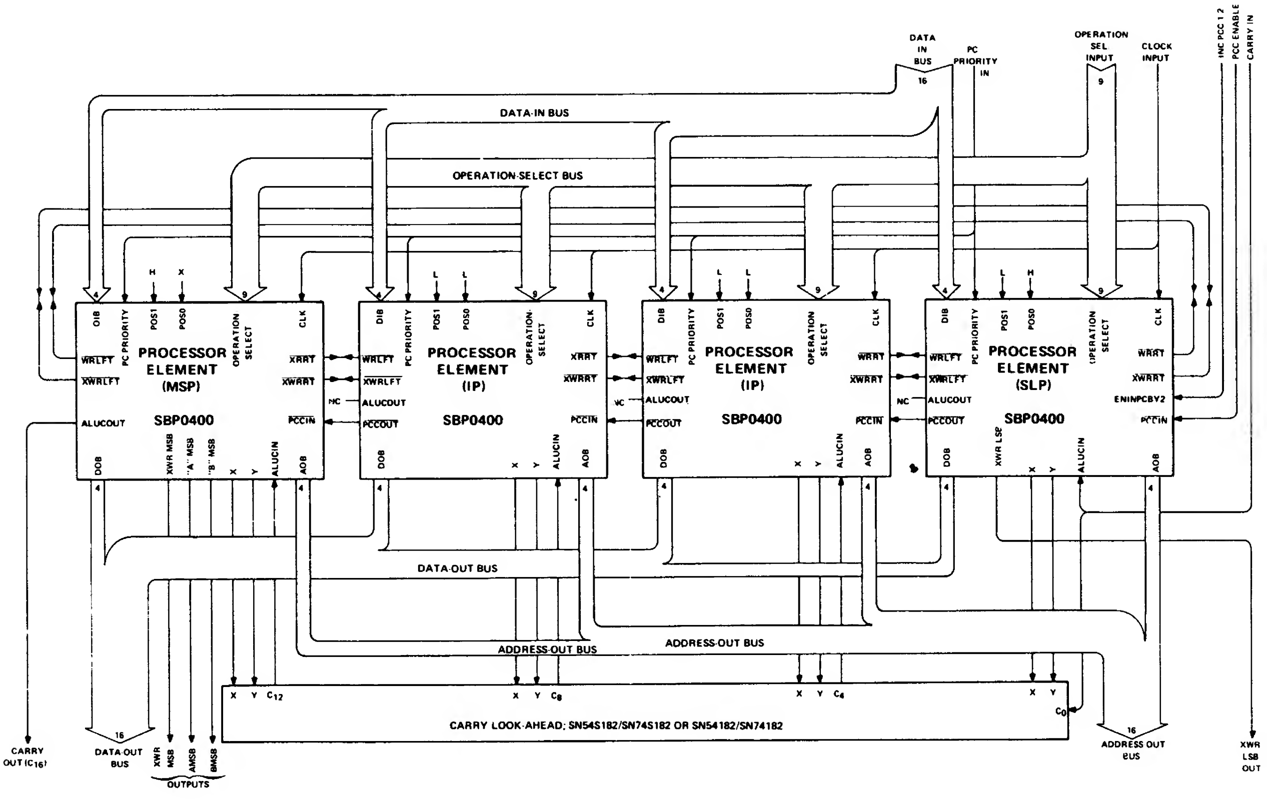

DATA IN BUS
16
PC PRIORITY IN
OPERATION SEL INPUT
9
CLOCK INPUT
INC PCC 1 2
PCC ENABLE
CARRY IN
DATA-IN BUS
OPERATION-SELECT BUS
H X
L L
L L
L H
DIB
PC PRIORITY
POS1
POS0
OPERATION SELECT
CLK
WRLFT
XWRLFT
XRRT
XWRRT
WRRT
ALUCOUT
PCCOUT
PCCIN
ENINCBY2
NC
PROCESSOR ELEMENT (MSP)
PROCESSOR ELEMENT (IP)
PROCESSOR ELEMENT (IP)
PROCESSOR ELEMENT (SLP)
SBP0400
DOB
XWR MSB
'A' MSB
'B' MSB
XWR LSB
X Y
ALUCIN
AOB
4
DATA-OUT BUS
ADDRESS-OUT BUS
ADDRESS-OUT BUS
X Y C12
X Y C8
X Y C4
X Y
C0
CARRY LOOK-AHEAD: SN54S182/SN74S182 OR SN54182/SN74182
CARRY OUT (C16)
16
DATA-OUT BUS
XWR MSB
MSB
AMSB
BMSB
OUTPUTS
16
ADDRESS OUT BUS
XWR LSB OUT

FIGURE 6. 16-Bit Parallel Operation with Full Carry Look Ahead

Operation

All operations carried out by the SBP0400 are defined by the operation select word. This word is 9 bits wide giving a total of 512 possible operations, of which 459 are used. The 459 operations are all executed in a single clock cycle, and the execution time of output instructions varies with the complexity of the data path of the given instruction according to the Table 3. The operation select word is divided into three fields – the OP Field (OP3-Op0) the D Field (D1, D0) and the S Field (S2, S1, S0). The 4-bit OP field defines one of the sixteen a.l.u. functions shown in Table 4. Eight of these functions are arithmetic (OP3 = 'low') and eight are logical (OP3 = 'high'). Bits D1 and D0 are used to define single or double precision working and to extend the interactivity of the operation select word. Finally the three bits of the S-Field either define the operand source and destination (from the DATA-IN BUS, DATA-OUT BUS, working or extended working registers, register file and ADDRESS-OUT BUS) or address one of the eight registers in the register file, depending on the rest of the operation select word. (See Table 5).

Program Control: In order to assist the user to program this microprocessor the operation select words are divided into six operation forms, representing a total of 45 types of operation. It is the combination of these operations with the appropriate a.l.u. functions and register file locations which makes up the total of 459 unique one-clock operations. The six operation forms and the functions which they can be used to perform are listed in Table 6. To use an expanded system the double-precision shift data flow is as shown in Figure 7.

Instruction Decoding: The incoming operation select word is decoded by the p.l.a. into a 20-bit wide internal

Table 3. Output Instruction Times

PARAMETER	FROM	TO	TEST CONDITIONS	TYPICAL	UNIT
t_{PLH} or t_{PHL}	DIB	DOB	VIA A BUS, BYPASS ALU	250	ns
t_{PLH} or t_{PHL}	DIB	DOB	VIA A BUS, THRU ALU	380	ns
t_{PLH} or t_{PHL}	DIB	DOB	VIA B BUS, THRU ALU	500	ns
t_{PLH} or t_{PHL}	PC PRIORITY	AOB		180	ns
t_{PLH} or t_{PHL}	ALUCIN	ALUCOUT		180	ns
t_{PLH} or t_{PHL}	DIB	ENINCBY2/AMSB	POS0 = X, POS1 = H	180	ns
t_{PLH} or t_{PHL}	DIB	$\overline{\text{PCCOUT}}$/BMSB	POS0 = X, POS1 = H	250	ns
t_{PLH} or t_{PHL}	POS0, or POS1	ENINCBY2/AMSB or $\overline{\text{PCCOUT}}$/BMSB		180	ns
t_{PLH} or t_{PHL}	$\overline{\text{PCCIN}}$	$\overline{\text{PCCOUT}}$		110	ns
t_{PLH} or t_{PHL}	ALUCIN	DOB		310	ns
t_{PLH} or t_{PHL}	CLOCK	$\overline{\text{PCCOUT}}$/BMSB	POS0 = X, POS1 = H	350	ns
t_{PLH} or t_{PHL}	CLOCK	DOB	VIA A BUS, BYPASS ALU	350	ns
t_{PLH} or t_{PHL}	CLOCK	DOB	VIA A BUS, THRU ALU	500	ns
t_{PLH} or t_{PHL}	CLOCK	ENINCBY2/AMSB	POS0 = X, POS1 = H	280	ns
t_{PLH} or t_{PHL}	CLOCK	DOB	VIA B BUS, THRU ALU	530	ns
t_{PLH} or t_{PHL}	CLOCK	X, Y, or ALUCOUT	VIA A OR B BUS, THRU ALU	440	ns
t_{PLH} or t_{PHL}	CLOCK	AOB		350	ns
t_{PLH} or t_{PHL}	CLOCK	$\overline{\text{WRLFT}}$, $\overline{\text{WRRT}}$, $\overline{\text{XWRLFT}}$, or $\overline{\text{XWRRT}}$		500	ns
t_{PLH} or t_{PHL}	CLOCK	XWR MSB	POS0 = H, POS1 = H	350	ns
t_{PLH} or t_{PHL}	CLOCK	XWR LSB	POS0 = H, POS1 = L	350	ns

Table 4. A.L.U. Function Select Table

ARITHMETIC OPERATIONS					LOGIC OPERATIONS
ALU SELECTION			ACTIVE-HIGH DATA (OP3 = L)		ACTIVE-HIGH DATA
			ALUCIN = H (WITH CARRY)	ALUCIN = L (NO CARRY)	
OP2	OP1	OP0			OP3 = H, ALUCIN = X
0	0	0	Fn = Low	Fn = High	Fn = AnBn
0	0	1	Fn = B – A	Fn = B – A – 1	Fn = An ⊕ Bn
0	1	0	Fn = A – B	Fn = A – B – 1	Fn = $\overline{\text{An} \oplus \text{Bn}}$
0	1	1	Fn = A plus B plus 1	Fn = A plus B	Fn = $\overline{\text{A}}$nBn
1	0	0	Fn = B plus 1	Fn = B	Fn = An$\overline{\text{B}}$n
1	0	1	Fn = $\overline{\text{B}}$ plus 1	Fn = $\overline{\text{B}}$	Fn = An + $\overline{\text{B}}$n
1	1	0	Fn = A plus 1	Fn = A	Fn = $\overline{\text{A}}$n + Bn
1	1	1	Fn = $\overline{\text{A}}$ plus 1	Fn = $\overline{\text{A}}$	Fn = An + Bn

NOTE: Positive logic is used throughout: 1 = high, 0 = low.

Table 5. Register File Selection Table

S-FIELD			REGISTER
S2	S1	S0	SELECT
0	0	0	RF0
0	0	1	RF1
0	1	0	RF2
0	1	1	RF3
1	0	0	RF4
1	0	1	RF5
1	1	0	RF6
1	1	1	PC

Table 6. Operation Forms and Possible Functions

OPERATION FORM I

Operation form I can be utilized to perform 1 of 16 ALU functions, selected by the Operation-Select Word OP-field, on 2 of 4 operand sources, (RF, WR, XWR, DIB). The result is transferred to 1 of 4 operand destinations (RF, WR, XWR, DOB).

OPERATION TYPE	OPERATION FORM I		
RF ALU WR → RF	ALU: 0000 → 1111	0 0	RF: 000 → 111
RF ALU WR → WR	ALU: 0000 → 1111	0 1	RF: 000 → 111
*DIB ALU WR → DOB	ALU: 0000 → 1111	1 1	0 0 0
*DIB ALU WR → WR	ALU: 0000 → 1111	1 1	0 0 1
DIB ALU XWR → WR	ALU: 0000 → 1111	1 1	0 1 1
DIB ALU WR → XWR	ALU: 0000 → 1111	1 1	1 0 0
DIB ALU XWR → XWR	ALU: 0000 → 1111	1 1	1 1 0
DIB ALU XWR → DOB	ALU: 0000 → 1111	1 1	1 1 1
	OP3 → OP0	D1 D0	S2 S1 S0

NOTE: When PC PRIORITY is low WR → AOB.
*XWR → AOB.

OPERATION FORM II

Operation form II can be utilized to arithmetically sum 1 or 2 operand sources (RF, WR, XWR, DIB) and a ripple-carry-in (ALUCIN). The result is transferred to 1 of 4 operand destinations (RF, WR, XWR, DOB).

OPERATION TYPE	OPERATION FORM II		
RF plus WR plus ALUCIN → XWR	0 0 1 1	1 0	RF: 000 → 111
RF plus DIB plus ALUCIN → WR	0 1 0 0	1 0	RF. 000 → 111
RF plus DIB plus ALUCIN → XWR	0 1 0 1	1 0	RF: 000 → 111
RF plus DIB plus ALUCIN → RF	0 1 1 1	1 0	RF: 000 → 111
RF plus XWR plus ALUCIN → WR	1 1 0 0	1 0	RF: 000 → 111
RF plus XWR plus ALUCIN → XWR	1 1 0 1	1 0	RF: 000 → 111
XWR plus ALUCIN → RF	1 1 1 0	1 0	RF: 000 → 111
DIB plus WR plus ALUCIN → XWR	0 0 1 1	1 1	0 1 0
DIB plus WR plus ALUCIN → DOB	0 1 1 1	1 1	0 1 0
DIB plus XWR plus ALUCIN → WR	1 1 0 0	1 1	0 1 0
DIB plus XWR plus ALUCIN → XWR	1 1 0 1	1 1	0 1 0
XWR plus ALUCIN → DOB	1 1 1 0	1 1	0 1 0
	OP3 → OP0	D1 D0	S2 S1 S0

OPERATION FORM III

Operation form III can be utilized to transfer 1 of 2 operand sources (RF, DIB) to 1 of 4 operand destinations (RF, WR, XWR, DOB).

OPERATION TYPE	OPERATION FORM III		
DIB → RF	1 1 1 1	1 0	RF: 000 → 111
RF → DOB	0 0 0 0	1 0	RF: 000 → 111
RF → XWR	0 0 0 1	1 0	RF: 000 → 111
DIB → WR	0 1 1 0	1 0	X X X
	0 1 1 0	1 1	0 1 0
DIB → XWR	0 0 0 1	1 1	0 1 0
DIB → DOB	1 1 1 1	1 1	0 1 0
	0 0 0 0	1 1	0 1 0
	OP3 → OP0	D1 D0	S2 S1 S0

OPERATION FORM IV

Operation form IV can be utilized to either:

- arithmetically sum the WR and the ripple carry-in (ALUCIN) with 1 of 2 operand sources (RF, DIB), arithmetically double-precision shift the result to the right, and transfer the shifted result to the WR and XWR;
- arithmetically sum the WR and the ripple carry-in (ALUCIN) with 1 of 2 operand sources (RF, DIB), double-precision circulate the result to the left, and transfer the circulated result to the WR and XWR;
- arithmetically subtract 1 of 2 operand sources (RF, DIB) and −1 from the WR, arithmetically add the ripple carry-in (ALUCIN), double-precision circulate the result to the left, and transfer the circulated result to the WR and XWR.

OPERATION TYPE	OPERATION FORM IV		
(WR − DIB − 1 plus ALUCIN) LCIR → WR, XWR	1 0 0 0	1 1	0 1 0
(WR plus DIB plus ALUCIN) LCIR → WR, XWR	1 0 0 1	1 1	0 1 0
(WR − RF − 1 plus ALUCIN) LCIR → WR, XWR	1 0 0 0	1 0	RF: 000 → 111
(WR plus RF plus ALUCIN) LCIR → WR, XWR	1 0 0 1	1 0	RF: 000 → 111
(WR plus ALUCIN) RSA → WR, XWR	1 0 1 0	1 0	X X X
	1 0 1 0	1 1	0 1 0
(WR − DIB − 1 plus ALUCIN) RSA → WR, XWR	0 0 1 0	1 1	0 1 0
(WR plus DIB plus ALUCIN) RSA → WR, XWR	1 0 1 1	1 1	0 1 0
(WR − RF − 1 plus ALUCIN) RSA → WR, XWR	0 0 1 0	1 0	RF: 000 → 111
(WR plus RF plus ALUCIN) RSA → WR, XWR	1 0 1 1	1 0	RF: 000 → 111
	OP3 → OP0	D1 D0	S2 S1 S0

OPERATION FORM V

Operation form V can be utilized to perform single-precision shifts on the contents of the WR, placing the result in the WR. The WR may be logically shifted left or right (LSL, RSL), arithmetically shifted left or right (LSA, RSA), or circulated left or right (LCIR, RCIR). In operation form V shifts, the MSB of the ALU is utilized as the sign-bit.

As the WR is passed through the ALU during form V and VI the ALUCIN is active and should be held at a low logic level for true shifts.

OPERATION TYPE	OPERATION FORM V		
(WR plus ALUCIN) RSA → WR	0 0 0 0	1 1	1 0 1
(WR plus ALUCIN) RCIR → WR	0 0 0 1	1 1	1 0 1
	1 0 0 1	1 1	1 0 1
(WR plus ALUCIN) LSA → WR	0 0 1 0	1 1	1 0 1
(WR plus ALUCIN) LCIR → WR	0 0 1 1	1 1	1 0 1
	1 0 1 1	1 1	1 0 1
(WR plus ALUCIN) RSL → WR	1 0 0 0	1 1	1 0 1
(WR plus ALUCIN) LSL → WR	1 0 1 0	1 1	1 0 1
	OP3 → OP0	D1 D0	S2 S1 S0

OPERATION FORM VI

Operation form VI can be utilized to perform double-precision shifts on the contents of WR in conjunction with XWR. The WR in conjunction with the XWR may be:

- logically shifted left or right (LSL, RSL);
- arithmetically shifted left or right (LSA, RSA) single- or double-signed;
- circulated left or right (LCIR, RCIR).

In OPERATION FORM VI arithmetic shifts, the MSB of the ALU is utilized as the sign bit. For single signed arithmetic shifts the MSB of the ALU is placed in the MSB of the WR. For double signed arithmetic shifts, the MSB of the ALU is placed in the MSBs of both the WR and XWR.

OPERATION TYPE	OPERATION FORM VI		
(WR plus ALUCIN, XWR) RSA → (WR, XWR)	0 1 0 0	1 1	1 0 1
(WR plus ALUCIN, XWR) RICR → (WR, XWR)	0 1 0 1	1 1	1 0 1
	1 1 0 1	1 1	1 0 1
(WR plus ALUCIN, XWR) LSA → (WR, XWR)	0 1 1 0	1 1	1 0 1
(WR plus ALUCIN, XWR) LCIR → (WR, XWR)	0 1 1 1	1 1	1 0 1
	1 1 1 1	1 1	1 0 1
(WR plus ALUCIN, XWR) RSL → (WR, XWR)	1 1 0 0	1 1	1 0 1
(WR plus ALUCIN, XWR) LSL → (WR, XWR)	1 1 1 0	1 1	1 0 1
	OP3 → OP0	D1 D0	R2 R1 R0

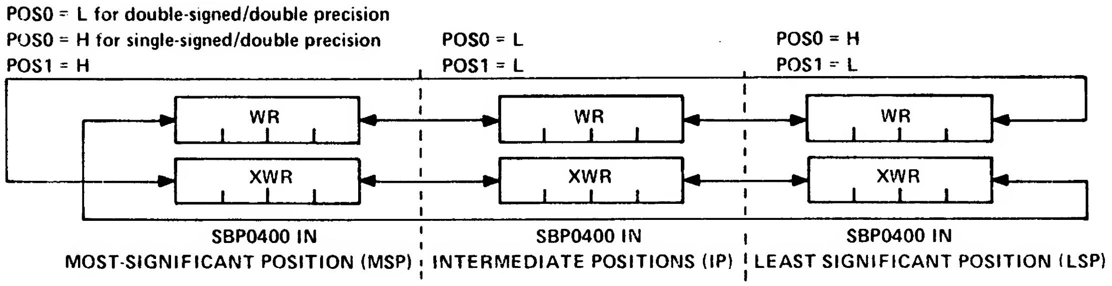

POS0 = L for double-signed/double precision
POS0 = H for single-signed/double precision
POS1 = H
POS0 = L
POS1 = L
POS0 = H
POS1 = L
WR
XWR
WR
XWR
WR
XWR
SBP0400 IN
MOST-SIGNIFICANT POSITION (MSP)
SBP0400 IN
INTERMEDIATE POSITIONS (IP)
SBP0400 IN
LEAST SIGNIFICANT POSITION (LSP)

FIGURE 7. Double Precision Shift Data Flow

control word which is stored in the operation register (o.r.). Referring to the input/output sequence timing, given in Figure 8, the decoded operation select word is clocked into the o.r. at the positive-going clock edge at t_0. The preceding time t_{setup} allows for the decoding to take place. The hold-time is in fact zero, so that the next operation select word can be presented at any time after t_0. The provision of the 'pipelining' operation register means that the current control word will be held while the next instruction is being fetched. As previously mentioned if the P C PRIORITY line is taken 'high' at any time the contents of the p.c. will be forced onto the ADDRESS-OUT BUS. The address of the next instruction is therefore available 180ns after the current instruction has been latched into the o.r. allowing 620ns for fetching the next instruction.

Instruction Sequencing: A sequence of instructions is carried out on consecutive clock cycles, with the instruction look ahead system described in the preceding section being used to fetch instructions from the microprogram memory. Figure 9 shows a typical sequence in which data is first put into the working register (DIB WR). The sum of this data and the a.l.u. carry input (ALUCIN) is then shifted arithmetically to the right and re-written into the working register. [(WR plus ALUCIN) RSA-WR]. Finally the new contents of w.r. and the contents of register file A are operated on by the a.l.u. (1 to 16 functions) and rewritten into register file A [WR (ALU) RFA-RFA]. The detailed functioning of this sequence is as follows. Prior to time t_0 the address of the first instruction has been fed out on to the ADDRESS-OUTPUT BUS and the first instruction presented on the OPERATION SELECT WORD BUS. At the positive-going clock transition, at time t_0, the instruction is latched into the operation register. This first instruction requires data from the DATA-IN BUS to be stored in the working register which is an edge-triggered static D-type latch. This latching operation takes place on the next positive-going clock, at time t_1, and therefore it is necessary for the data relating to the instruction stored at t_0 to be present at t_1. This requirement is common to all instructions which result in new data being stored in a register. During the first clock cycle t_0-t_1 the PC PRIORITY input is taken 'high', forcing the incremented program counter onto the ADDRESS-OUT BUS. This allows the

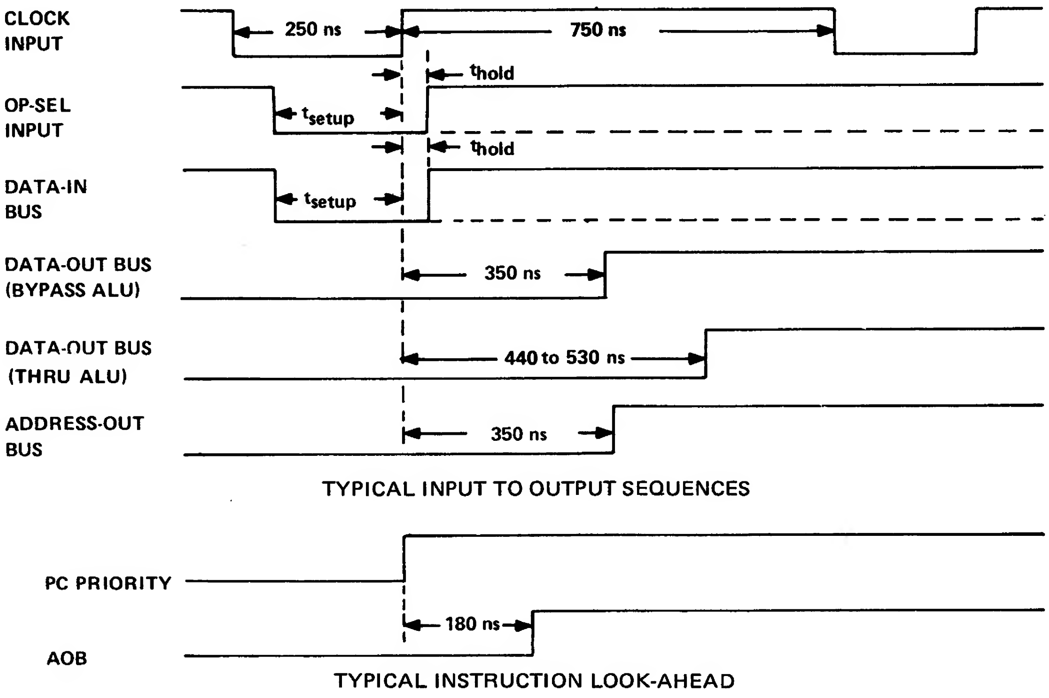
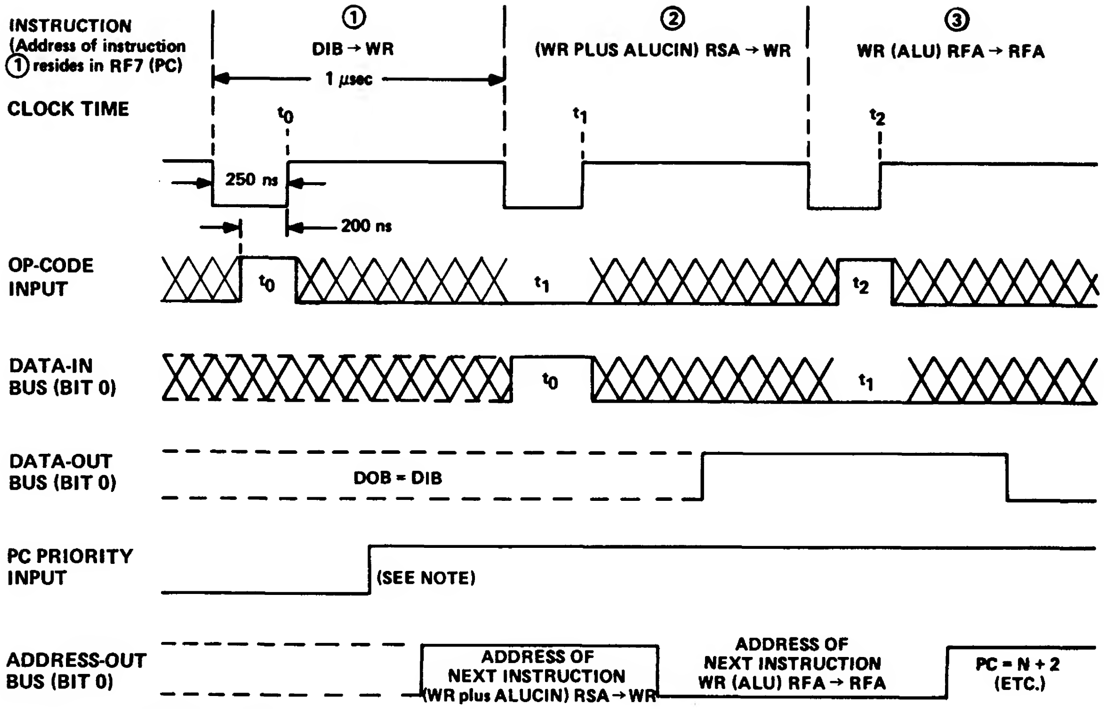

CLOCK INPUT
250 ns
750 ns
OP-SEL INPUT
t_{hold}
t_{setup}
DATA-IN BUS
t_{hold}
t_{setup}
DATA-OUT BUS (BYPASS ALU)
350 ns
DATA-OUT BUS (THRU ALU)
440 to 530 ns
ADDRESS-OUT BUS
350 ns
TYPICAL INPUT TO OUTPUT SEQUENCES
PC PRIORITY
180 ns
AOB
TYPICAL INSTRUCTION LOOK-AHEAD

FIGURE 8. Input/Output Sequence Timing


INSTRUCTION
(Address of instruction ① resides in RF7 (PC)
CLOCK TIME
①
DIB → WR
1 μsec
②
(WR PLUS ALUCIN) RSA → WR
③
WR (ALU) RFA → RFA
t0
t1
t2
250 ns
200 ns
OP-CODE INPUT
DATA-IN BUS (BIT 0)
DATA-OUT BUS (BIT 0)
DOB = DIB
PC PRIORITY INPUT
(SEE NOTE)
ADDRESS-OUT BUS (BIT 0)
ADDRESS OF NEXT INSTRUCTION (WR plus ALUCIN) RSA → WR
ADDRESS OF NEXT INSTRUCTION WR (ALU) RFA → RFA
PC = N + 2 (ETC.)

A typical sequence of operations shows:

1. Op-code instruction (DIB → WR) is setup and clocked into operation register (OR) at t_0 transition. Advance program counter (PC by 1 for next address.
2. At t_1 execute DIB → WR and fetch address of next instruction.
3. At t_2 execute (WR plus ALUCIN) RSA → WR and fetch address of next instruction.

NOTE: When taken high the PC priority input overrides any OR instruction and routes program-counter (PC) contents to AOB. PC can be incremented by the clock to generate next address at the AOB.

FIGURE 9. Typical Instruction Sequence

second instruction to be latched into the operation register at time t_1. Note that this is the same time at which the data in instruction 1 was being stored, making this data available for use in instruction 2. The PC PRIORITY input has remained 'high' so that the incremented p.c. is available 180ns after time t_1, for fetching the third instruction. Again the result of instruction 2 is stored at the same time that instruction 3 is being stored, i.e. at time t_2. Instructions where the result is not latched into a register, but is output from the device, are executed in times between 110 and 530 ns according to the figures previously given in Table 3, and the data is available on the outputs after that execution time.

Driving the Device: As explained in the chapter on i.i.l.[1], this type of logic is current driven rather than voltage driven and accordingly the SBP0400 has two current injector inputs which can be externally connected together. The nominal operating condition for the device is when the total current flowing into the two injector inputs is 150mA. Under this condition a forward voltage of 0·85V is generated internally and appears at the common node. The device can therefore be run from a single d.c. power supply of greater than 0·85V by the inclusion of a resistor suitable for dropping the voltage to 0·85V at 150mA. This arrangement is shown in Figure 10. The inputs and outputs are t.t.l. compatible at this nominal injector current. On the input a voltage dividing network of two 10kΩ resistors as shown in Figure 11, raises the low threshold of the transistor to 1·5V, while the diode protects against negative excursions. The open-collector output looks like a normal Schottky t.t.l. output, and a discrete resistor is used to 'pull-up' to logic '1' level. These circuit arrangements are integrated directly to form the bidirectional input/output needed on some of the SBP0400 connections.

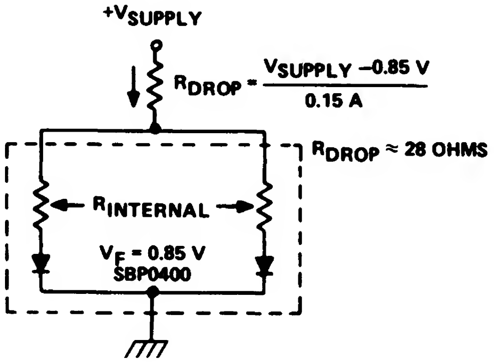

+VSUPPLY
RDROP = (VSUPPLY −0.85 V) / 0.15 A
RDROP ≈ 28 OHMS
RINTERNAL
VF = 0.85 V
SBP0400

FIGURE 10. Power Supply Arrangement

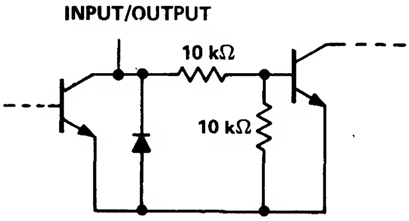

INPUT/OUTPUT
10 kΩ
10 kΩ

FIGURE 11. I.I.L. Gate Input/Output Equivalent

A 16-Bit Microcomputer System

Figure 12 shows one way in which four SBP0400 microprocessor devices may be used, with external components, to implement a 16-bit word length computer system. The system architecture features the modern concepts of:

a) Reduced package count
b) Programmable control through read-only memory devices.
c) 3-state bus organisation virtually eliminating the need for multiplexers.

Fundamental system control is provided by a standard p.r.o.m. micro-controller. The micro-controller directs the fetching of an instruction from either program memory or a peripheral device, and directs system execution of the fetched instruction. The organisation of the SBP0400 device allows the micro-controller to increase system efficiency by overlapping the execution of the present instruction with the fetching of the next instruction. The micro-controller consists of:

a) a 256-word x 52-bit c.r.o.m.,
b) a 256-word x 16-bit p.r.o.m.,
c) a 9-input, 20-output p.l.a. internal to each '0400,
d) a 2-bit, D-type operation register (o.r.) internal to each '0400,
d) a 43-bit, D-type external operation register.

Each instruction is constructed from a sequential series of micro-operations. Each micro-operation directs the maximum amount of instruction execution progress which the processor ('0400s with micro-controller) is capable of achieving in one system clock period. The set of micro-operations required for execution of a particular instruction is referred to as an instruction micro-sequence. The instruction micro-sequence for each instruction in the computer system's instruction set is programmed into the c.r.o.m.. At any particular time, the c.r.o.m. is addressed, under the direction of 1 to 4, 3-state, 8-bit buses:

a) the instruction operation code bus,
b) the next address bus #1 (NA1),
c) the next address bus #2 (NA2) or
d) the interrupt address bus.

Each addressable location in the c.r.o.m. is referred to as a micro-state of the micro-controller. At the time when a fetched instruction first becomes available to the micro-controller, the state transfer p.r.o.m. selects the instruction operation-code to address the c.r.o.m. As a result, an 8-bit operation-code field of the fetched instruction addresses the initial micro-state of the respective instruction micro-sequence. Upon the positive transition of the system clock: (a) 43 of 52 bits of micro-operation data is transferred from the c.r.o.m. output to the 43-bit, external operation register and (b) 9 of 52 bits of micro-operation data is transferred from the c.r.o.m. output of each '0400, where it is internally decoded via each individual '0400's p.l.a. and loaded into the internal 20-bit o.r. of the SBP0400s. At this time the o.r. internal to each '0400 contains control information which enables the appropriate internal '0400 functional blocks and buses to execute the present one-clock period, micro-operation. Also, at this time, the external operation register contains:

a) control information which enables the appropriate registers and buses external to the '0400s to execute the present, one-clock period, micro-operation,
b) select information which directs the state transfer p.r.o.m. to interrogate the appropriate system conditions pertinent to the present micro-operation and, as a result, select the relevant c.r.o.m. address bus to address the next one-clock period, micro-operation,and
c) two 8-bit next address data blocks, one driving the c.r.o.m. address bus NA1, the other driving the c.r.o.m. address bus NA2.

Upon the next positive transition of the system clock, the 'next' one-clock period micro-operation is loaded into the o.r.s, where it becomes the present micro-operation. The above process is continued, completing the instruction micro-sequence necessary to execute the relevant instruction. During execution of the present instruction micro-sequence, the system is prepared for fetching the next instruction for either program memory or a peripheral device. Consequently, when the present instruction micro-sequence is completed, the micro-controller, if a system interrupt is not pending, merely steps to the initial micro-state of the next instruction's micro-sequence. If upon completion of the 'present' instruction's micro-sequence, a system interrupt is pending, the micro-controller merely steps to the initial micro-state of the interrupt micro-sequence.

Summarising, the micro-controller sequences both the execution of an instruction at the micro-operation level and the execution of a program at the instruction level. If an abnormal system condition warrants interruption of the main program instruction stream, the micro-controller branches the program execution to an interrupt-servicing subroutine. At the completion of the interrupt-servicing subroutine, the micro-controller may be instructed to branch back to the point where the normal program instruction stream was interrupted. At this time, normal program execution will continue.

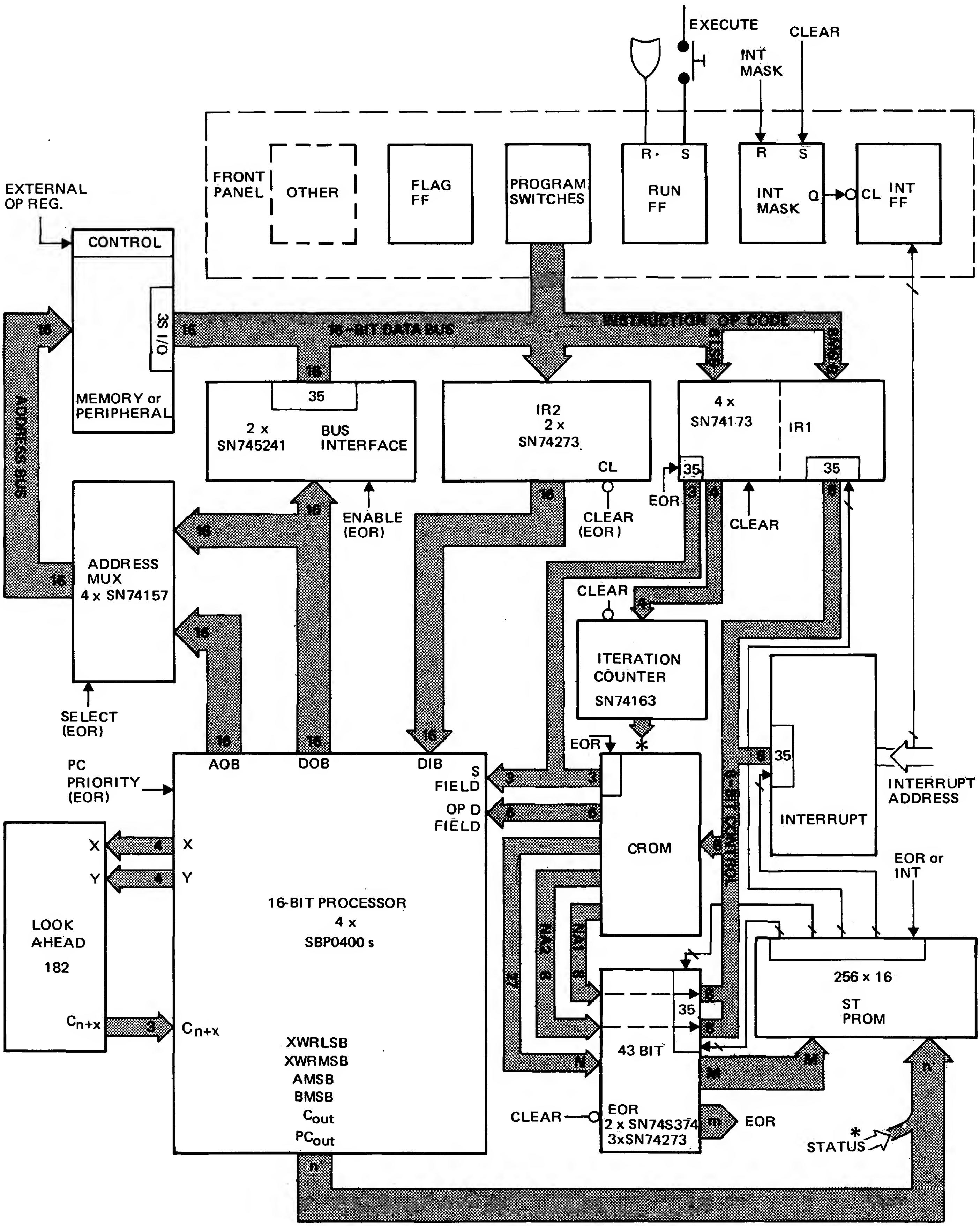

EXECUTE
CLEAR
INT MASK
FRONT PANEL
OTHER
FLAG FF
PROGRAM SWITCHES
R S
RUN FF
R S
INT MASK
Q
CL
INT FF
EXTERNAL OP REG.
CONTROL
3S I/O
MEMORY or PERIPHERAL
16
16-BIT DATA BUS
INSTRUCTION OP CODE
16
35
2 x SN745241
BUS INTERFACE
IR2
2 x SN74273
CL
4 x SN74173
IR1
35
35
EOR
ENABLE (EOR)
CLEAR (EOR)
CLEAR
ADDRESS BUS
ADDRESS MUX
4 x SN74157
SELECT (EOR)
CLEAR
ITERATION COUNTER
SN74163
EOR
*
35
INTERRUPT
INTERRUPT ADDRESS
PC PRIORITY (EOR)
AOB
DOB
DIB
S FIELD
OP D FIELD
CROM
8-BIT CONTROL
LOOK AHEAD
182
X
Y
X
Y
Cn+x
Cn+x
16-BIT PROCESSOR
4 x
SBP0400 s
XWRLSB
XWRMSB
AMSB
BMSB
Cout
PCout
NA2
NA1
35
43 BIT
CLEAR
EOR
2 x SN74S374
3xSN74273
EOR
EOR or INT
256 x 16
ST PROM
STATUS
*
M
m
n

FIGURE 12. 16-Bit Microcomputer System

Organisation

An example of one chip microcomputers, where all sections are integrated to form the complete self-contained micro-computer system, is the TMS1000 series. The internal organisation of this family is shown in Figure 13. The main elements are an 8192-bit program r.o.m., an instruction decoder, an output p.l.a., a 256-bit data r.a.m., a 4-bit parallel binary a.l.u., X, Y and accumulator registers, R(Control) OUTPUTS and latch, and 0 (data) OUTPUTS and latches. During the manufacture of the device the customer's binary program is mask-programmed into the r.o.m. defining a unique version of the TMS1000 for that particular customer. The same gate-mask which specifies the program will also define the format of the output data, and additionally can be used to alter and combine some of the instructions in the basic set. The micro-computer's program r.o.m. controls the functions of data input and output, storage, processing, and control output. Input data from the four parallel K INPUTS is read via the a.l.u. into the accumulator register. The accumulator register acts as an operand source for the output latches, the data r.a.m. and the a.l.u.. Data output is by means of the 8 parallel 0 OUTPUTS. These outputs are driven by the output formating p.l.a. which formats data from the accumulator into any code of 8 bits or less. The output code is defined in the mask programming state. A further set of outputs is provided by the R OUTPUTS. Each of these lines is driven from a latch which is individually set by the program r.o.m. The TMS1000 (28-pin package) has eleven R OUTPUTS while the TMS1200 (40-pin package) has thirteen R OUTPUTS. The R OUTPUTS are used to control external devices such as multiplexers, universal asynchronous receiver/transmitters (u.a.r.t.) etc. and can also be used as strobes for keyboards and displays. In the first case the R OUTPUTS will scan connections made to the K INPUTS and in the second case the R OUTPUTS will be used as digit strobes indicating that a particular digit is available on the output lines.

Architecture: There is a fundamental difference in architecture between the single-chip micro-computer and conventional microprocessors. The TMS1000 family, although similar to the microprocessor in that it has a 4-bit a.l.u., is constructed to handle numbers in a hexadecimal sequence: an incoming word of, say, 16 bits is read in four 4-bit bytes, each byte then representing a hexadecimal digit. Data is stored in each r.a.m. word location as a 4-bit digit and is called up by the a.l.u. in digit sequence. If the outout decoding p.l.a. gives a 1 to 1 representation of the accumulator contents, the final output number will again be a string of hexadecimal digits which in serial will represent

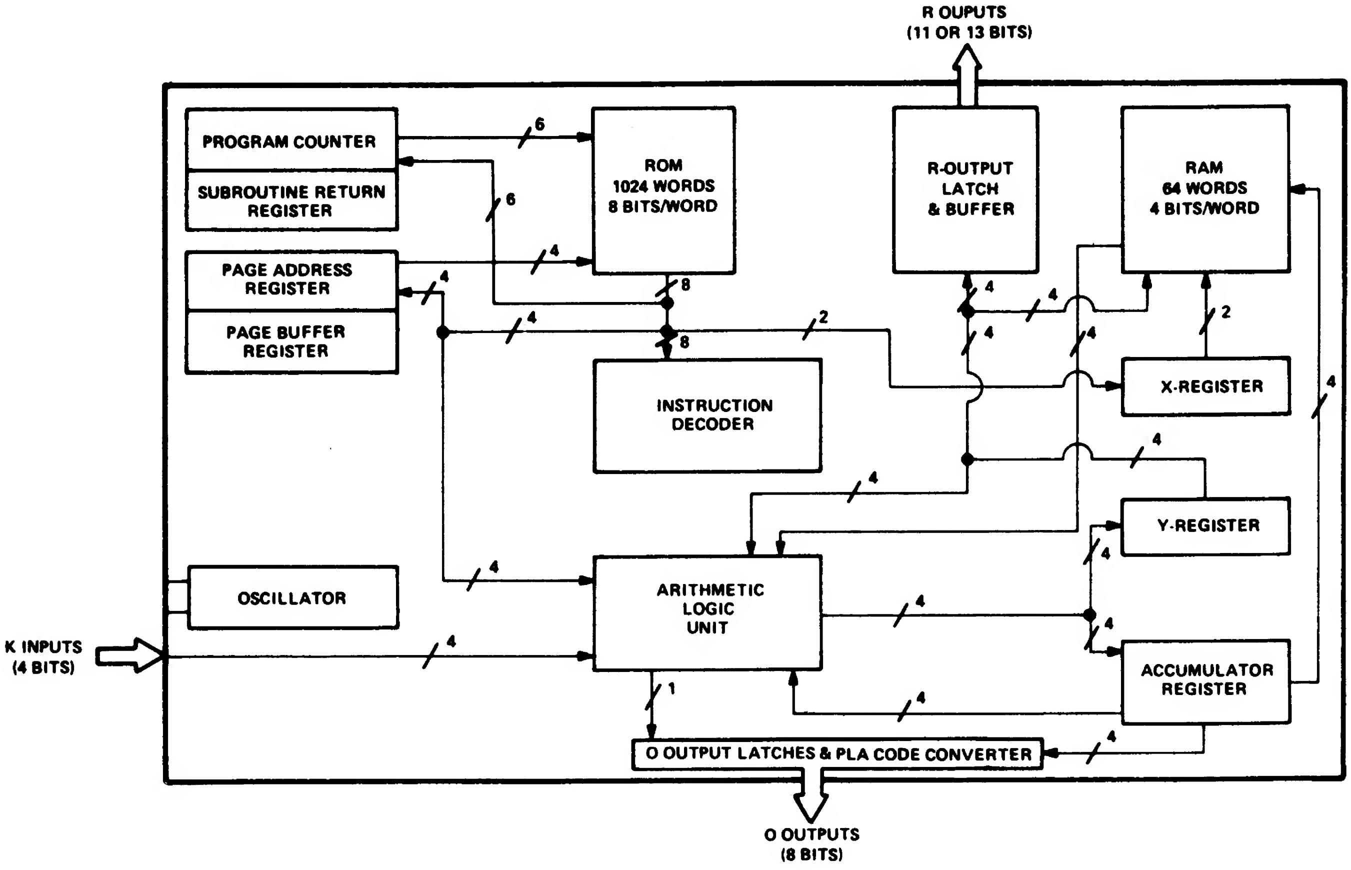

R OUPUTS
(11 OR 13 BITS)
PROGRAM COUNTER
SUBROUTINE RETURN REGISTER
PAGE ADDRESS REGISTER
PAGE BUFFER REGISTER
ROM
1024 WORDS
8 BITS/WORD
R-OUTPUT LATCH & BUFFER
RAM
64 WORDS
4 BITS/WORD
INSTRUCTION DECODER
X-REGISTER
Y-REGISTER
OSCILLATOR
ARITHMETIC LOGIC UNIT
ACCUMULATOR REGISTER
K INPUTS
(4 BITS)
O OUTPUT LATCHES & PLA CODE CONVERTER
O OUTPUTS
(8 BITS)
6
6
4
4
8
8
4
2
4
4
4
4
2
4
4
4
4
4
4
4
1
4
4

FIGURE 13. Internal Organisation of TMS1000 Series

an ordinary n-bit binary number. Alternatively a b.c.d. correct loop may be executed before data is output, and the resultant data could then be read out as a string of b.c.d. digits or it could be converted by the output p.l.a. into 7-segment data to drive a display.

Program Memory· The program of macroinstructions which the device is required to execute is held in an 8192-bit r.o.m. organised as 1024 by 9-bit words. There are 16 pages of instructions with 64 instructions on each page. The 6-bit program counter register addresses one of the 64 instructions on a given page which is addressed by the 4-bit page address register, as shown in Figure 14. The program counter is reset to the start address by a special latch which is activated after power-up, thereafter the program counter sequentially addresses each r.o.m. instruction on a page. The contents of the program counter may be altered by a conditional branch or call subroutine instruction. One level of subroutine return address is stored in the subroutine return register. To change pages a constant held in the r.o.m. is loaded into the page address buffer and when a branch or call takes place the page buffer loads into the page address register. In the subroutine mode the address of the return page is held in the page address buffer.

Data Memory and Registers: 256 bits of r.a.m. storage are provided for data. The r.a.m. is organised as 4 pages each containing 16 by 4-bit words, and is addressed by the X page address register and the Y word-address register as shown in Figure 15. The X register is loaded from a constant held in the r.o.m. or can be complemented, while the Y register is set by the a.l.u. There are several instructions in the basic set which perform modifications of the Y register. Data from the r.a.m. is sent to the a.l.u. and can be operated on or loaded into the Y or accumulator registers in one instruction cycle. Data is loaded into the r.a.m. from the accumulator register or from a constant held in the r.o.m. Any data bit in the r.a.m. can be individually set, reset or tested by the bit instruction.

A.L.U.: The 4-bit parallel binary a.l.u. is made up of a two port 4-bit binary adder, the 4-bit accumulator and Y registers, and data input multiplexers as shown in Figure 16. The two 4-bit inputs through the P and N ports may be added together or logically compared. The accumulator outputs can be inverted through the N port to provide for subtraction by 'twos complement' arithmetic. Other inputs to the N port are from the accumulator (true), the r.a.m. and the r.o.m. constants, or K inputs. Inputs to the P port are from the r.a.m., the Y register and the r.o.m. constants, or K inputs. Results of the addition or subtraction steps are held in either the Y register or the accumulator. The status bit is used to signal either the result of a logical comparison or a carry output generated in an arithmetic add. The status bit is tested with a conditional branch or call instruction which is executed if the status is logic '1'.

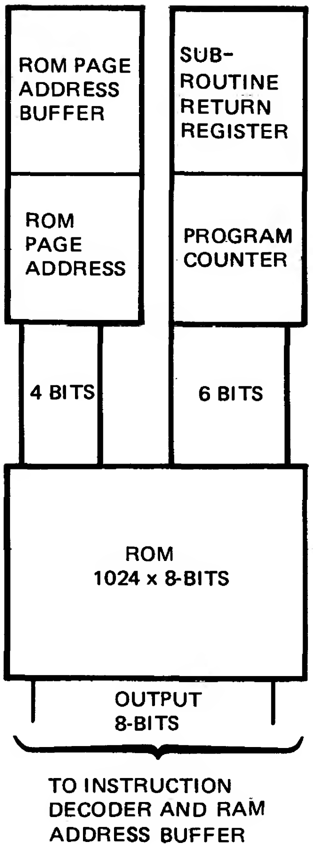

ROM PAGE ADDRESS BUFFER
SUB-ROUTINE RETURN REGISTER
ROM PAGE ADDRESS
PROGRAM COUNTER
4 BITS
6 BITS
ROM 1024 x 8-BITS
OUTPUT 8-BITS
TO INSTRUCTION DECODER AND RAM ADDRESS BUFFER

FIGURE 14. Program Memory and Address Register

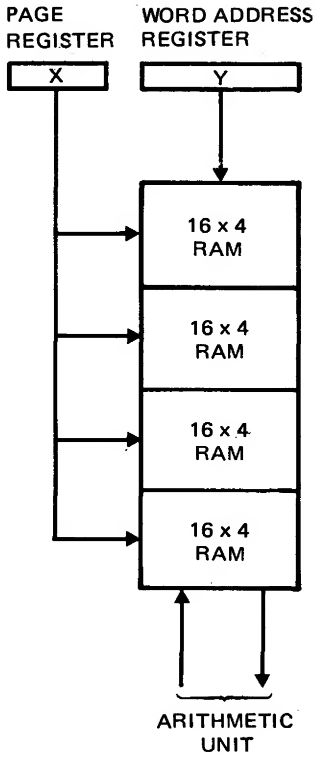

PAGE REGISTER
WORD ADDRESS REGISTER
X
Y
16 x 4 RAM
16 x 4 RAM
16 x 4 RAM
16 x 4 RAM
ARITHMETIC UNIT

FIGURE 15. Data Memory and Address Registers

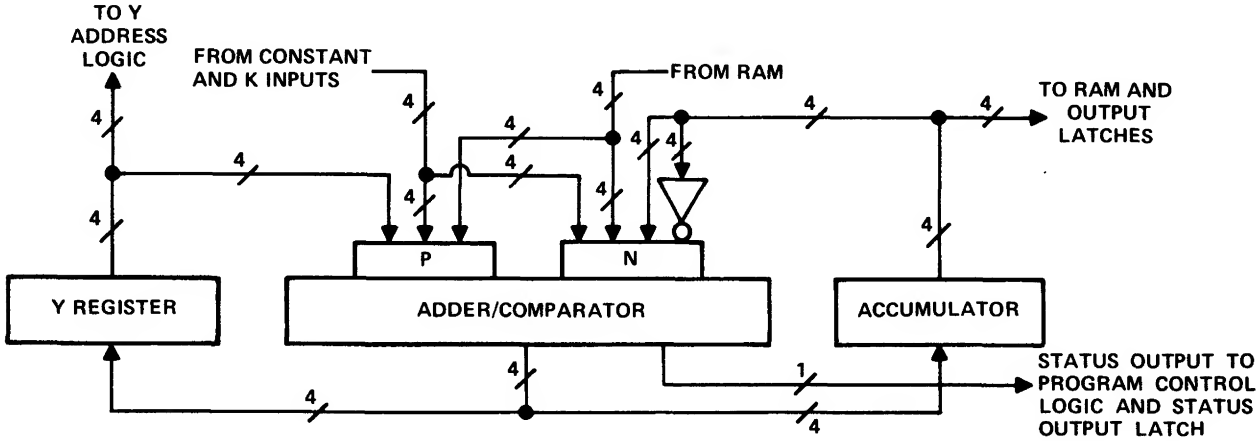

TO Y ADDRESS LOGIC
FROM CONSTANT AND K INPUTS
FROM RAM
TO RAM AND OUTPUT LATCHES
4
4
4
4
4
4
4
4
4
4
4
4
4
P
N
Y REGISTER
ADDER/COMPARATOR
ACCUMULATOR
1
STATUS OUTPUT TO PROGRAM CONTROL LOGIC AND STATUS OUTPUT LATCH

FIGURE 16. A.L.U. and Associated Data Paths

Data Input and Output: There are four parallel data inputs to the TMS1000, the K1, K2, K4, and K8 lines. When an input word is requested by the program the data path from the K INPUTS to the adder is enabled. The inputs may then be either tested or stored in the accumulator, from where they may be operated on or stored in the r.a.m.. The R OUTPUTS may be used to signal to external devices that data is about to be requested, or to control multiplexers fetching data from different sources. If data is being input from a keyboard the R OUTPUTS may be used to scan the keyboard contacts. The R OUTPUTS may also be used to signal that output data is available on the eight O OUTPUTS, and to select the source to which that data is directed. Data or addresses may also be output from the R lines by setting each bit using the SETR instructions. The output formating logic, shown in Figure 17, takes the four data bits from the accumulator and on the load output command, loads them into the output latches, together with the status bit. The formating logic array will then either output directly the four binary bits, or will output the data encoded according to mask-programmed encoded logic.

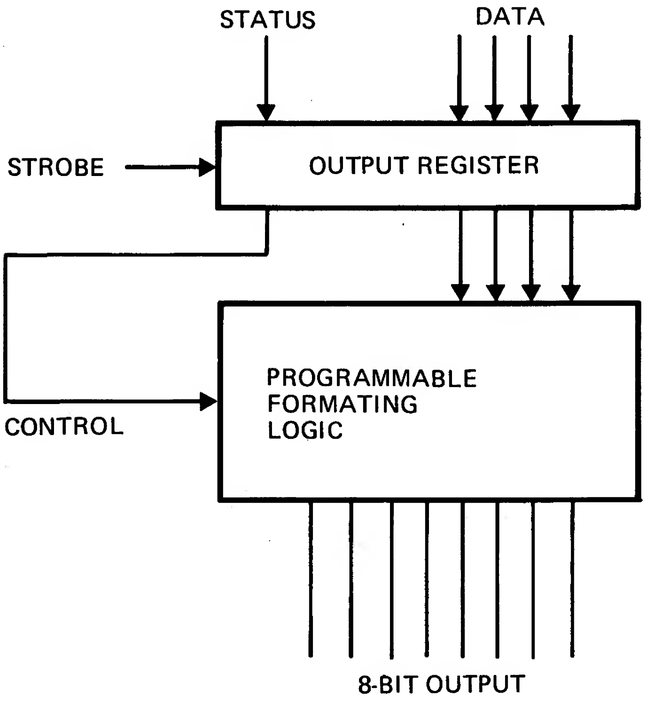
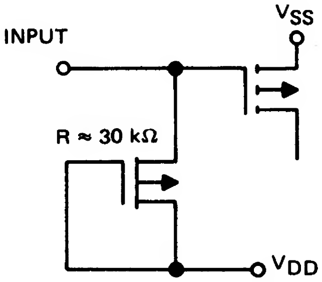


FIGURE 17. Output Formating Logic

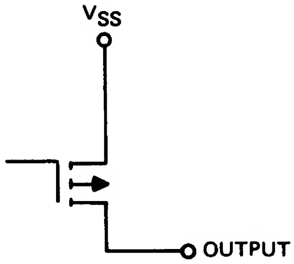
Operation

Instruction Set: The standard instruction set for the TMS1000 family of microcomputers is given in Table 7 together with the mnemonic description and effect on the status output of either comparisons or carry signals. The status bit will only be tested if there is a conditional call or branch instruction immediately following the instruction which caused the status bit to be set. The status bit always returns to its normal state (logic '1') after the next complete instruction cycle, so it can not be tested later.

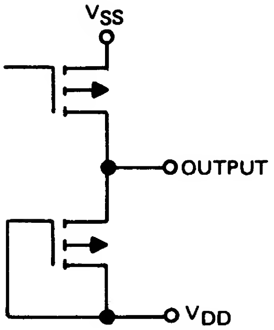
Driving: The TMS1000 family operate from a single 15V rail and their inputs are compatible with 15V open collector t.t.l. circuits. The outputs may be specified by the customer as either 'open-drain' or with 'pull-down' resistors to various short-circuit current requirements, as shown in Figure 18. A resistor dividing network may be used to shift this output level to t.t.l. levels. An internal oscillator is available, and as shown in Figure 9 this may be activated with a resistor to V_{DD} and capacitor to V_{SS}. Alternatively an external clock may be connected to OSC1 with OSC2 connected directly to the V_{SS} supply.



TYPICAL OF ALL K INPUTS



TYPICAL OF ALL O AND R OPEN-DRAIN OUTPUTS



TYPICAL OF ALL O AND R OUTPUTS WITH OPTIONAL PULL-DOWN RESISTORS

FIGURE 18. Input and Output Schematics

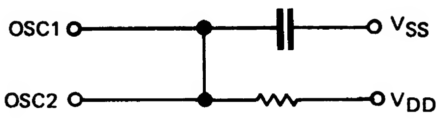


FIGURE 19. Connection for Internal Oscillator

Table 7. Standard Instruction Set for TMS1000 Series

FUNCTION	MNEMONIC	STATUS EFFECTS		DESCRIPTION
		C	N	
Register to Register	TAY			Transfer accumulator to Y register.
	TYA			Transfer Y register to accumulator.
	CLA			Clear accumulator.
Transfer Register to Memory	TAM			Transfer accumulator to memory.
	TAMIY			Transfer accumulator to memory and increment Y register.
	TAMZA			Transfer accumulator to memory and zero accumulator.
Memory to Register	TMY			Transfer memory to Y register.
	TMA			Transfer memory to accumulator.
	XMA			Exchange memory and accumulator.
Arithmetic	AMAAC	Y		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	Y		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	Y		Increment memory and load into accumulator. If carry, one to status.
	DMAN	Y		Decrement memory and load into accumulator. If no borrow, one to status.
	IA			Increment accumulator, no status effect.
	IYC	Y		Increment Y register. If carry, one to status.
	DAN	Y		Decrement accumulator. If no borrow, one to status.
	DYN	Y		Decrement Y register. If no borrow, one to status.
	A8AAC	Y		Add 8 to accumulator, results to accumulator. If carry, one to status.
	A10AAC	Y		Add 10 to accumulator, results to accumulator. If carry, one to status.
	A6AAC	Y		Add 6 to accumulator, results to accumulator. If carry, one to status.
	CPAIZ	Y		Complement accumulator and increment. If then zero, one to status.
Arithmetic Compare	ALEM	Y		If accumulator less than or equal to memory, one to status.
	ALEC	Y		If accumulator less than or equal to a constant, one to status
Logical Compare	MNEZ		Y	If memory not equal to zero, one to status.
	YNEA		Y	If Y register not equal to accumulator, one to status.
	YNEC		Y	If Y register not equal to a constant, one to status
Bits in Memory	SBIT			Set memory bit.
	RBIT			Reset memory bit.
	TBIT1		Y	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register.
	TCMIY			Transfer constant to memory and increment Y.
Input	KNEZ		Y	If K inputs not equal to zero, one to status.
	TKA			Transfer K inputs to accumulator.
Output	SETR			Set R output addressed by Y.
	RSTR			Reset R output addressed by Y.
	TDO			Transfer data from accumulator and status latch to O outputs.
	CLO			Clear O-output register.
RAM 'X' Addressing	LDX			Load 'X' with a constant.
	COMX			Complement 'X'.
ROM Addressing	BR			Branch on status = one.
	CALL			Call subroutine on status = one.
	RETN			Return from subroutine.
	LDP			Load page buffer with constant.

NOTES: C-Y (Yes) means that if there is a carry out of the MSB, status output goes to the one state. If no carry is generated, status output goes to the zero state.

N-Y (Yes) means that if the bits compared are not equal, status output goes to the one state. If the bits are equal, status output goes to the zero state.

A zero in status remains through the next instruction cycle only. If the next instruction is a branch or call and status is a zero, then the branch or call is not executed.

Program Development and Simulation

As shown in the flowchart for the TMS1000 series given in Figure 20, the program is written in assembly language using standard mnemonics. The assembler converts the source code (assembly language program) into machine code, which is transferred to a software simulation program. Also the assembler produces a machine code object deck. The object deck is used to produce a tape for hardware simulation or a tape for generating prototype tooling. The programs are checked by software and hardware simulation. The software simulation offers the advantages of printed outputs for instruction traces or periodic outputs. The hardware simulation offers the designer the advantages of real-time simulation and testing asynchronous inputs. A software user's guide is available. After the algorithms have been checked and approved by the customer, he supplies the final object code and machine option statements. A gate mask is generated, slices produced and devices assembled and tested.

Example: Register addition of up to fifteen b.c.d. digits. The add subroutine (whole flow chart is shown in Figure 21) can use the entire r.a.m., which is divided into two pairs of register. The definition of registers, for the purpose of illustration, is expanded to include the concept of a variable-length word that is a subset of a 16-digit file. Addition proceeds from the least significant digit (l.s.d.) to the most significant digit (m.s.d.), and carry ripples through the accumulator. The decrement – Y instruction is used to index the numbers in a register. The initial Y value sets the address for the l.s.d.s of two numbers to be added. Thus, if Y equals eight at the start, the l.s.d. is defined to be stored in M(X, 8), (M(X, Y) ≡ contents of r.a.m. word location X equals 0, 1, 2, or 3, and Y equals 0 to 15). If Y is eight initially, M(X, 7) is the next-most-significant digit. The r.a.m. data map before executing the sample routine is given in Table 8. In this registers D and G are nine digits long, and registers E and F are 16 digits long. The sample routine calls the D plus G→D subroutine and the E plus F→E subroutine. After executing the two subroutines, the r.a.m. data map is as given in Table 9 (Cross hatched areas indicate locations in the r.a.m. that are unaffected by executing the example routine). Table 10 shows how the program is arranged, with the main program controlling the use of the subroutines.

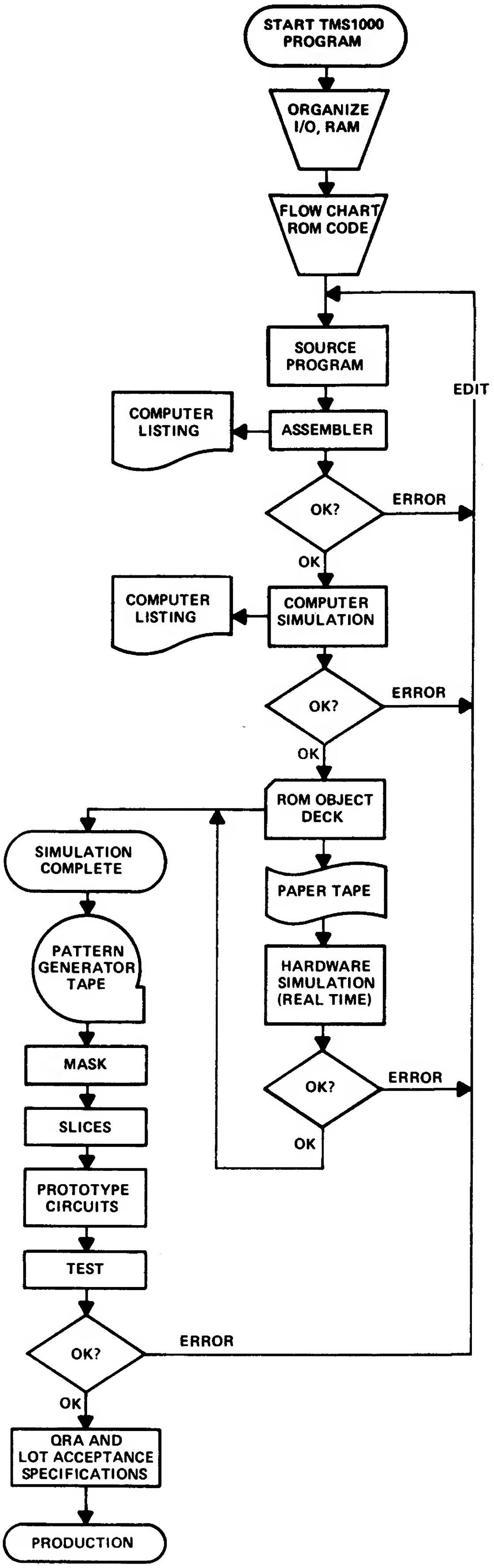
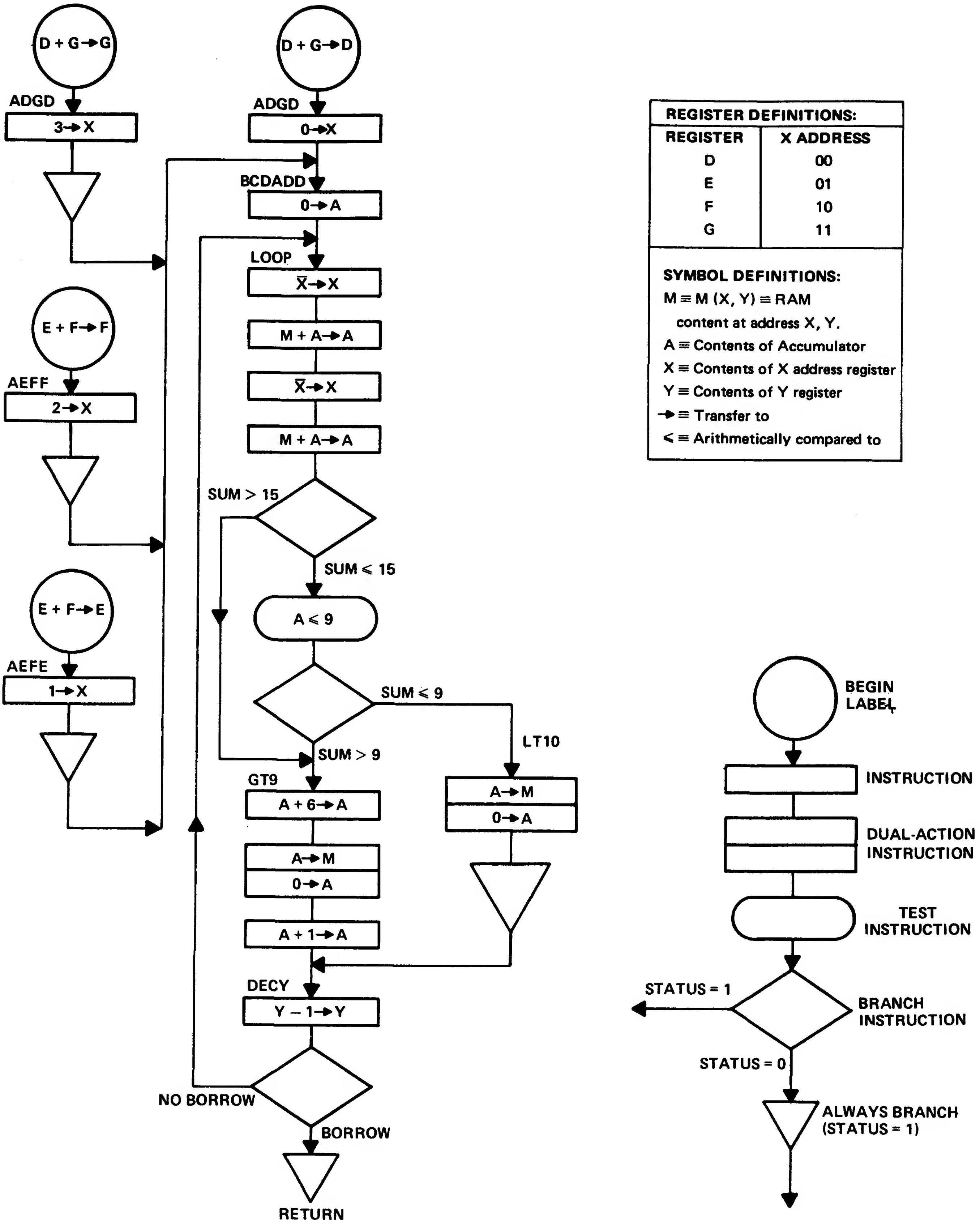

START TMS1000 PROGRAM
ORGANIZE I/O, RAM
FLOW CHART ROM CODE
SOURCE PROGRAM
EDIT
COMPUTER LISTING
ASSEMBLER
OK?
ERROR
OK
COMPUTER LISTING
COMPUTER SIMULATION
OK?
ERROR
OK
ROM OBJECT DECK
SIMULATION COMPLETE
PAPER TAPE
PATTERN GENERATOR TAPE
HARDWARE SIMULATION (REAL TIME)
MASK
OK?
ERROR
SLICES
OK
PROTOTYPE CIRCUITS
TEST
OK?
ERROR
OK
QRA AND LOT ACCEPTANCE SPECIFICATIONS
PRODUCTION

FIGURE 20. Algorithm Development Flowchart for TMS1000 Series


D + G→G
ADGD
3→X
D + G→D
ADGD
0→X
BCDADD
0→A
LOOP
X̄→X
M + A→A
X̄→X
M + A→A
E + F→F
AEFF
2→X
E + F→E
AEFE
1→X
SUM > 15
SUM ⩽ 15
A ⩽ 9
SUM ⩽ 9
LT10
SUM > 9
GT9
A + 6→A
A→M
0→A
A + 1→A
A→M
0→A
DECY
Y – 1→Y
NO BORROW
BORROW
RETURN
BEGIN LABEL
INSTRUCTION
DUAL-ACTION INSTRUCTION
TEST INSTRUCTION
STATUS = 1
BRANCH INSTRUCTION
STATUS = 0
ALWAYS BRANCH (STATUS = 1)

REGISTER DEFINITIONS:

REGISTER	X ADDRESS
D	00
E	01
F	10
G	11

SYMBOL DEFINITIONS:

M ≡ M (X, Y) ≡ RAM content at address X, Y.
A ≡ Contents of Accumulator
X ≡ Contents of X address register
Y ≡ Contents of Y register
→ ≡ Transfer to
⩽ ≡ Arithmetically compared to

FIGURE 21. Machine Instruction Flowchart – B.C.D. Addition Subroutine

Table 8. R.A.M. Data Map Before Executing Sample Routine

FILE ADDRESS	REGISTER	Y-REGISTER ADDRESS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X = 00	D	OV 0	MSD 9	8	7	6	5	4	3	LSD 2	▨	▨	▨	▨	▨	▨	▨
X = 01	E	OV 0	MSD 1	2	3	4	5	6	7	8	9	0	1	2	3	4	LSD 5
X = 10	F	OV 0	MSD 5	4	3	2	1	0	9	8	7	6	5	4	3	2	LSD 1
X = 11	G	OV 0	MSD 8	7	6	5	4	3	2	LSD 1	▨	▨	▨	▨	▨	▨	▨

Table 9. R.A.M. Data Map After Executing Sample Routine

FILE ADDRESS	REGISTER	Y-REGISTER ADDRESS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X = 00	D	OV 1	MSD 8	6	4	1	9	7	5	LSD 3	▨	▨	▨	▨	▨	▨	▨
X = 01	E	OV 0	MSD 6	6	6	6	6	7	7	7	6	6	6	6	6	6	LSD 6
X = 10	F	OV 0	MSD 5	4	3	2	1	0	9	8	7	6	5	4	3	2	LSD 1
X = 11	G	OV 0	MSD 8	7	6	5	4	3	2	LSD 1	▨	▨	▨	▨	▨	▨	▨

Table 10.

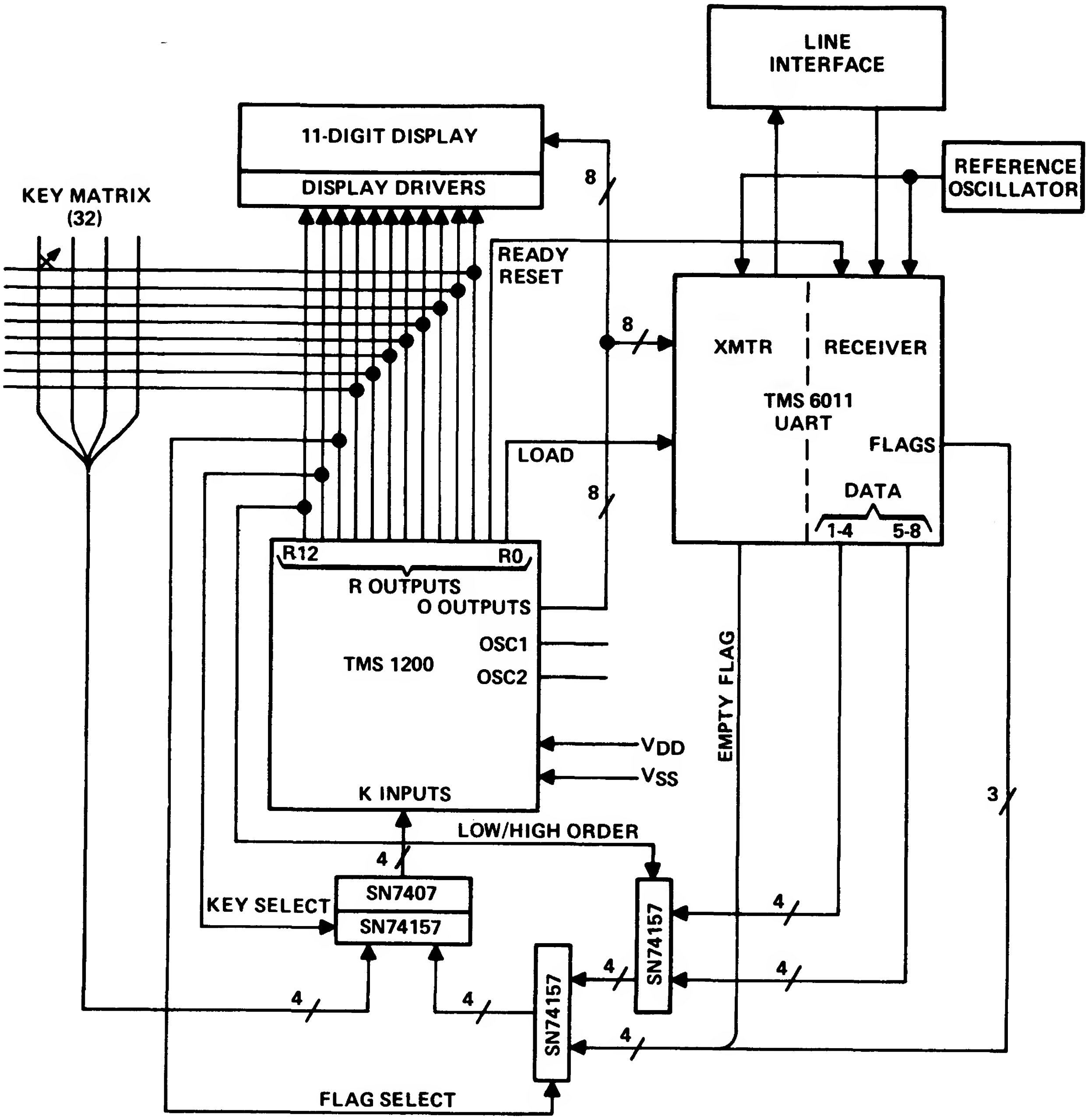
```
                    LABEL     OPCODE   OPERAND   COMMENT
MAIN PROGRAM      {           TCY      8         Transfer 8 → Y
PRESETS Y,        {           CALL     ADGD      Add: D + G → D
AND CALL          {           TCY      15        Transfer 15 → Y
SUBROUTINES       {           CALL     AEFE      Add: E + F → E


                  { ADGG      LDX      3         3 → X; Set up for D + G → G.
                  {           BR       BCDADD    Branch to BCD add.
MULTIPLE ENTRY    { AEFF      LDX      2         2 → X; Set up for E + F → F.
POINTS FOR        {           BR       BCDADD    Branch to BCD add.
SUBROUTINES       { AEFE      LDX      1         1 → X; Set up for E + F → E.
                  {           BR       BCDADD    Branch to BCD add.
                  { ADGD      LDX      0         0 → X; Add D + G → D.
                  { BCDADD    CLA                Clear accumulator (A).
                  { LOOP      COMX               X̄ → X.
                  {           AMAAC              M(X,Y) + A → A; A contains
                  {                              possible carry if in loop.
                  {           COMX               X̄ → X.
                  {           AMAAC              Add digits:
                  {                              M(X, Y) + [M(X̄ Y) + Carry] → A.
BASE              {           BR       GT9       Branch if sum >15.
SUBROUTINE        {           ALEC     9         If A ≤ 9, one to status.
CONTAINS          {           BR       LT10      Branch if sum < 10.
LOOPING           { GT9       A6AAC              Sum > 9, A + 6 → A,
AND               {                              BCD Correction.
BCD               {           TAMZA              Transfer corrected sum
CORRECTION        {                              to memory, 0 → A.
                  {           IA                 1 → A; to propogate carry
                  { DECY      DCYN               Y − 1 → Y; index next digit.
                  {           BR       LOOP      If no borrow, continue.
                  {           RETN               If borrow, return to
                  {                              instruction after call.
                  { LT10      TAMZA              Sum < 9, A → M(X,Y); 0 →A;
                  {                              No carry propogated.
                  {           BR       DECY
```

Note that there are four entry points to the base subroutine (ADGG, ADGD, AEFF, AEFE). The main program can call two of the other possible subroutines that store the addition results differently. These subroutines have applications in floating-point arithmetic, multiplication, division, and subtraction routines.

A Terminal Controller

Figure 22 shows a TMS1200 microcomputer used as the control part of a terminal controller system. The R OUTPUTS R2 to R12 strobe 7-segment and decimal point data into an 11-digit display. Additionally eight of the R OUTPUTS R2 to R9 scan four input lines from a keyboard. In this case the characters would be held in a look-up table in the TMS1200 r.o.m. and called-up according to the sequence of signals from the keyboard. Outputs R0 and R1 drive the transmitter and receiver respectively of a u.a.r.t.. Output R0 loads 8-bit output data into the u.a.r.t. transmitter register, while R1 either enables or resets the receiver register.[2]The u.a.r.t. communicates with a remote computer via the line interface. Output R12 selects the 'low' or 'high' order 4-bit bytes of the incoming received word via the first level of multiplexing with an SN74157 i.c. The second level of multiplexing, driven by output R10 selects either the control outputs (flags) from the u.a.r.t. or one of the data bytes previously selected. Finally the third SN74157 i.c. selects between incoming keyboard data or data bytes/flags from the u.a.r.t.. This is a good example of how a complex system can be implemented with a very low package count using this type of specially programmed microcomputer device. Similar applications are possible in most industrial mass produced control systems.


LINE INTERFACE
REFERENCE OSCILLATOR
11-DIGIT DISPLAY
DISPLAY DRIVERS
KEY MATRIX (32)
8
READY
RESET
8
XMTR
RECEIVER
TMS 6011 UART
FLAGS
DATA
1-4
5-8
LOAD
8
R12
R0
R OUTPUTS
O OUTPUTS
OSC1
OSC2
TMS 1200
VDD
VSS
K INPUTS
EMPTY FLAG
3
LOW/HIGH ORDER
4
SN7407
SN74157
KEY SELECT
SN74157
4
4
4
4
4
SN74157
4
FLAG SELECT

NOTE: Discrete components for level shifting and other functions are not shown

FIGURE 22. Block Diagram of a Terminal Controller

REFERENCES

1. Chapter XVI
2. Chapter XII

IX A SCHOTTKY TTL MICROCOMPUTER

by

Steve Craft and David A. Bonham

The first part of this chapter describes how a fast microprogrammable minicomputer may be built using Schottky t.t.l. devices. The heart of this microcomputer is the SN74S281 4 bit accumulator. The latter part of the chapter is devoted to describing the 'S281 and showing how it may be used to perform multiplication and division. As discussed in the previous chapter all microcomputers have a similar arrangement to the block diagram shown in Figure 1. The program, or programs, to be performed are listed as a series of steps. The steps of the program are stored in the instruction memory (i.m.) These address the control r.o.m. (c.r.o.m.) in sequence one at a time and the r.o.m. generates the control signals relevant to that instruction or step. The control signals from the c.r.o.m. govern the action of the memory, arithmetic/logic unit, input port and/or output port during an instruction by enabling inputs, outputs, loads and data and clock pathways. Feedback from these blocks can be used to branch the programs if conditions are correct. Thus program loops can be made and decisions can be taken. This also allows the program being performed to be 'interrupted' by a higher priority requirement. The initial program is stopped and the new, more important program started. It is possible to remember the condition of the processor just before the 'interrupt' and put it into store. When the interrupting program is completed the first program can be restored where it left off. The instruction set can be changed to execute a given task more efficiently, by programming the c.r.o.m.s. It is the latter which send out control signals at the correct instant in time to change data pathways and to load certain registers and memories in the machine. The outputs of the c.r.o.m.s completely control the action of the machine. Therefore, if these outputs are changed for a given input code, the action of the machine has been changed. For example: A certain input code could be interpreted, say, as the code to increment a specified register. The c.r.o.m.s would cause the accumulator contents to be temporarily stored in the 'push-down-file', the specified register would be loaded into the accumulator, incremented and reloaded into the register file. The accumulator is then rewritten with its original contents. However, by inserting new c.r.o.m.s a different function could be caused by the same input code. Therefore, instructions that were rarely used in a specific application could be changed for more useful instructions thus increasing the efficiency of execution of the task. This is the basis of microprogramming.

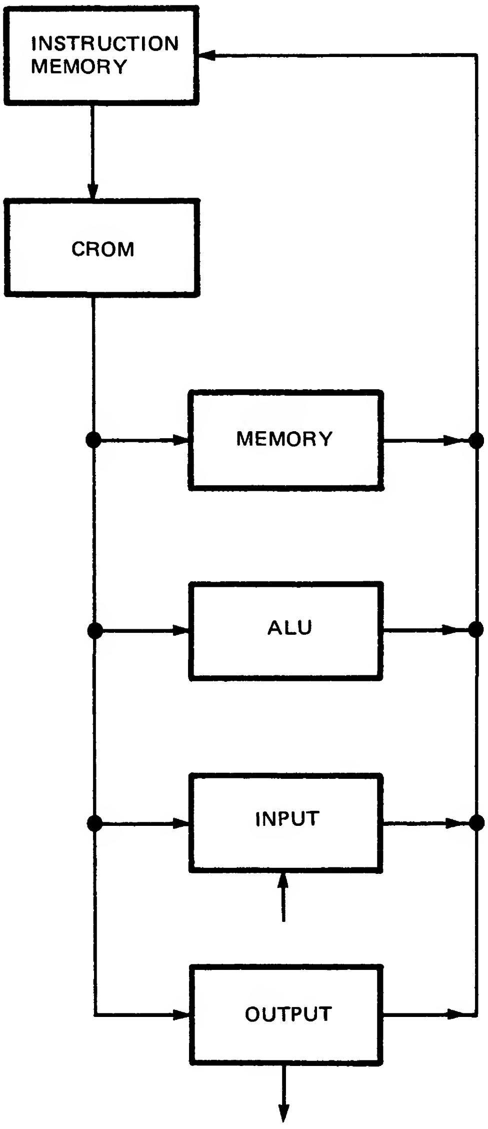


FIGURE 1. Basic Microcomputer Block Diagram

A FAST MICROPROCESSOR

The machine, which is shown in Figure 2, is 8 bits wide to match the architecture of the c.r.o.m.s used and to optimise package count, and was designed to operate at a state time of 150ns. Most instructions occupy 4 or 5 states. So a typical instruction time is 600 or 750ns. This is fairly fast, but the real test for a processor is the time taken to execute a given task, and this is also dependent on the machine instruction set. This processor has a flexible instruction set, i.e. it can be microprogrammed.

The Instruction Set

The c.r.o.m.s of this machine are programmed to give a set of basic instructions, which might be suitable for a general requirement. A typical instruction set is shown in Table 1. There are three basic types of instruction.

1. Control instructions which move data between the register file, accumulator and data memory, and also from the instruction memory.
2. Arithmetic instructions which cause arithmetic/logic functions to occur between the accumulator and the other data stores.
3. Software control instructions such as jumps and conditional jumps.

Control Instructions: Data in the i.m. is fixed, i.e. it can only be read, it cannot be written and temporarily stored in the i.m. Therefore, it is used mainly as a constant source. The remaining blocks have the ability to sink and source data. The register file is addressed by the last three bits of an instruction and therefore the instructions transferring data from i.m. to a register, or to and from register and accumulator, are only single byte instructions. The data memory (d.m.) is addressed in two modes, either direct, with it address supplied from i.m. as part of the instruction, or by the indexed mode. This mode uses the memory address register (m.a.r.) as an index register. The required address is generated by adding to the value in the index register, an increment, supplied from i.m. as part of the instruction. The new address is then loaded into the m.a.r. which addresses the correct store in the d.m. This is now the new value of the index register. The index addressing facility is extremely useful in the list processing type of problem.

Arithmetic Instruction: The arithmetic/logic instructions are three byte instructions. They operate on the present value of the accumulator, and data which is obtained from i.m., d.m. or register file. The operator is defined by the third byte from i.m. These 8 bits completely control the actions of the accumulator. The results of the arithmetic/logic operations are stored in the accumulator.

Software Instructions: The software control statements available are instructions such as conditional or unconditional jumps, subroutine jumps and return from subroutines. The conditions are teletype keyboard not ready, printer not ready, non-zero-accumulator, non underflow or overflow, least significant bit detection (used in multiplication) and one spare user condition. The conditions are all inverse, i.e. jump if the condition is not true. This is because with the specified conditions, the program is normally required to repeat as task if the condition has

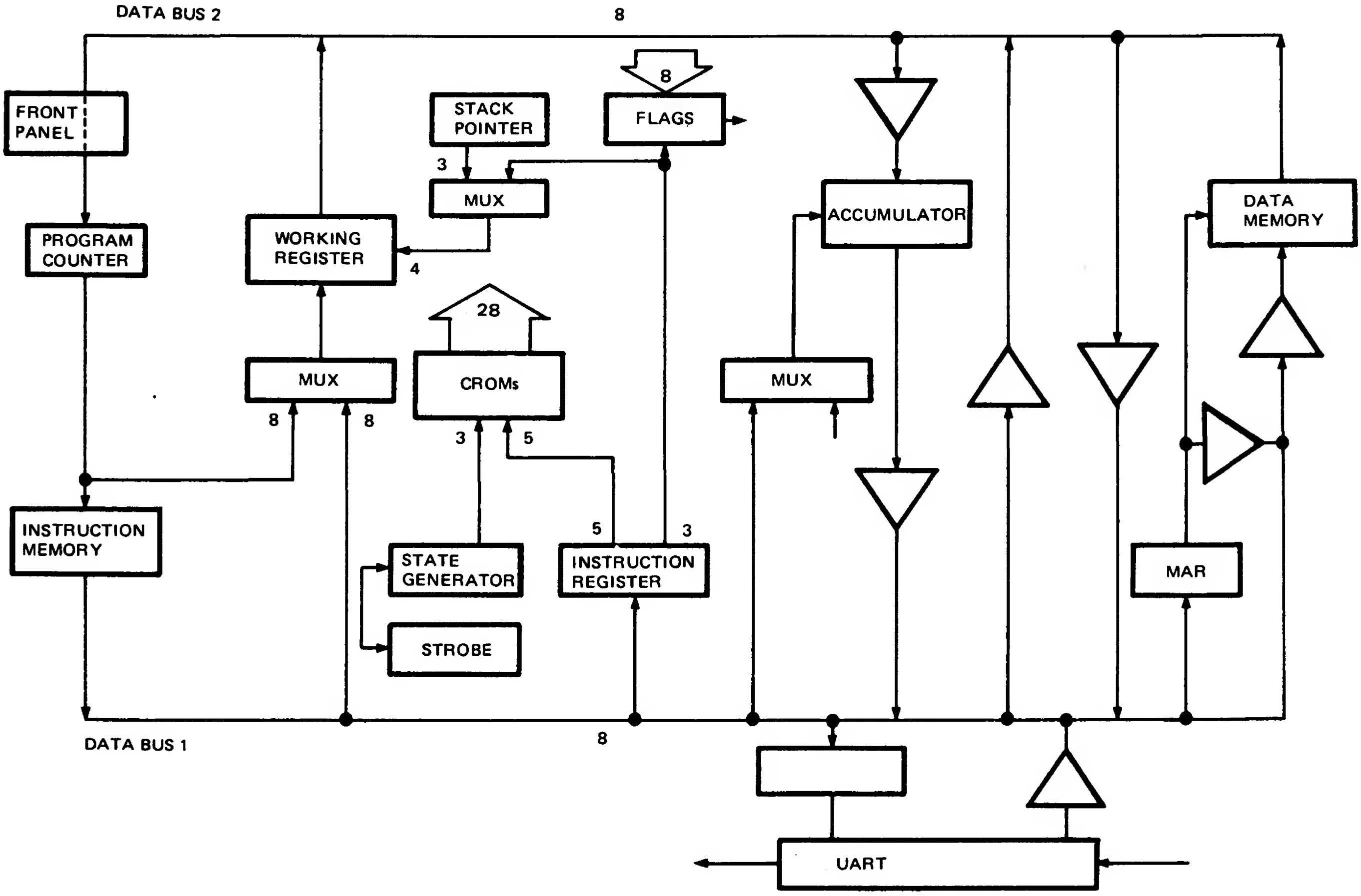


FIGURE 2. Block Diagram of Schottky Fast Microprocessor

Table 1. Typical Instruction Set

Instruction	**Mnemonic**	**Alternatives**	**Bytes**	**Code**
Load register Immediate	LDRI	R0 → R7	2	AH → AO; Data
Load register from accumulator	LDRA	R0 → R7	1	B0 → B7
Load register from memory	LDRD	R0 → R7	2	BH → BO; Address
Load register from memory (indexed)	LRDX	R0 → R7	2	G0 → G7; Increment
Increment register	INR	R0 → R7	1	CH → CO
Decrement register	DER	R0 → R7	1	D0 → D7
Load accumulator Immediate	LDAI		2	DH; Data
Load accumulator from register	LDAR	R0 → R7	1	E0 → E7
Load accumulator from memory	LDAD		2	RH; Address
Load accumulator from memory (indexed)	LDAX		2	EH; Increment
Load index register Immediate	LDXI		2	IH; Data
Load index register from memory	LDXD		2	JP; Address
Load index register from accumulator	LDXA		1	II
Store register in memory	STRD	R0 → R7	2	F0 → F7 Address
Store register in memory (indexed)	STRX	R0 → R7	2	FH → FO Increment
Store accumulator in memory	STAD		2	G0; Address
Store accumulator in memory (indexed)	STAX		2	GI; Increment
Store in memory Immediate	STID		2	MP; Address
Store in memory Immediate (indexed)	STIX		2	MH; Increment
Store index in memory	STXD		2	LP; Address
Store index in accumulator	STXA		1	KH; Address
Increment index register by N	INX		2	JH; Increment
Decrement index register by N	DEX		2	KP; Decrement
Input to accumulator	IPA		1	LH
Output from accumulator	OPA		1	LI
Jump	JMP		2	PH; Address
Jump conditional	JMP C	Conditions	2	
		$\overline{\text{Printer ready}}$		PK; Address
		$\overline{\text{Keyboard ready}}$		PJ; Address
		$\overline{\text{Acc zero}}$		PL; Address
		$\overline{\text{Carry out}}$		PM; Address
		$\overline{\text{LSB Acc}}$		PN; Address
		External		PO; Address
Jump to subroutine	JMS		2	PP; Address
Jump to subroutine conditional	JMS C	C1 → C6	2	PB → PG; Address
Return from subroutine	RTN		1	A0
Return from subroutine conditional	RTN C	C1 → C6	1	AB → AG
Arithmetic logic function Immediate	ALF I		3	GH Data; control
With register	ALFR	RO → R7	2	H0 → H7; control
With memory	ALFD		3	HH; Address; control
With memory (indexed)	ALFX		3	IP; Increment; control

Control decides function performed

Arithmetic	Acc – Data	PL
Arithmetic	Data – Acc	PJ
Arithmetic	Acc + Data	PF
Logic	Data ● Acc	AA
Logic	$\overline{\text{Data} \bullet \text{Acc}}$	AC
Logic	Data + Acc	AG
Logic	$\overline{\text{Data} + \text{Acc}}$	AE
Logic	$\overline{\text{Data} \oplus \text{Acc}}$	AB
Logic	Data ⊕ Acc	AD
Logic	Shift Data Right	DA
Logic	Shift Data Left	BA
Arithmetic	Shift Data Right	LA
Arithmetic	Shift Data Left	JA
Load and Shift Right		DC
Load and Shift Left		BC

not been met, and so this organisation means fewer instructions to achieve looping. There are also instructions which load and store the index register, and have the ability to increment or decrement the index register by any amount up to 255.

Sections

The microcomputer can be conveniently broken down into seven sections.

Instruction Memory (i.m.): At present this memory is a random access memory (r.a.m.) due to the need to change the test programs quickly and economically. The r.a.m. is 256 bytes, i.e. 256 x 8 bits and is comprised of eight SN74S200 packages, with a maximum access time from address of 50ns, typically 33ns. The i.m. is addressed by two SN74LS197 chips forming the 8 bit program counter (p.c.). The counters are programmable thus enabling jumps as well as sequential stepping through the program. Eventually when the operating program is fixed the r.a.m.s can be replaced by p.r.o.m.s such as the SN74S287. Figure 3 shows the two alternative configurations.

Instruction Decode: This section has two SN74S175 devices forming the instruction register (i.r.) which stores each instruction to be decoded. As shown in Figure 4 the instruction decode is performed by 7 c.r.o.m.s. These are SN74S387, 256 x 4 bits p.r.o.m.s. The first five bits in the i.r. specify which instruction is to be performed. (The remaining three bits are used for register or conditional definitions). The 5 bits are fed to the most significant addresses of the c.r.o.m.s. The 3 least significant c.r.o.m. addresses are provided by the state generator which in turn is driven by the machine clock. Thus for each of the 32* available instructions there are eight available states during which the c.r.o.m.s output control signals to cause correct execution of the instruction. There are seven c.r.o.m.s which give 28 separate control signals. These comprise such signals as increment program counter, enable working register, load working register, etc. Certain control signals are 'strobe-enabled' halfway through the state, to improve system noise immunity.

A simple example of the way in which an instruction is decoded and executed is given below. For example if the instruction to be performed is Load Working Register 3 from accumulator, then the i.r. is loaded during state 0. The code for this instruction is thus presented to the five most significant addresses of the c.r.o.m.s enabling them to give the correct control signals for that instruction during the subsequent states. The clock increments the state generator and the c.r.o.m.s give the control signals for state 1 of this instruction. This enables the working register file (addressed by the last 3 bits of the instruction, in this case register 3). It also enables the data pathway between accumulator and working register and activates the write input to the register file, causing the 8 bits of information present in the accumulator to be written into working register 3. State 2 causes the p.c. to be incremented thus presenting the next instruction to the i.r. State 3 causes the state generator to reset to State 0, which as above causes a new instruction to be loaded. This resetting procedure means the machine does not have to run through unused states, thus on average considerably speeds up the operation of the machine. Table 2 lists the output signals from the c.r.o.m.s.

Table 2. C.R.O.M. Control Signals.

C.R.O.M. 1	1.	Load instruction register.
	2.	Increment program counter.
	3.	Enable register file.
	4.	Write in register file.
C.R.O.M. 2	1.	Program counter to register pathway.
	2.	Clock Push-Down store.
	3.	Load accumulator.
	4.	Clock accumulator.
C.R.O.M. 3	1.	Reset state generator.
	2.	Enable Push-Down store capability.
	3.	Write in Push-Down.
	4.	Load Program counter.
C.R.O.M. 4	1.	Load output register.
	2.	Enable flags.
	3.	Increment accumulator.
	4.	Control Accumulator with second byte.
C.R.O.M. 5	1.	Enable instruction memory.
	2.	Enable Data memory.
	3.	Enable input buffer.
	4.	Write in memory.
C.R.O.M. 6	1.	Load memory address register.
	2.	Enable m.a.r. output buffer.
	3.	Increment m.a.r.
	4.	Enable accumulator output.
C.R.O.M. 7	1.	Not used.
	2.	Enable TMS6011 u.a.r.t.
	3.	Add Accumulator
	4.	Sub.

Arithmetic Logic Unit (a.l.u.): This is made up of two SN74S281 chips. These are 4 bit parallel binary accumulators, containing a storage register B. The accumulator can perform eight arithmetic and seven logic functions between register B and the external input A. The B register is also capable of shifting one place at a time left or right in logical mode or arithmetic mode, (where the maximum significant bit is treated as a sign bit and is not shifted). There are eight control inputs to these devices and thus the accumulator can be completely controlled by 1 byte of data. Therefore, one arithmetic/logic instruction denoting action between the accumulator and, say, the working register stack, can in fact be broken down into 25 smaller instructions such as exclusive OR between accumulator and register or addition or subtraction, etc. These smaller instructions are defined by a second byte from the i.m. fed

---

* There are in fact 100 available instructions due to bit manipulation.

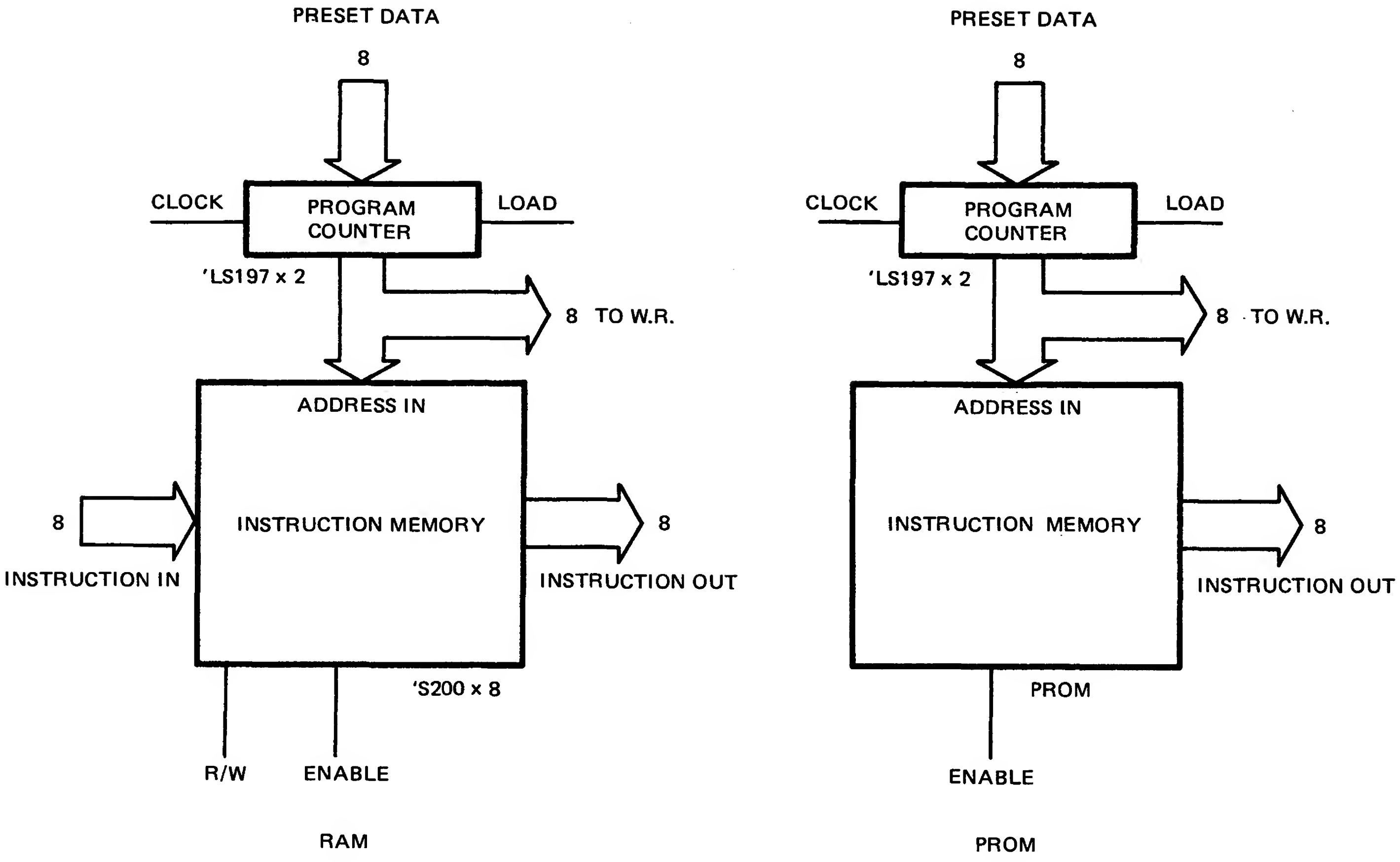

PRESET DATA
8
CLOCK
PROGRAM COUNTER
LOAD
'LS197 x 2
8 TO W.R.
ADDRESS IN
8
INSTRUCTION IN
INSTRUCTION MEMORY
8
INSTRUCTION OUT
'S200 x 8
R/W
ENABLE
RAM
PRESET DATA
8
CLOCK
PROGRAM COUNTER
LOAD
'LS197 x 2
8 TO W.R.
ADDRESS IN
INSTRUCTION MEMORY
8
INSTRUCTION OUT
PROM
ENABLE
PROM

FIGURE 3. Instruction Memory

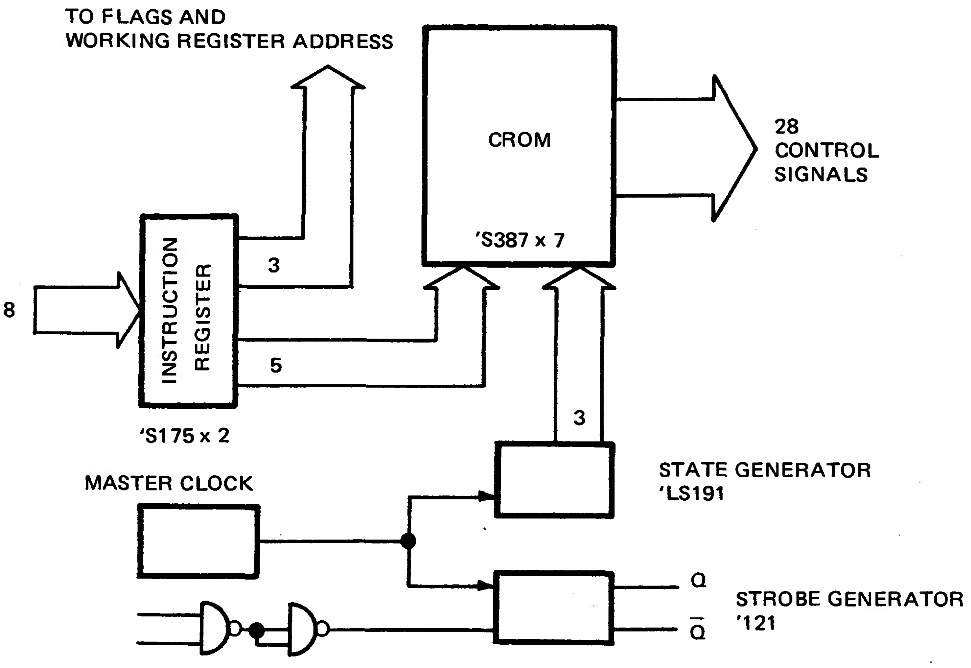

TO FLAGS AND
WORKING REGISTER ADDRESS
CROM
'S387 x 7
28
CONTROL
SIGNALS
8
INSTRUCTION REGISTER
3
5
'S175 x 2
3
MASTER CLOCK
STATE GENERATOR
'LS191
Q
$\bar{Q}$
STROBE GENERATOR
'121

FIGURE 4. Control Read Only Memory

to the a.l.u. via a multiplexer as shown in Figure 5. For instructions other than arithmetic/logic the multiplexer allows the a.l.u. to be controlled by the c.r.o.m.s. Then instruction elements such as: ready to be loaded, or to increment the B register, can be implemented without requiring an extra control byte.

Working Register and Push-Down Store: The working register is made up of two SN74S189 random access memories giving a 16 x 8 register file. Figure 6 shows the working register, its associated logic and the flag multiplexer. This file has been split into two parts. The first half is used as a normal register file of eight words, the second half is used as a push-down store, i.e. last-in-first-out. This is extremely useful to store subroutine return addresses and enables subroutine nesting of up to seven levels. The register stack is addressed by a multiplexer SN74S158, one set of the inputs is fed by the last 3 bits of the i.r. and a hardwired '0' for use as a normal register file, the other set of inputs is fed by an SN74LS191 up/down counter and a hardwired '1'. When a subroutine is called the c.r.o.m.s transfer control of the register stack addresses to the counter,

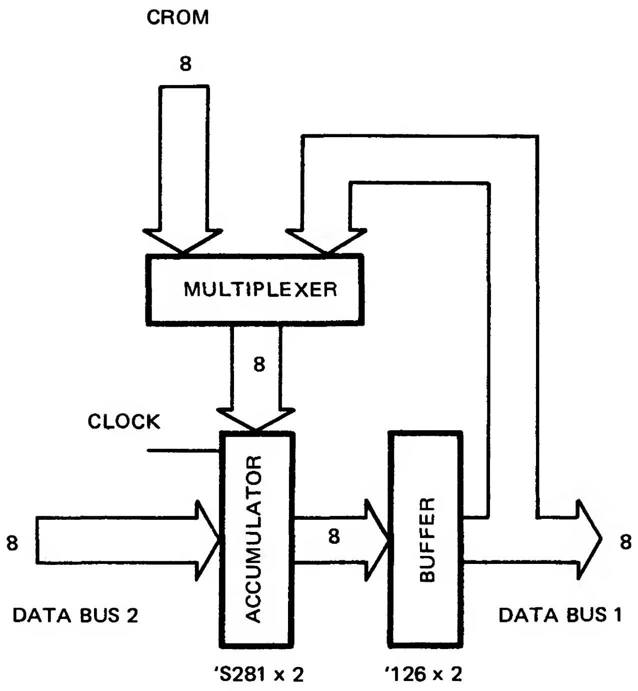

CROM
8
MULTIPLEXER
8
CLOCK
ACCUMULATOR
BUFFER
8
8
8
DATA BUS 2
DATA BUS 1
'S281 x 2
'126 x 2

FIGURE 5. Arithmetic Logic Unit

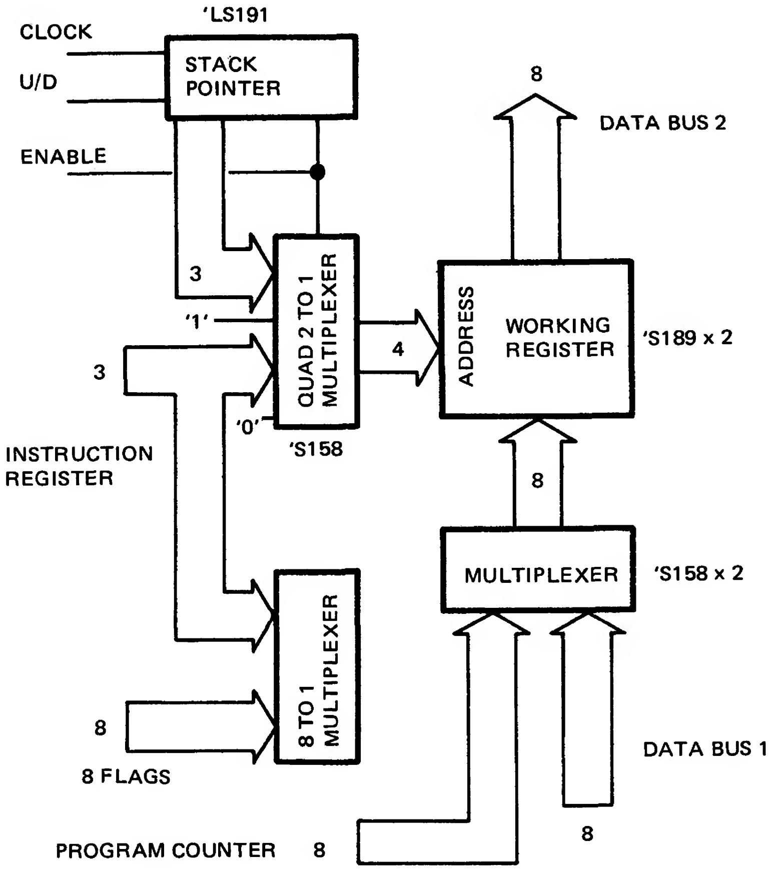

CLOCK
U/D
'LS191
STACK POINTER
ENABLE
3
'1'
3
'0'
QUAD 2 TO 1 MULTIPLEXER
'S158
4
ADDRESS
WORKING REGISTER
'S189 x 2
8
DATA BUS 2
8
MULTIPLEXER
'S158 x 2
INSTRUCTION REGISTER
8 TO 1 MULTIPLEXER
8
8 FLAGS
DATA BUS 1
PROGRAM COUNTER
8
8

FIGURE 6. Working Register and Flag Multiplexer

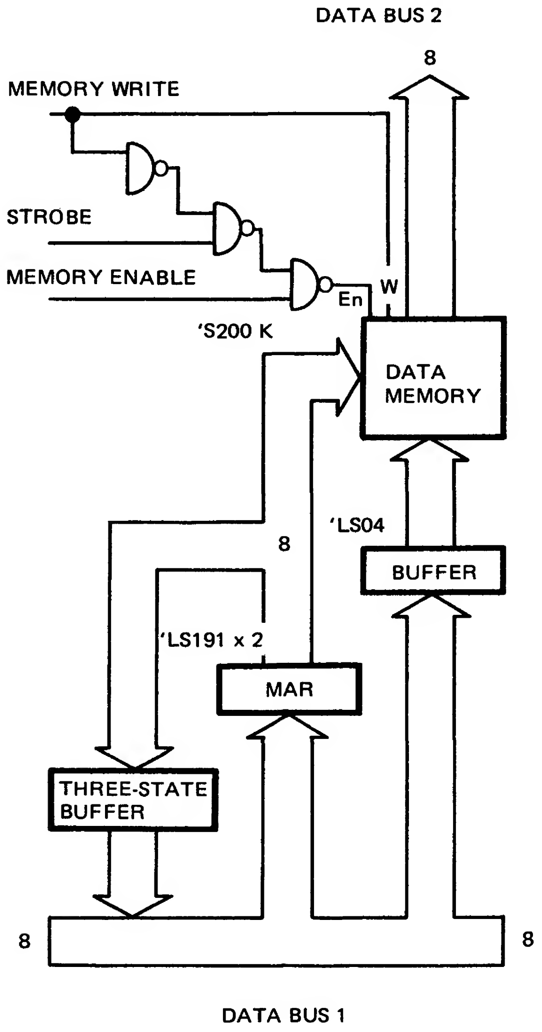

DATA BUS 2
8
MEMORY WRITE
STROBE
MEMORY ENABLE
En
W
'S200 K
DATA MEMORY
'LS04
BUFFER
8
'LS191 x 2
MAR
THREE-STATE BUFFER
8
8
DATA BUS 1

FIGURE 7. Data Memory

which is told when and in which direction to count. These registers are fast; typically 25ns from address to output. They are also easy to address, needing no extra byte from the i.m. Thus they are very useful as a 'scratchpad' memory.

Main Memory: The microprocessor is capable of accessing 64k bytes of memory. This is achieved by loading the 16 bit memory address register with 2 bytes from i.m. in the direct addressing mode, and by sensing overflow or underflow of the accumulator in the indexed mode. The arrangement of a memory of 256 bytes is shown in Figure 7.

Flags: The flags or condition flip-flops are fed into the inputs of a SN74LS151 multiplexer, addressed by the last 3 bits of the i.r. The state of the selected flag determines whether or not a jump instruction is executed. This is achieved by allowing the multiplexer output, when enabled, to influence the incremental program counter control signal.

Input/Output: These functions are controlled by 2 five bit instructions: The remaining 3 bits of each 8 bit instruction may be used to define which of the eight input/output ports is used. Both instructions operate via the accumulator. The input instruction is microprogrammed to perform an echo data signal to the teletype. Thus the teletype will print out the data that is entered without requiring an additional output instruction.

THE SN74S281 4 BIT ACCUMULATOR

Description

This device can be cascaded to any number of bits and look-ahead-carry technique can be added to cascaded packages. One look-ahead-carry device, the 'S182, is used to every four accumulator packages. The 'S281 consists of a fast 4 bit a.l.u. and a multi-mode shift register. They are connected to each other as shown in Figure 8. The a.l.u.

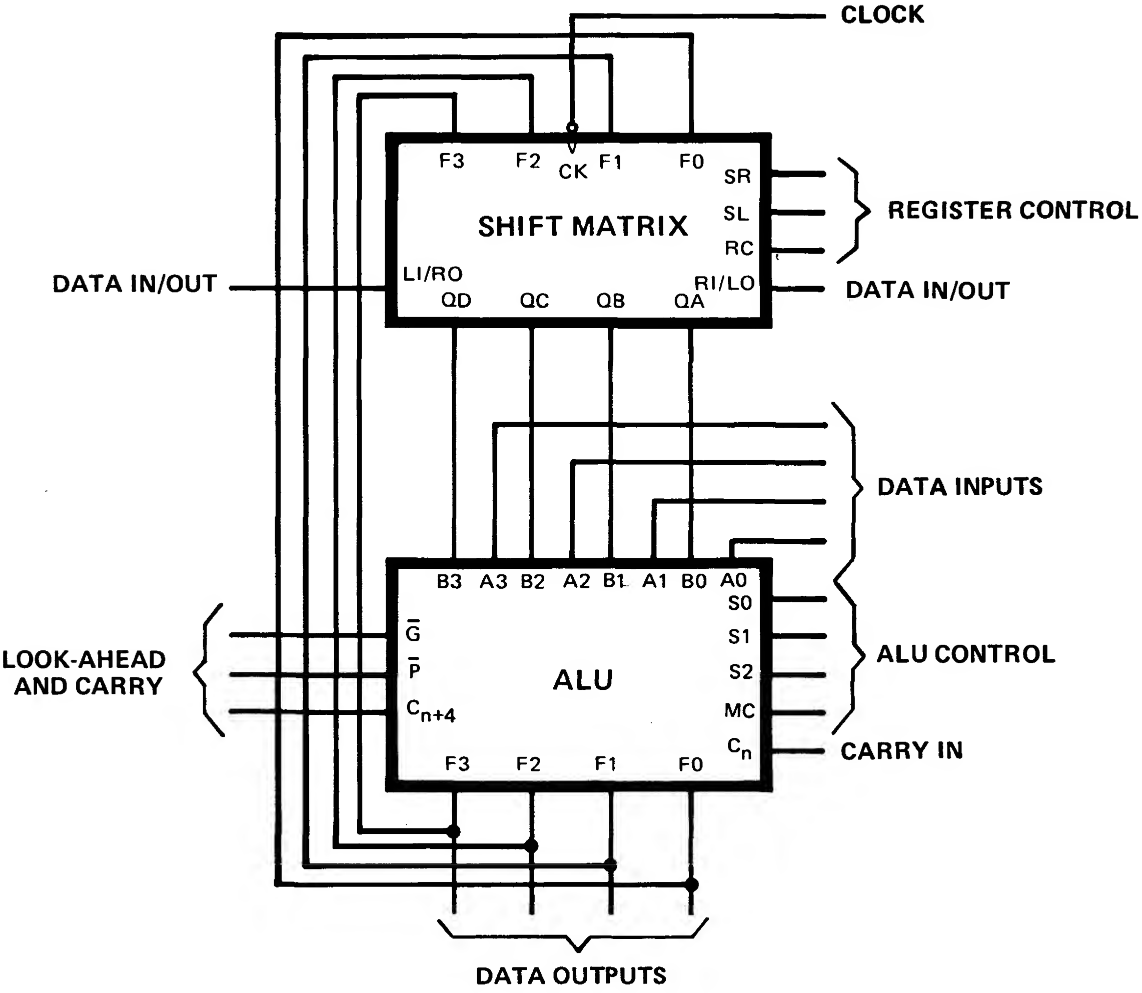

CLOCK
F3
F2
CK
F1
F0
SR
SL
RC
SHIFT MATRIX
REGISTER CONTROL
DATA IN/OUT
LI/RO
RI/LO
QD
QC
QB
QA
DATA IN/OUT
DATA INPUTS
B3 A3 B2 A2 B1 A1 B0 A0
S0
S1
S2
MC
C_n
$\bar{G}$
$\bar{P}$
C_{n+4}
ALU
LOOK-AHEAD AND CARRY
ALU CONTROL
CARRY IN
F3
F2
F1
F0
DATA OUTPUTS

FIGURE 8. 4-Bit Parallel Binary Accumulator

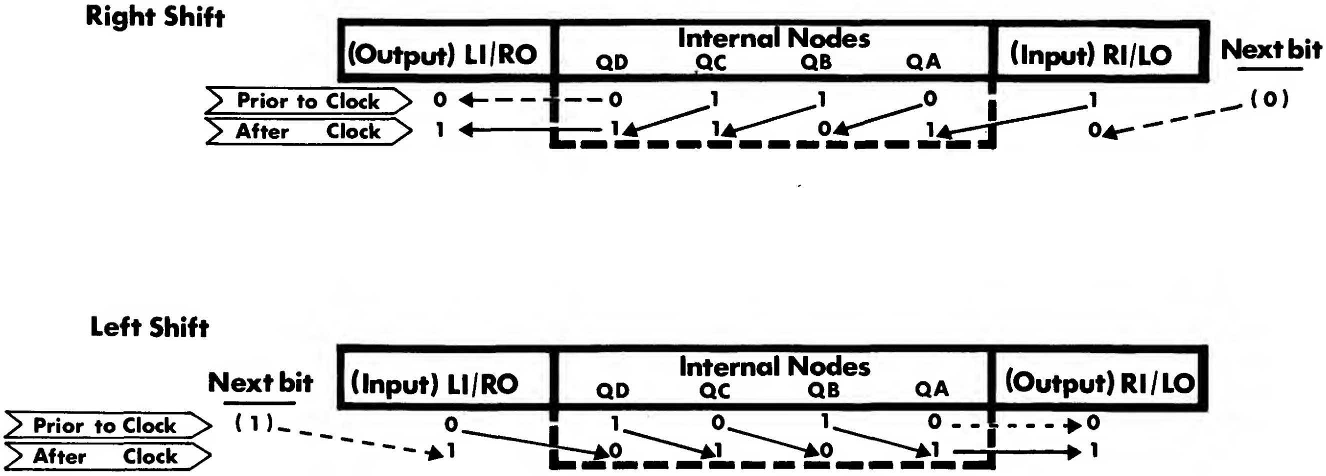

Right Shift
(Output) LI/RO
Internal Nodes
QD
QC
QB
QA
(Input) RI/LO
Next bit
Prior to Clock
After Clock
0
0
1
1
0
1
(0)
1
1
1
0
1
0
Left Shift
Next bit
(Input) LI/RO
Internal Nodes
QD
QC
QB
QA
(Output) RI/LO
Prior to Clock
After Clock
(1)
0
1
0
1
0
0
1
0
1
0
1
1

FIGURE 9. Logic Shifting with the 'S281 Accumulator

can perform eight arithmetic operations such as adding, subtracting and complimenting and seven logic operations such as NANDing, NORing and exclusive ORing. The shift register is of four bits with parallel entry and exit from and to the a.l.u. There are also two 3-state serial input/output terminals. Each terminal becomes an output or an input according to the direction of shift. An unusual feature of the shift register is that it has two methods of shifting—the normal mode as shown in Figure 9 and called logical shifting, and the mode shown in Figure 10 called arithmetic shifting. This second mode needs some explanation. When doing an arithmetic operation the sign of a number has to be stored if both positive and negative numbers can be involved. It can either be in a separate sign store or associated with the number as its most significant bit. If the latter way is used, then normal shifting will move the sign bit and the most significant position will then contain other data. When the 'S281 is in its arithmetic shift mode then the data at output Q_D is not shifted. Thus output Q_D can be used as a sign bit. When 'S281s are cascaded to make a word of more than 4 bits then obviously only the most significant package should be used in arithmetic mode.

Operation

Numbers to be manipulated must be presented to the A and B inputs of the a.l.u. Although the A inputs come from the data input terminals the B inputs come from the shift register. Thus the entry B must be first loaded into the shift register. The path of the data from input to store output looks complicated, but it is not difficult to negotiate. There are control inputs to the a.l.u. and register

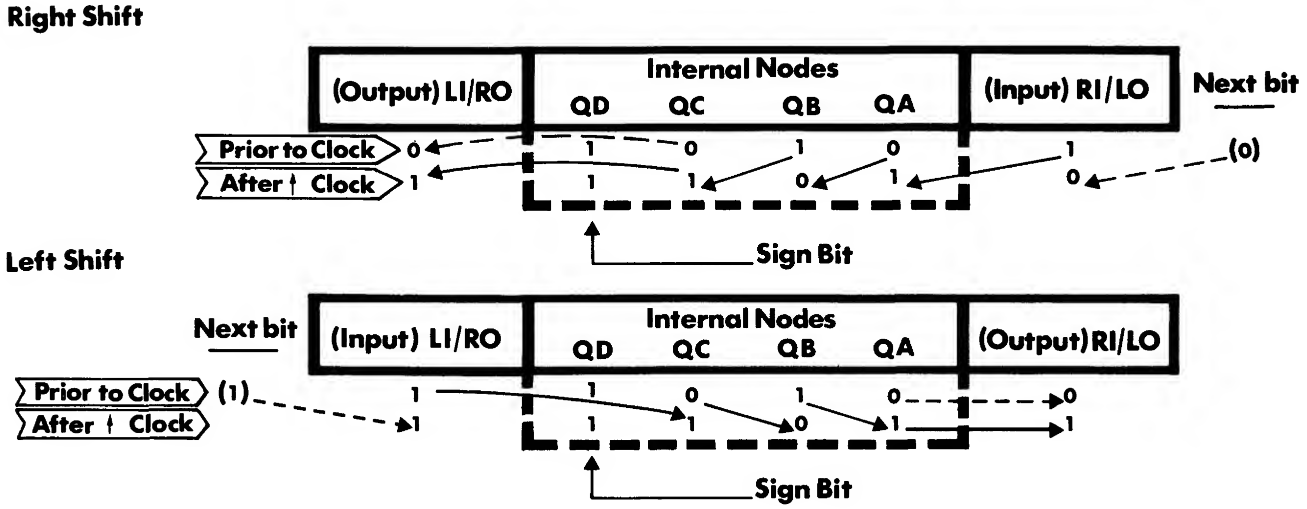

Right Shift
(Output) LI/RO
Internal Nodes
QD
QC
QB
QA
(Input) RI/LO
Next bit
Prior to Clock
After ↑ Clock
0
1
1
1
0
1
1
0
0
1
1
0
(0)
Sign Bit
Left Shift
Next bit
(Input) LI/RO
Internal Nodes
QD
QC
QB
QA
(Output) RI/LO
Prior to Clock
After ↑ Clock
(1)
1
1
1
1
0
1
1
0
0
1
0
1
Sign Bit

FIGURE 10. Arithmetic Shifting

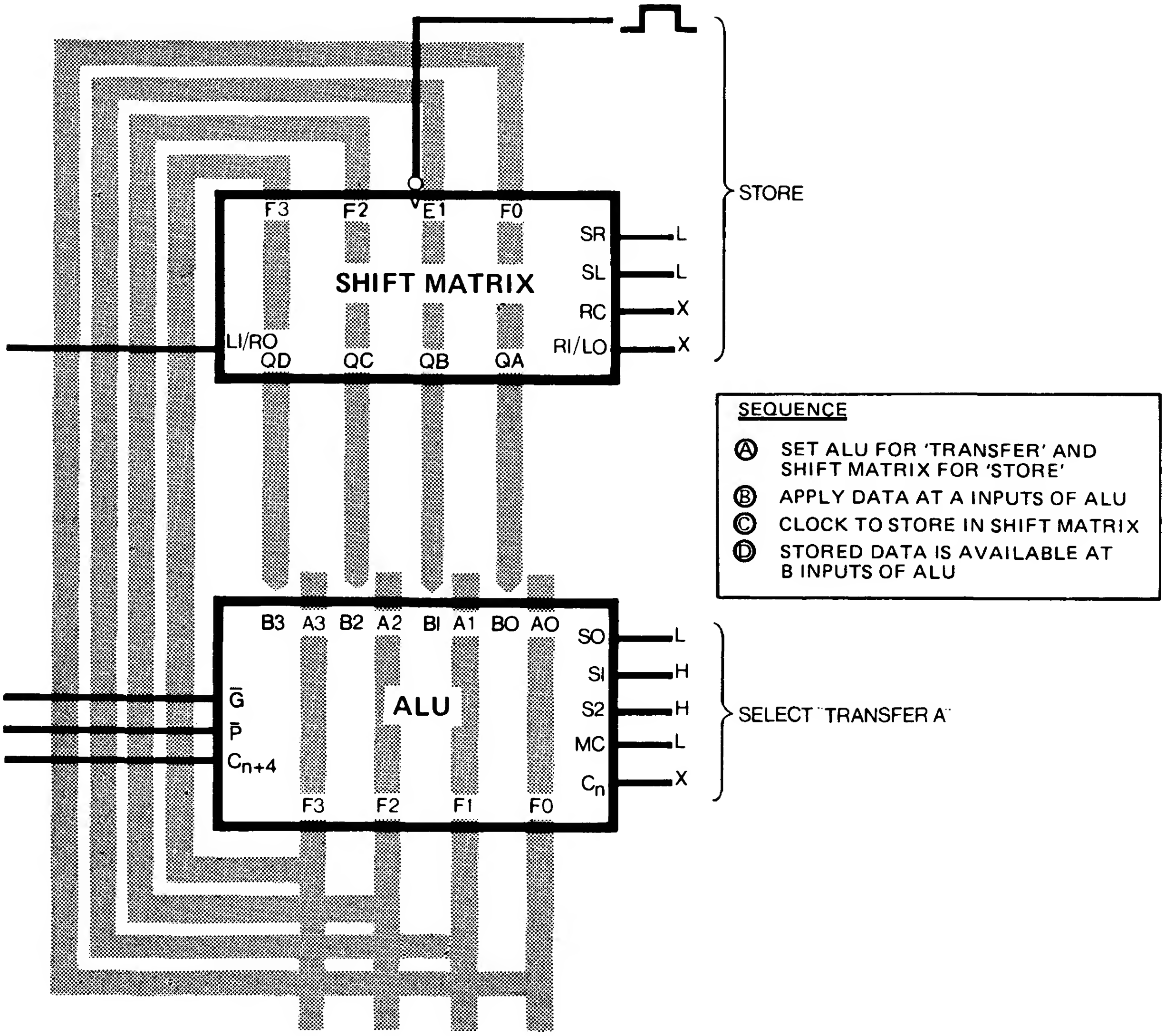
which select which of the available functions is performed. Those of the a.l.u. are set to 'Transfer A' ($F_n = A_n$) and those of the register are set to store. On the next clock edge the data at the package inputs appears at the register outputs. This is shown diagramatically in Figure 11.

Addition, say, of A and B can now be performed. At the same time the answer could be shifted one place. (Adding and shifting, and subtracting and shifting are steps in the algorithms for binary multiplication and subtraction). To do an Add and Shift the a.l.u. controls are set to add ($F_n = A_n$ plus B_n) and the register controls to shift right. The sum of A plus B will now be stored, shifted one place to the right, at the register outputs. Figure 12 shows this operation.

Table 3 shows an example of the Add and Shift technique of multiplication by the standard algorithm. The least significant bit of the multiplier is inspected, and, if it is a '1', then the multiplicand is added into an accumulator. The multiplicand is then shifted one place more significant. The step is then repeated adding in the multiplicand whenever the multiplier bit is a '1'. This method is analogous to the pencil and paper method of long multiplication of binary numbers except that each sub-product is added in as it is produced instead of adding together all subproducts at the end. There is an alternative

Table 3. Binary Multiplication by the Normal Algorithm

Multiplicand	1101	Thirteen
Multiplier	1011	Eleven
	1101	Multiplier LSB "1" add Multiplicand to Zero
	1101	Next Multiplier Digit "1" Shift Multiplicand and add
	100111	Next Multiplier Digit "0" Shift Multiplicand
	1101	Next Multiplier Digit "1" Shift Multiplicand and add
	10001111	One Hundred and Forty Three



SEQUENCE

Ⓐ SET ALU FOR 'TRANSFER' AND SHIFT MATRIX FOR 'STORE'
Ⓑ APPLY DATA AT A INPUTS OF ALU
Ⓒ CLOCK TO STORE IN SHIFT MATRIX
Ⓓ STORED DATA IS AVAILABLE AT B INPUTS OF ALU

FIGURE 11. Data Flow for Loading Accumulator

Table 4. Binary Multiplication

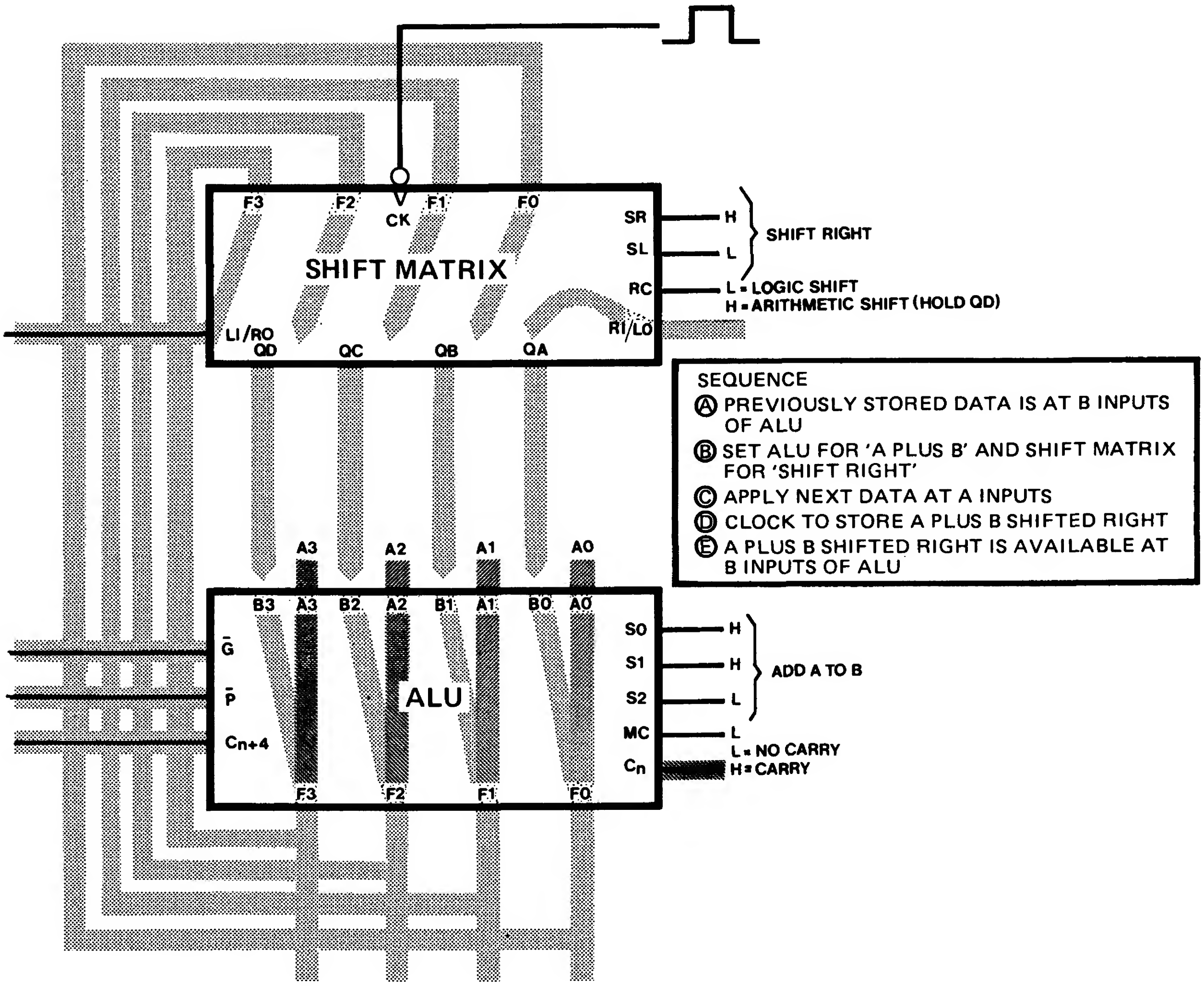
Eleven	1011	Multiplicand
Nine	1001	Multiplier
	1011	Add Multiplicand to Accumulator
	1011	Right Shift one place
	1011	Right Shift one place
	1011	Right Shift one place
	1011	
	1100011	Add Multiplicand to Accumulator
Ninety-Nine	1100011	Shift Accumulator

Rule
Inspect Multiplier one Bit at a time
LSB first.
If Multiplier Bit is "1" add Multiplicand to
Accumulator and shift Accumulator one place right
If Multiplier Bit is "0" shift Accumulator one place right

method which is shown in Table 4. Again the multiplier is inspected l.s.b. first, and the multiplicand is added into the accumulator if the bit is a '1'. However, the multiplicand is not shifted at each step. The accumulated value is shifted one place less significant. This has the advantage that a four bit adder can be used to produce an eight bit product. A seven bit adder would be required for the first method.

Multiplier

A 'S281 and two four bit registers together with some control logic can be used to make such a 4 by 4 bit multiplier. A block diagram of the arrangement is shown in Figure 13. The multiplicand is loaded and stored in a 'S195, 4 bit shift register. The multiplier is also loaded into a 'S195, the multiplier product (m.p.) register. The control logic determines the functions of the a.l.u. and shift registers (i.e. the accumulator register and the m.p. register). Having managed the loading it inspects the least significant output of the m.p. register and in accordance with the algorithm of Table 4 adds or does not add the multiplicand to the accumulator. It then produces a shift clock to control the accumulated value in the registers. The second bit of the multiplier is now at the least significant output of the m.p. register, and the (add/not add) and shift can be repeated for a further three cycles. Then the multiplier will have been displaced and replaced by the four less significant bits of the product, while the four more significant bits of the multiplier will be in the accumulator register. Setting the controls of the a.l.u. to transfer ($F_n = B_n$) will produce them at the outputs of the 'S281.



SEQUENCE
Ⓐ PREVIOUSLY STORED DATA IS AT B INPUTS OF ALU
Ⓑ SET ALU FOR 'A PLUS B' AND SHIFT MATRIX FOR 'SHIFT RIGHT'
Ⓒ APPLY NEXT DATA AT A INPUTS
Ⓓ CLOCK TO STORE A PLUS B SHIFTED RIGHT
Ⓔ A PLUS B SHIFTED RIGHT IS AVAILABLE AT B INPUTS OF ALU

FIGURE 12. Data Flow for Add-and-Shift-Right

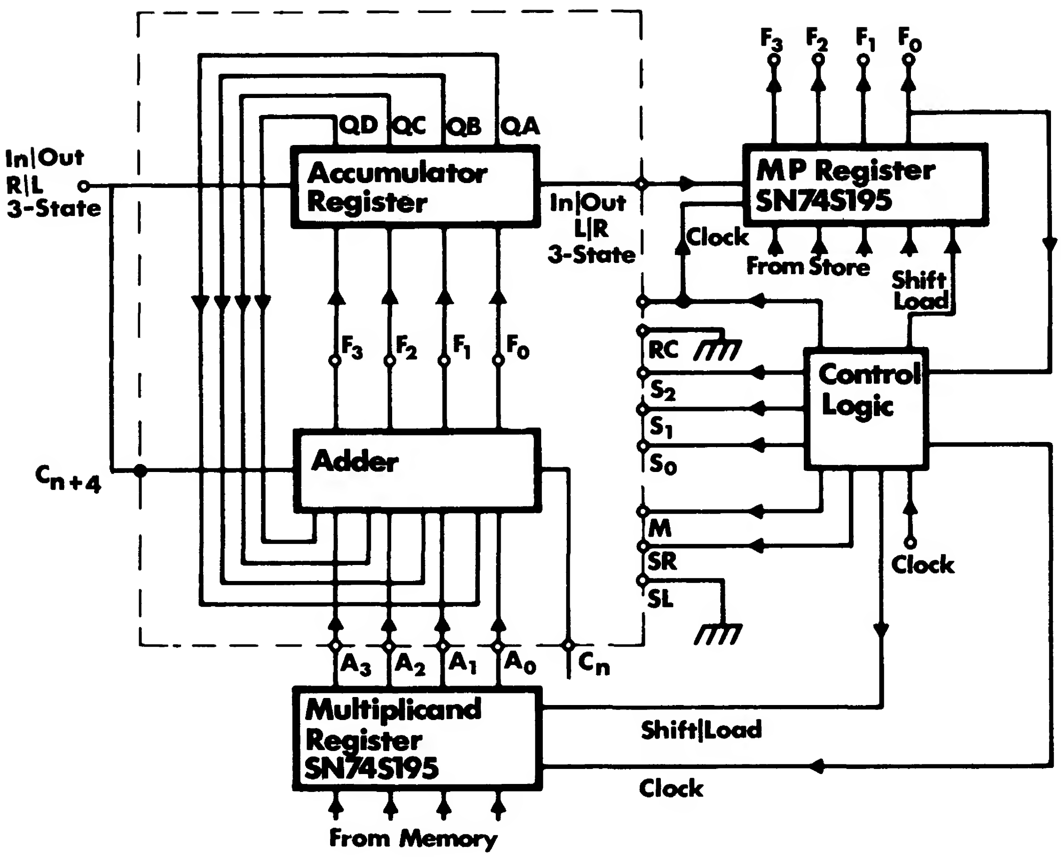

In|Out
R|L
3-State
QD
QC
QB
QA
Accumulator Register
In|Out
L|R
3-State
F3
F2
F1
F0
MP Register SN74S195
Clock
From Store
Shift Load
F3
F2
F1
F0
RC
S2
S1
S0
Control Logic
Cn+4
Adder
M
SR
SL
Clock
A3
A2
A1
A0
Cn
Multiplicand Register SN74S195
Shift|Load
Clock
From Memory

FIGURE 13. Binary Multiplier Block Diagram

Control Logic: The control sequence that must be performed is as follows:

Program Step 1. Set loop counter N=0.
2. Clear accumulator.
3. Load multiplicand register from store.
4. Load m.p. register from store.
5. If l.s.b. m.p. = 1, set control to add.
6. Shift right.
7. $N = N + 1$.
8. If $N \neq 4$, go to step 5.
9. Set a.l.u. to transfer
10. Load store from 'S281 and m.p.

Each of the above instructions involves the setting of various control lines in the correct sequence. A r.o.m. is used to produce the correct control signals (outputs) for each instruction (address input). If the program is simple then the instructions can be stored in the r.o.m. in the order that they are required. This r.o.m. which stores the program, is addressed by a program step counter. Thus as the program counter is incremented the program steps are produced in sequence. At each step all of the control lines (and there may be 12), are switched to the relevant logic levels. The circuit requirement may be more complex than multiplication alone. Other functions such as division, addition, incrementing and complimenting may also be required. It would be possible to write all the requirements into a program r.o.m. but this would be wasteful of storage space as many of the steps would be used several times. A more compact way, and one that makes program changes simpler is to use two r.o.m.s. One r.o.m. would contain the machine's repertoire of possible instructions. As before each address would produce all the control signals relevant to the

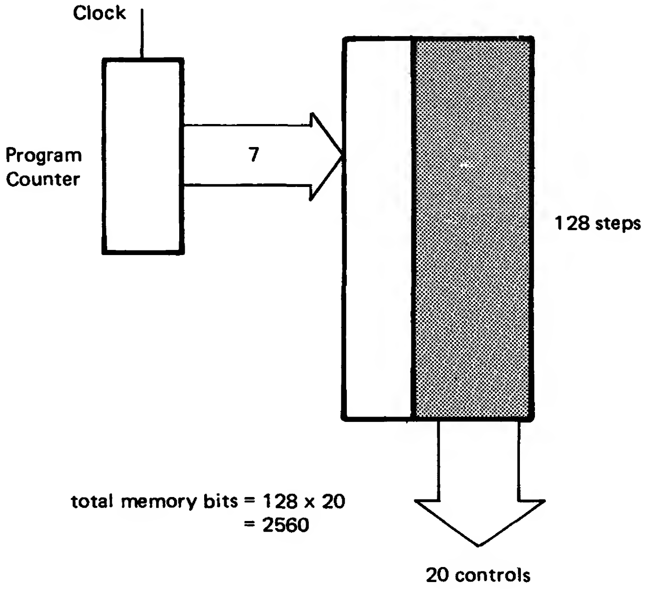

Clock
Program Counter
7
128 steps
total memory bits = 128 x 20
= 2560
20 controls

FIGURE 14. Program Store

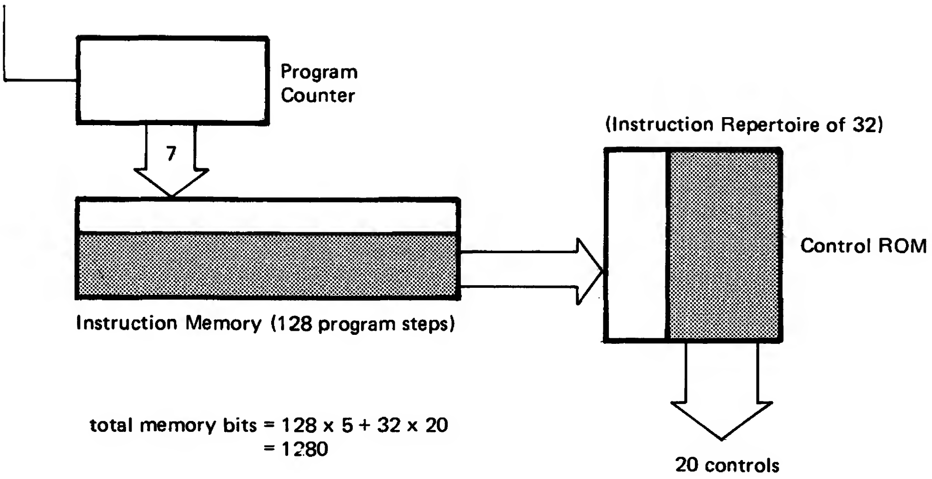

Program Counter
7
(Instruction Repertoire of 32)
Control ROM
Instruction Memory (128 program steps)
total memory bits = 128 x 5 + 32 x 20
= 1280
20 controls

FIGURE 15. Program Store using Instruction Memory and Control ROM

instruction stored at that address. However, each instruction in the repertoire would appear only once in this r.o.m. and the order of the instructions would have no significance. It is then possible to store the addresses of each instruction in the program sequence in the second memory (instruction address memory or more simply instruction memory). The two systems are shown in Figures 14 and 15. There is a saving in total memory size which increases with the length of the program. However, the single r.o.m. approach gives the faster speed.

Binary Divider

Division is similar to multiplication except that the divisor is subtracted from the dividend. Table 5 shows binary division as it would be performed on paper. The divisor is subtracted from the dividend where possible and then shifted to the right. Where subtraction would have caused underflow then it is not performed. With pencil and paper one uses inspection. With logic circuitry it can either be ascertained by inspection (a), or subtraction can be

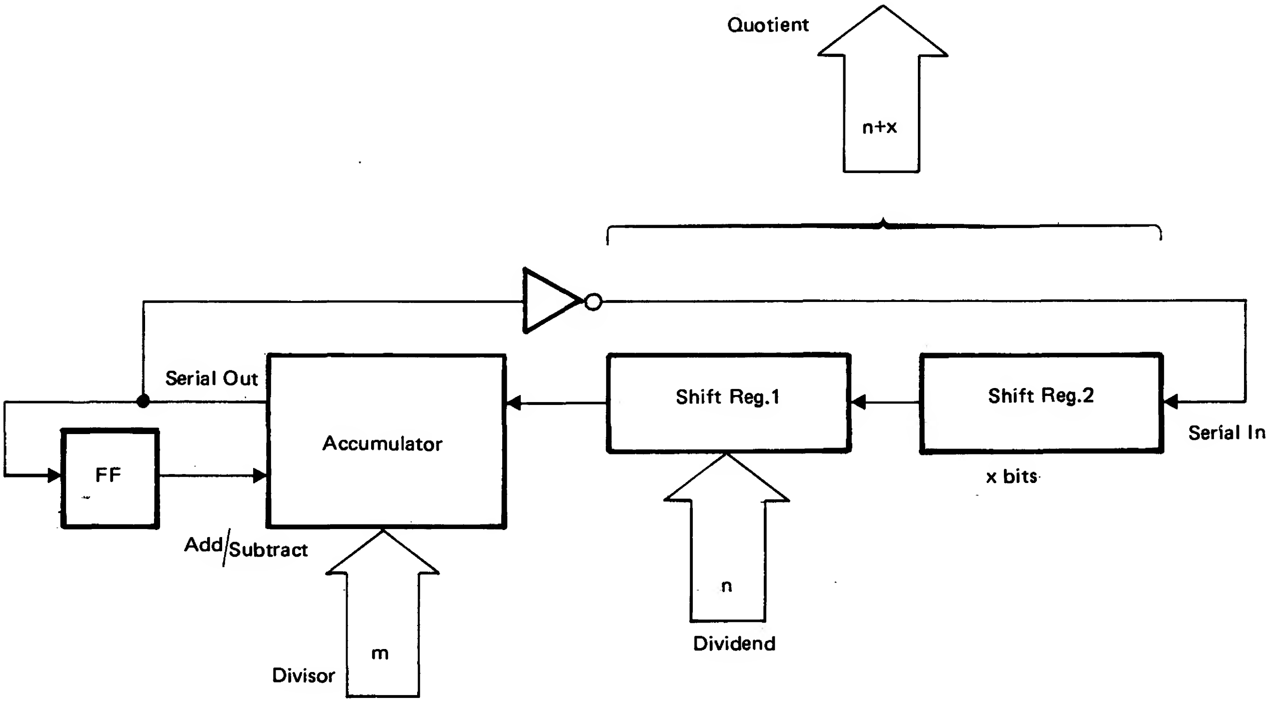

Quotient
n+x
Serial Out
Accumulator
Shift Reg.1
Shift Reg.2
Serial In
x bits
FF
Add/Subtract
n
Dividend
m
Divisor

FIGURE 16. Circuit for Binary Division

Table 5: Example of 'Paper and Pencil' Division

```
                  100011      Quotient
Divisor   1001 )1001111100    Dividend
                1001
                ----
                00001110      Intermediate Remainder
                    1001
                    ----
                    01010
                     1001
                     ----
                     00010    Remainder
```

performed and if underflow occurs then the previous value can be reinstated (b), or it can be 'restored' by adding back the divisor (c). If one examines the hardware requirements for a divider then method (a) needs a comparator, and (b) needs a temporary store. Method (c) requires that the subtractor can also add. If the time required is examined it will be seen that in method (a) the comparison must be performed every time to decide whether to subtract or not, and in method (b) and (c) subtraction is performed every time whether the previous value is reinstated (or restored) or not. So all three methods take one or two operations, an average of 1.5 clock periods.

A time saving can be made by using a non-restoring method. Whenever the intermediate remainder underflows it is not restored as in method (c) but the divisor is shifted one place to the right and it is added. Table 6 shows an example of this technique. The most significant bit of the intermediate remainder decides whether the next operation, after shifting the divisor to the right, is to add or subtract. The inverse of this bit is also the next bit of the quotient. How this can be implemented is shown diagramatically in Figure 16. Initially all registers are cleared. The divisor is presented to the a.l.u. and the dividend loaded into a shift register. The 'S281 accumulators are set in their shift mode and the final serial output wired to control addition or subtraction, '1' for addition, '0' for subtraction. All three registers are clocked in parallel, one bit of the answer being produced for every clock pulse. The system can be clocked until the answer fills shift registers 1 and 2. The maximum length of answer is determined by the length of shift registers 1 and 2. If, for instance, the word length of the answer is required to be the same as the dividend then shift register 2 could be omitted.

Table 6: Example of Non-Restore Algorithm

```
                     100011      Quotient
Divisor   1001 )1001111100       Dividend
                1001
                0|0001
  Subtract       |1001
                 1|0001
   Add            |1001
                  1|0101
    Add            |1001
                   1|1100
     Add            |1001
                    0|1010
      Subtract       |1001
                      00010  Remainder
```

X USE OF PROGRAMMABLE READ ONLY MEMORIES

by
Howard Cook

A versatile device which is suitable for a wide range of functions in electronic systems is the programmable read only memory, p.r.o.m. In the preceeding volume of this book a chapter was devoted to both p.r.o.m.s and mask programmed r.o.m.s, and a range of applications of these devices was discussed, including microprogramming, analogue and digital function generating, random logic applications, and arithmetic operations[1]. To re-state the fundamental difference between a r.o.m. and a p.r.o.m., the latter is a device which may have a program written into it once by the user, after which the device virtually becomes a fixed program r.o.m. The mechanism by which the program is stored is irreversible, and in the majority of devices this takes the form of fusing metal links within the device. This latter operation has proved to be very reliable with the links buried under a thick layer of quartz within the device. When blown, the link metal pulls back from the centre towards each end of the link thus causing a clean break with no possibility of the two halves of the link re-combining. (The only modification which can be made to the stored program once a device has been programmed is by blowing more links which were previously unblown). Thus with this type of p.r.o.m. the design engineer is presented with a very flexible tool, as by programming his own devices he can employ r.o.m. techniques in applications which could not be previously considered using mask-programmed r.o.m.s, due to the high cost and long waiting periods associated with having these devices manufactured. In this chapter the device is used in the system timing generation, information checking, and high speed character generation areas.

SYSTEM TIMING GENERATION

Introduction

Some requirements for system timing are difficult to implement by usual logic techniques. This may be due to the range of time periods which have to be defined within a timing cycle. The system shown in Figure 1 shows a method for producing such a sequence using a p.r.o.m. In this case the p.r.o.m. is an SN74186 which is organised as

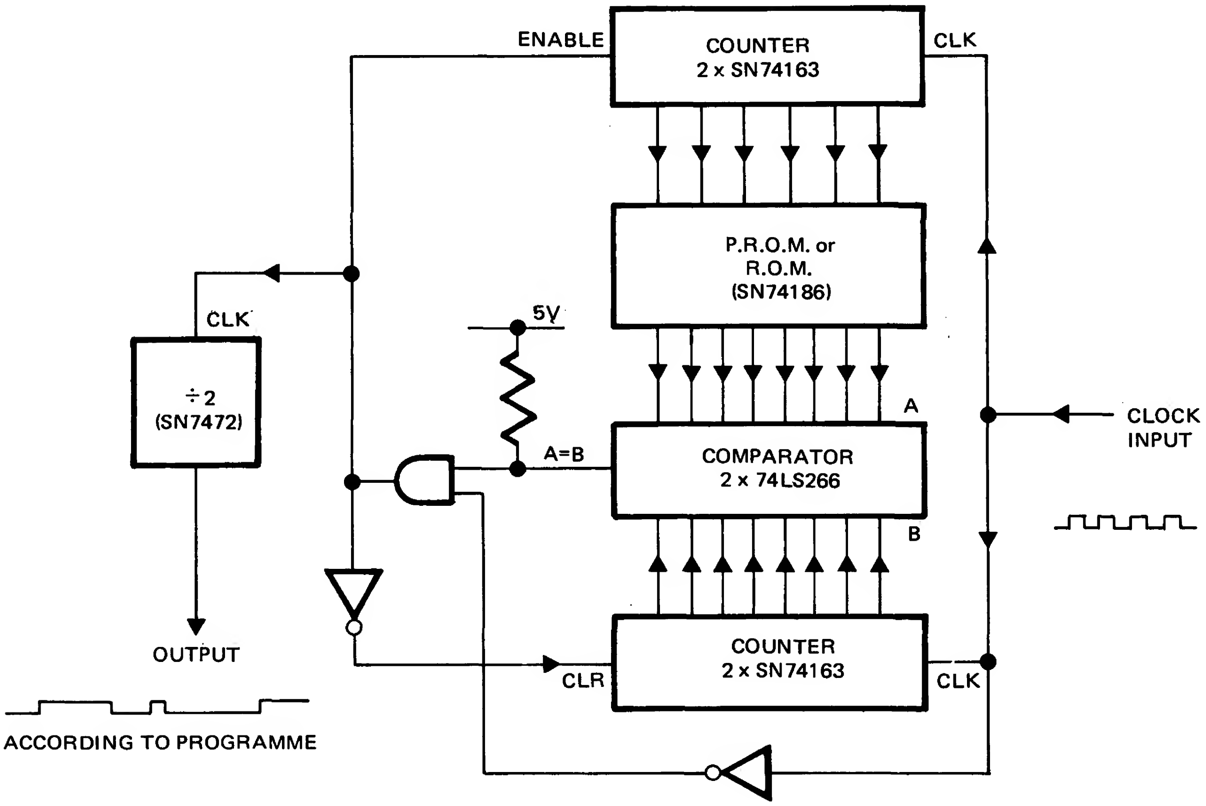


FIGURE 1. Programmable Sequence Timer.

64 words x 8 bits, and hence has six select inputs and eight data outputs. The select inputs are supplied by the outputs of the upper pair of SN74163 synchronous counters. The most significant two outputs from these counters are disregarded. The outputs from the p.r.o.m. are compared with the outputs of the lower pair of SN74163 counters by the two SN74LS266 devices. These devices are quad 2-input exclusive NOR devices with open collector outputs. Figure 2 shows how these devices can be used as an 8-bit word comparator, with the outputs connected together in wire-AND fashion with a pull-up resistor to form the 'equality' output.

Operation

The clock input to the system is supplied to both sets of counters, and is then inverted and used to gate the 'A=B' output from the comparator. Assuming that the counters receive a reset pulse from another part of the system when the power is turned on, all the counters will start from zero. The 'all zeros' input to the p.r.o.m. is a valid address, and a corresponding output from the p.r.o.m. is supplied to the data comparator. However, the input to the comparator from the lower counter is still all zeros, and hence not equal to the p.r.o.m. output. The A=B output from the comparator thus remains at logic '0' and this inhibits the 'enable' input to the upper counters. As clock pulses are supplied to the system, the positive going clock edges try to increment the counters. However, only the bottom counters actually increment since the upper counters are disabled. This continues until the output of the lower counters changes to the same word as the output from the p.r.o.m. .This causes the A=B line to change to a logic '1', which is allowed through the AND gate when the clock returns to a '0'. (Since $\overline{\text{clock}}$ is supplied to this gate, this protects the system against spurious output spikes on the A=B line due to propagation delay variations in the counter outputs changing.) When the A=B line changes to a '1' the lower counters are cleared to zero, and the upper counters are enabled ready for the next clock pulse. The A=B signal also clocks the divide-by-two stage which provides the system output. This stage allows the duration of both the high and low states of the system output to be programmed. The next clock pulse increments all the counters, which causes the data words supplied to the comparator to change, thus causing the A=B line to return to '0', which disables the upper counters. The new output from these counter forms a new address to the p.r.o.m. which in turn supplies a new output word to the comparator. Thus the process continues.

This system can be programmed to store 64 intervals and each one can be any length from one clock period to 2^8 clock periods. (An example of such a requirement would be the timing of an automatic washing machine where the steps in the 'rinse-wash-spin' procedures vary in length from perhaps 3 seconds to 10 minutes. With the clock period set to 3 seconds, the longest interval which could be achieved by the circuit is 12.8 minutes, which is greater than 10 minutes and thus adequate.)

INFORMATION CHECKING

Hamming Code

One method of protecting the integrity of digital information whilst it passes through a circuit 'network' is to use a Hamming code. In 1950 R.W. Hamming produced a paper[2] describing how such a system could be implemented, and with the low cost per function in modern electronics, the increased complexity involved in using such a system now may have little effect on the total system cost. The circuit 'network' mentioned above may be a transmission line from one piece of apparatus to another for example, or

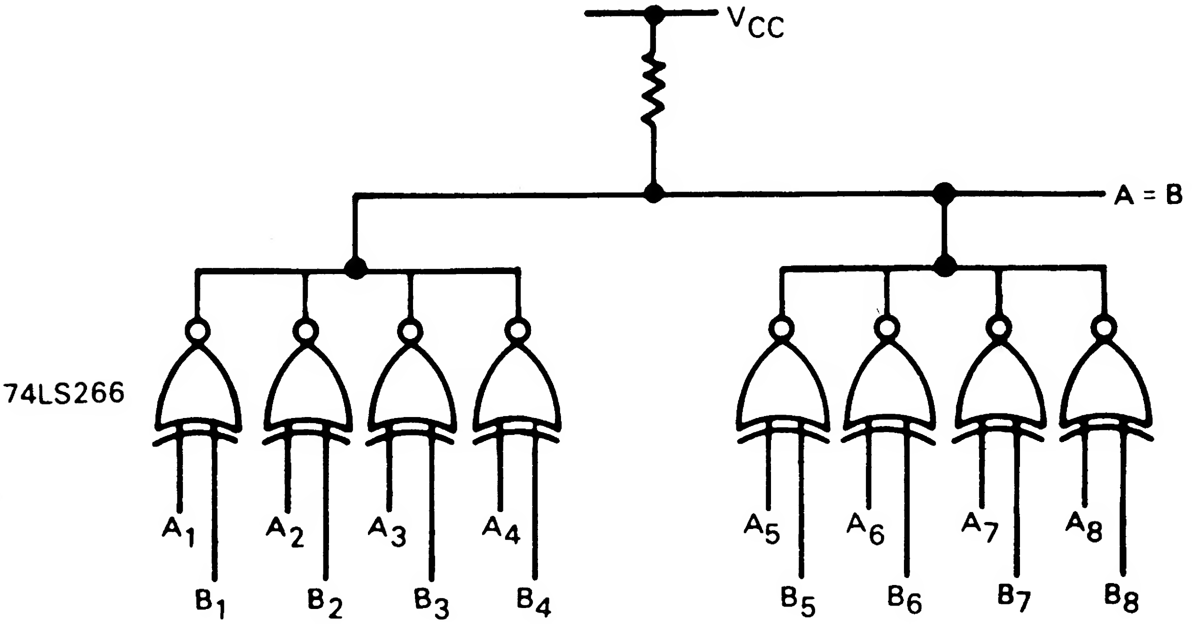


FIGURE 2. Connection of Exclusive NOR Gates as 8 Bit Word Comparator

perhaps a memory system. In any case the Hamming code allows errors which have been introduced into the data by the network to be located and corrected; the number of errors which can be corrected being a function of the added complexity necessary for the Hamming code. The codes described by Hamming in the above paper are Systematic codes. These may be defined as codes which each code symbol has exactly 'n' binary digits, where 'm' digits are associated with the information while the other k = n-m digits are used for error detection and correction. This produces a redundancy, R, defined as

R = total number of digits/information digits

which effectively reduces the channel efficiency. The k check bits are generated as parity bits on selected parts of the data word. It can be shown that to be capable of correcting a single error in the data word, the relationship of m to n is $2^m \leqslant 2^n/(n+1)$. This shows that 4 check bits are sufficient for information word lengths (m) up to 11 bits. Thus the redundancy varies according to the value of m. In order to be able to detect (without correcting) a further error an additional check bit is required. P.r.o.m.s can be used to carry out the generation of the check bits for a data word made up of 4 information bits, and also the checking and correcting of the combined word.

Check Bit Generation

Table 1 shows the defining equations for generating the check bits, P, from the data bits, X, and Figure 3 a method of implementing this for P1 using exclusive OR gates. Table 2 shows the logic truth table for 4 data bits and 4 check bits (single error correcting, and double error detecting) generated from the equations in Table 1. An economical alternative for generating the check bits is to use a 256 word x 4 bit p.r.o.m., an SN74S287, as shown in Figure 4. The 4 check bits are in fact sufficient for up to 11 information bits if only single error correction without double error detection is required. Hence this p.r.o.m. can generate the check bits for up to 8 information bits, since it has 8 select (address) inputs. If it is used for information word lengths of less than 8 bits, then the unused select inputs must be held permanently to one level or the other. The p.r.o.m. is programmed according to the appropriate truth table, such as that in Table 2.

Table 1

$$P_1 \oplus X_1 \oplus X_2 \oplus X_4 = 0$$

$$P_2 \oplus X_1 \oplus X_3 \oplus X_4 = 0$$

$$P_3 \oplus X_2 \oplus X_3 \oplus X_4 = 0$$

$$P_1 \oplus X_1 \oplus P_2 \oplus X_2 \oplus P_3 \oplus X_3 \oplus P_4 \oplus X_4 = 0$$

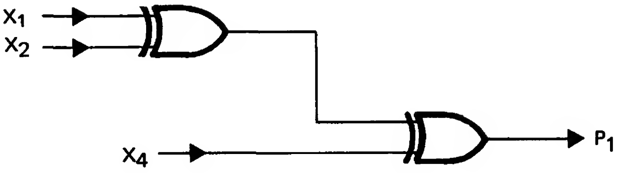


FIGURE 3. Hamming Code Generation.

Table 2

Decimal Number	P_1	X_1	P_2	X_2	P_3	X_3	P_4	X_4
0	0	0	0	0	0	0	0	0
1	1	0	1	0	1	0	0	1
2	0	0	1	0	1	1	1	0
3	1	0	0	0	0	1	1	1
4	1	0	0	1	1	0	1	0
5	0	0	1	1	0	0	1	1
6	1	0	1	1	0	1	0	0
7	0	0	0	1	1	1	0	1
8	1	1	1	0	0	0	1	0
9	0	1	0	0	1	0	1	1
10	1	1	0	0	1	1	0	0
11	0	1	1	0	0	1	0	1
12	0	1	1	1	1	0	0	0
13	1	1	0	1	0	0	0	1
14	0	1	0	1	0	1	1	0
15	1	1	1	1	1	1	1	1

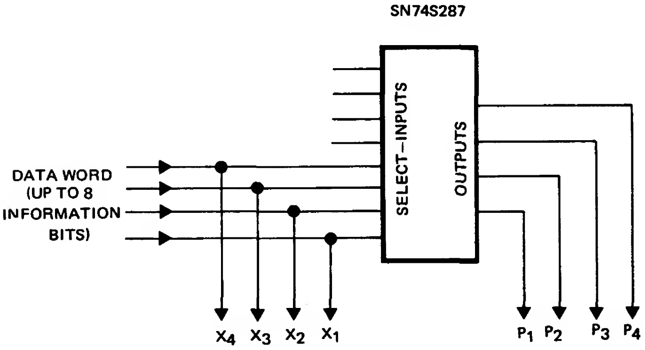


FIGURE 4. Hamming Code Check Bit Generation.

Error Checking and Correcting

The method of checking a data word for errors, locating, and correcting the error, is to perform parity checks on the various groups of bits, as defined by the equations in Table 1. A numerical example of this is as follows:

Consider the code representing decimal 12.

Decimal Number	P1	P2	X1	P3	X2	X3	X4	P4
12	0	1	1	1	1 (0)	0	0	0

If the '1' in position X2 is corrupted to a '0' then:
The equation for P1 predicts a '1' and actually present is a '0'. Therefore write . . . 1
The equation for P2 predicts a '1' and actually present is a '1'. Therefore write a '0' to the left of the previous '1', giving . . . 01 01
The equation for P3 predicts a '0' and actually present is a '1'. Therefore write a '1' giving . . . 101 101

This binary number represents 5, indicating that the fifth bit is the error. P4 is used to indicate the presence of two errors. The equation for P4 predicts a '0' and actually present is a '0'. Hence there are not two errors. This procedure can also be performed economically using p.r.o.m.s.

Figure 5 illustrates a system for processing an 8 bit data word made up of 4 information bits and 4 check bits. All 8 bits are supplied to the select inputs of integrated circuits which once again is an SN74S287 256 x 4 p.r.o.m. This device is programmed according to the procedure outlined above for single error correcting, and its four outputs thus give true information for zero or one error at the input. Integrated circuits IC2 and IC3 form a block of memory organised as 256 words of 1 bit; IC2 is an SN74188 p.r.o.m. which is 32 words x 8 bits (256 bits total) and IC3 is a 1 line from 8 line data selector. The latter, controlled by three of the input lines, selects one output from the SN74188 at a time. The select inputs of the SN74188 are connected to the other 5 inputs, and the device is programmed according to the equation defining the last check bit P4. Thus if the input word of 8 bits contains two errors, the output of IC3 indicates that the output word from IC1 is incorrect.

HIGH SPEED CHARACTER GENERATORS

Introduction

In systems involving the display or printing of alpha-numeric characters it is usually necessary to convert from a digital code to the character format at some stage. This step is defined by economics, since a character formed by a 5 x 7 dot matrix display involves defining 35 dots, but 64 characters, for example, could be defined by only six bits in a binary word. (Since $2^6 = 64$). Thus the electronics of the system need only be capable of handling 6 bit words in this instance. Although standard 'character generator' integrated circuits are available for the conversion from digital code to dot matrix format, they are not suitable for certain applications. A typical standard device is the TMS 2501 which is a p-channel MOS device programmed with 64 standard characters[3]. (A to Z, 0 to 9, punctuation, etc.). Due to the technology used for the manufacture of devices

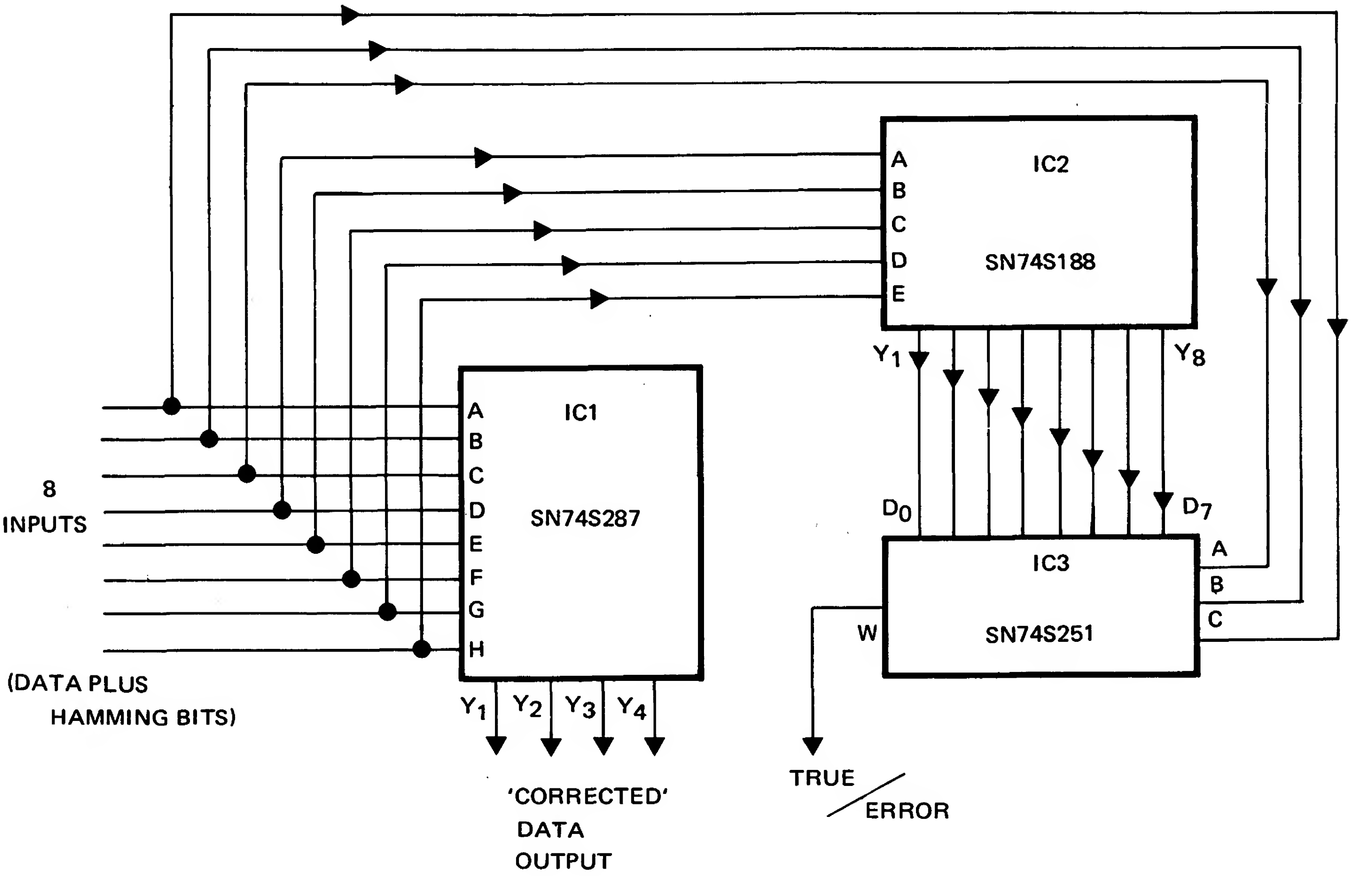


FIGURE 5. 4 + 4 Bit Hamming Code Error Detector and Corrector.

such as this, the speed of operation is very limited (approximately 1.5MHz maximum character row rate). This limitation plus the fact that the program in the device is fixed to a standard set of characters, does impose restrictions on the usefulness of the device. A method to overcome both of these restrictions is to construct the character generator using t.t.l. p.r.o.m.s. Again this allows the user to define and enter his own program of characters, and also the circuit is capable of much higher speed of operation. The system shown in Figure 6 stores 128 characters for display on a 5 x 7 dot matrix, and has an access time from address input to character row output of typically 50ns.

Operation

The p.r.o.m. components used in this system are SN74S287 1024 bit devices organised as 256 words of 4 bits. In order to store 128 characters for 5 x 7 matrix display, the total memory capacity must be at least 128 x 5 x 7 = 4480 bits, organised as 896 words of 5 bits. The first four p.r.o.m.s, integrated circuits IC1, 2, 3 and 4, have their corresponding outputs connected together in Wire-AND fashion, and the devices are selected one at a time via their 'enable' inputs. These inputs are driven from the outputs of one half of an SN74S139, IC6, which is a 2-line to 4-line decoder, and its two inputs are two of the ten address inputs to the system. The remaining 8 address inputs are connected to each of the five p.r.o.m.s in the system. Integrated circuits IC1 to 4 thus form a memory block of 1024 words of 4 bits, and it then remains to provide 1024 words of 1 bit to complete the system. This is supplied by the fifth device, IC5, whose four outputs are selected one at a time by one half of an SN74S153 data selector, IC7. The data selector inputs are controlled by the same two address lines that controlled the decoder device of the 1024 x 4 memory block. IC5 with IC7 then forms a memory block of 1024 words of 1 bit, giving a total organisation of 1024 words of 5 bits.

Operating Speed: The typical propagation delay through the SN74S139 is 7ns, and the typical access time of the p.r.o.m.s from their enable inputs is 15ns. This total delay, 22ns is less than the typical access time of the p.r.o.m.s from the address inputs, which is 45ns. The access time of the 1024 x 1 block is determined by the access time of the p.r.o.m. from its address inputs, i.e. 45ns, plus the propagation delay through the SN74S153, i.e. 6ns, giving a total of 51ns. Since this is the longer of the two total access times in the system, it determines the systems maximum operating speed.

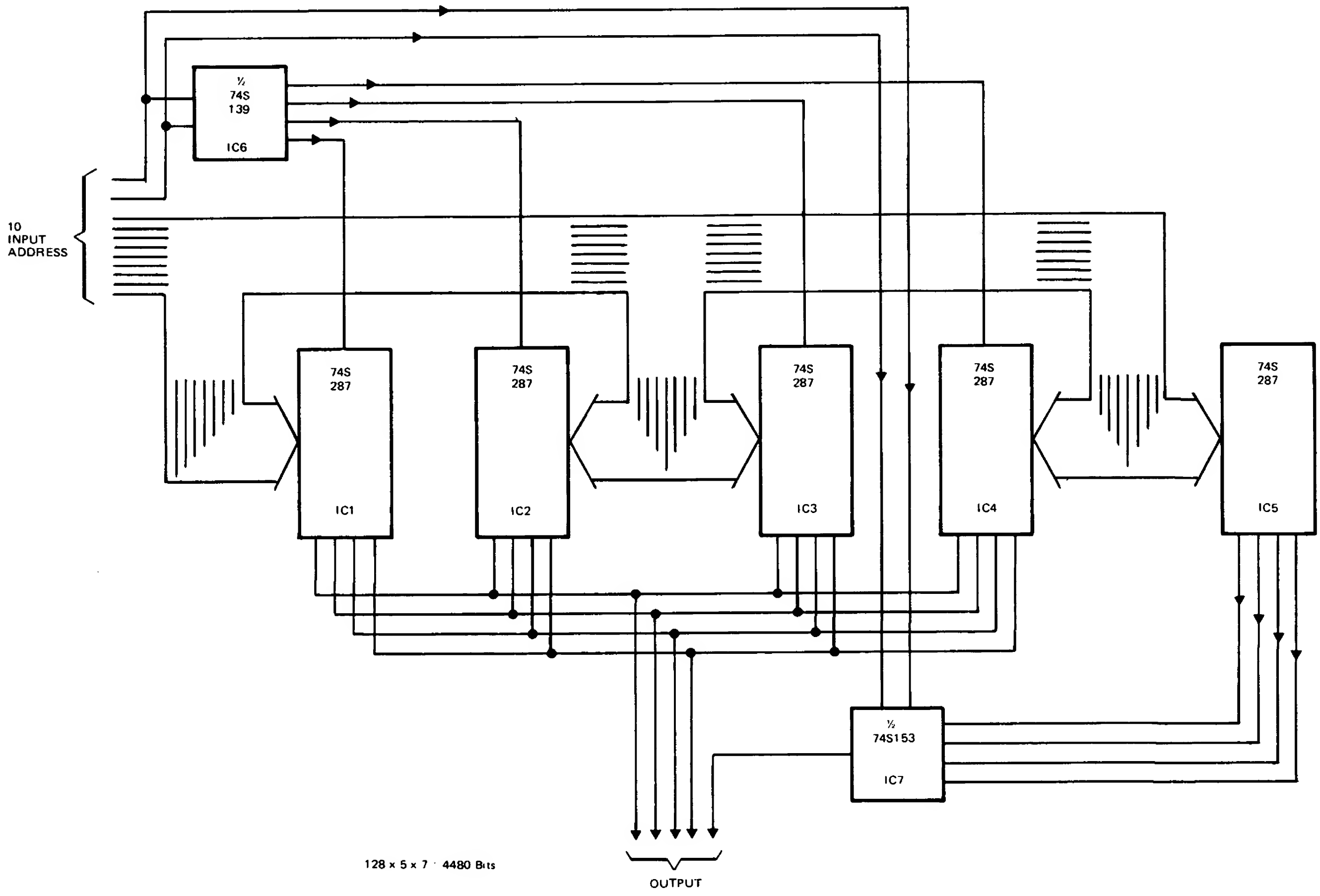


FIGURE 6. High Speed 128 Character Generator.

Other Simple Solutions

For applications requiring fewer characters a single device may be used. The SN74S471 is a 2k bit p.r.o.m. organised as 256 words and 8 bits. This device can thus be used for various different organisations of character generator. For a 5 x 7 character matrix 5 of the outputs can be used for row output applications, or 7 outputs used in column output applications. In these examples of the device can be programmed to store 36 and 51 characters respectively. Also, the device is suitable as a row output device for use with a 7 x 9 display matrix, by using 7 of its outputs. In this case the device can store 28 characters.

In such applications as this, the p.r.o.m. is an invaluable device. It enables a few extra characters to be available when used in conjunction with a standard character generator device, or alternativly the number of characters stored (up to 51) may be sufficient for the total requirement of a simple system. These devices can, of course, be cascaded to increase the number of stored words. Figure 7 shows two devices cascaded to form 512 words x 8 bits, which can be programmed to store 73, 102 or 56 characters in the organisations previously described. The ninth input address line enables one device at a time, thus allowing the 8 outputs from the two devices to be connected to a common 8 output lines from the system. When one device is disabled, its outputs are high impedance due to their three state circuitry, and thus do not affect the data outputs from the device which is selected.

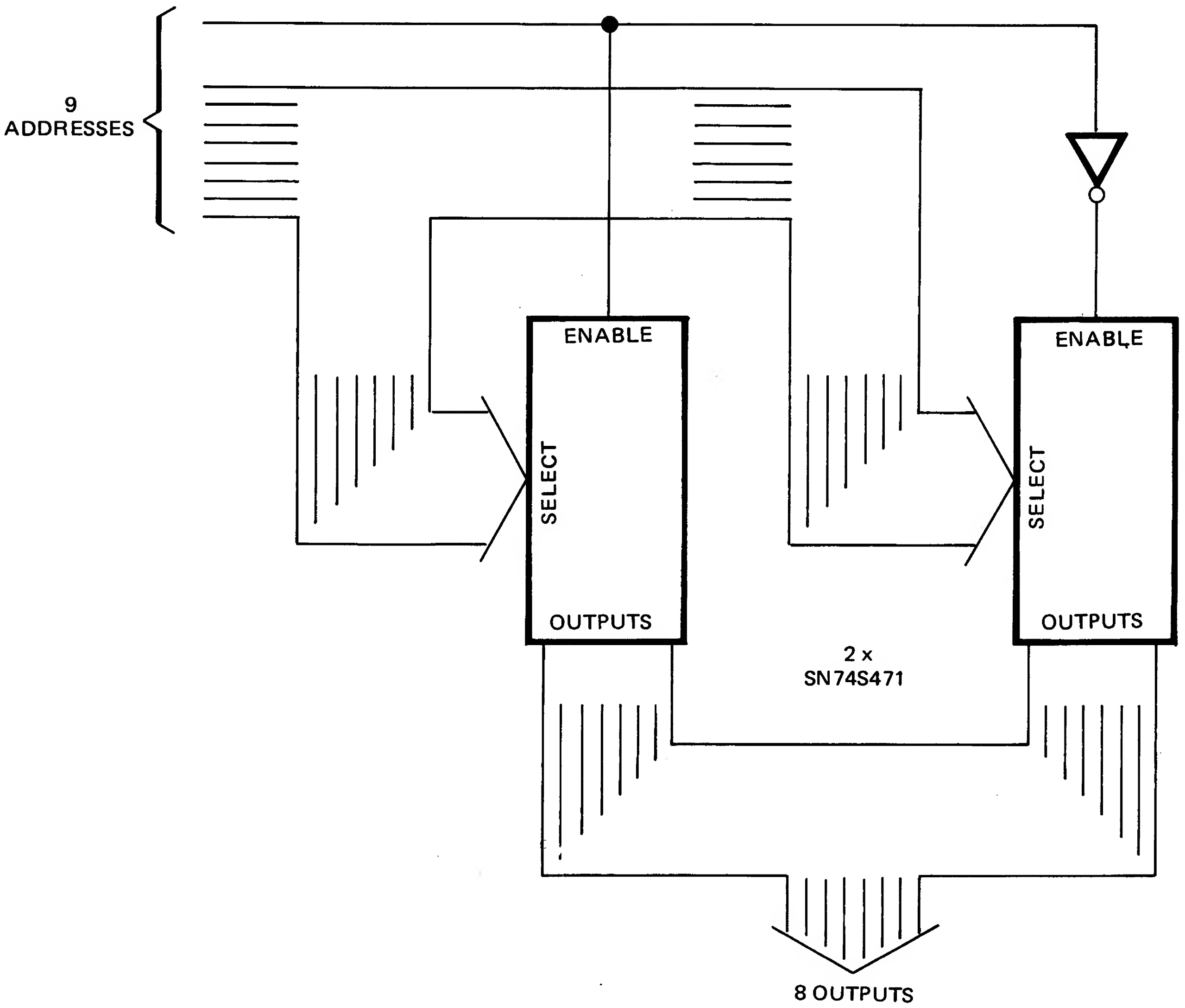


FIGURE 7. Cascading.

REFERENCES

1. *Semiconductor Circuit Design Vol III,* Texas Instruments Limited, Chapter VII, April 1974.

2. R. W. Hamming, 'Error Detecting and Error Correcting Codes,' *The Bell System Technical Journal,* April 1950.

3. *Semiconductor Circuit Design Vol III,* Texas Instruments Limited, p.p. 18-26, April 1974.

XI REFERENCE MARK LOCATOR FOR AUTOMATED EQUIPMENT

Although the ultimate aim is to operate a power control unit, the inclusion of this chapter is more appropriate here, rather than in the power control section, as the system employs digital processing techniques including a memory. The full automation of many computer controlled processes is dependent on the ability of the system to positionally align each step of the process to previous steps. This is particularly true of the photographic processes used in semiconductor or printed-circuit board manufacture but can also be relevant in mechanical fabrication techniques such as the cutting and/or drilling of sheet materials. If all the steps in a process can be achieved without removal of the material on which the work is being performed, then alignment need only be limited by the mechanical accuracy of the machine components. Where the material has to be handled between process stages, a mechanical 'banking' system using the edges of the target as a reference will commonly achieve alignment accuracies of a few tens of microns. In cases where the above two techniques are either impractical or insufficiently accurate, a useful method is to place one or more reference marks on the material and use an electronic or electro-mechanical system to measure their exact position. A vidicon tube system with a marker either very bright or very dark compared with the surrounding material forms a simple accurate system but various other methods, based on light reflection or transmission, or capactive or magnetic sensing, may be devised for specific applications. A highly successful implementation of this technique, capable of sub micron accuracy, has been achieved using an electron beam scanned across a narrow trough etched in silicon or metal with a secondary electron detector to measure the 'brightness' of the trough edges. It is from work carried out in this field that the circuitry which will be described has been taken.

OPERATION

For a single axis alignment the simplest marker shape is that of a narrow line. In the more common case of two-dimensional alignment on 'L' shape is desirable with separate alignment of each 'arm' of the marker. In this case an improvement in accuracy may be achieved by aligning in each axis twice, such that the position of the second alignment in each axis will take place at a precise position on the marker 'arm' defined by the first alignment in the other axis.

Returning to the case of a single axis alignment, from which the two-dimensional method may be simply evolved, there are only two variables involved, 'relative position' and 'video signal'. The 'relative position' may be a measure of the mechanical movement applied to the target to vibrate it under the sensor, or, as in the vidicon or electron beam techniques an electronic signal indicating where the sensor is 'looking' at a particular instant. The 'video signal' is the sensor output which signifies by a peak or trough the presence of the marker.

Whatever technique is used, the variation of video signal with position will ideally be that shown in Figure 1. If the signal is as 'clean' as indicated in Figure 1 then the problem of alignment may be relatively easily solved by applying a relatively slow movement to the target and sensing when the marker peak is central. In practice a reliable alignment system has to cope with many practical problems such as dust, electrical noise and sensor degradation and to succeed with minimum operator intervention must possess enough 'intelligence' to withstand far from ideal circumstances.

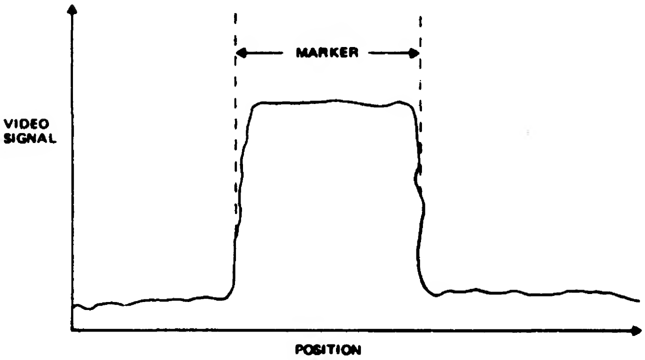


FIGURE 1. Ideal Video Waveform

CIRCUITS

General

The obvious source of this 'intelligence' in a computer controlled system is the computer itself but this requires conversion of the data to digital format. The video signal may be converted by means of a comparator but a problem often arises in selecting the comparison voltage so that variations in sensor sensitivity can be accommodated. A simple way of overcoming this is illustrated in Figure 2.

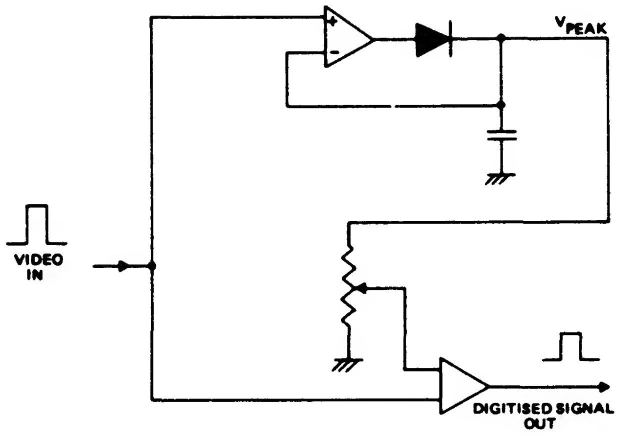


FIGURE 2. Video Digitizing Circuit with Automatic Trigger Level

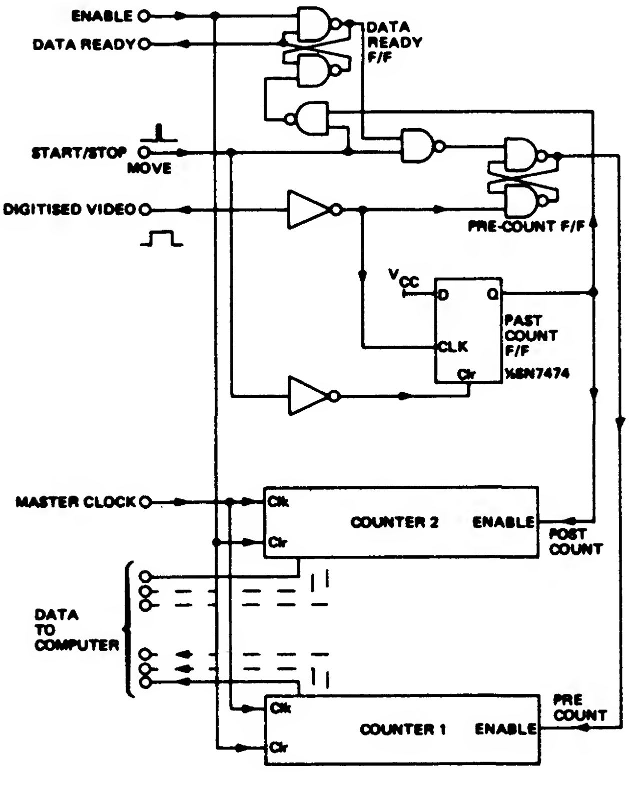


FIGURE 3. Basic Timing System

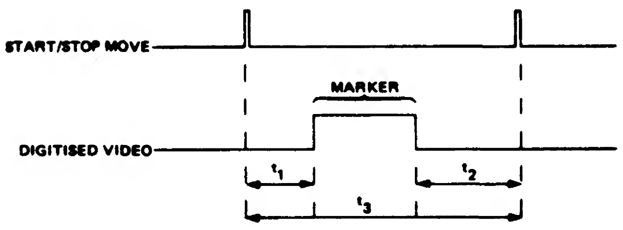


FIGURE 4. Basic Timing

Here on amplifier measures the peak signal voltage[1] and a fraction of this, either manually set by a potential divider or computer controlled via a multiplying digital-to-analogue converter, is used as the comparator reference. Conversion of the positional information is often easiest achieved by a timing system such as that shown in Figure 3. Here the only positional information is a pulse indicating the start or end of a move. In a vibrating system this simple pulse indicates a change of direction.

In Figure 3 an ENABLE pulse from the computer resets the DATA READY flip-flop and clears the two counters. On the next START MOVE pulse the PRE-COUNT flip-flop is set and counter 1 counts from the master clock. The leading edge of the digitised Video clears the PRE-COUNT flip-flop and stops counter 1. On the trailing edge the POST-COUNT flip-flop is set and counter 2 starts. This counts until the next START MOVE pulse, at which point the DATA READY flip-flop is set. The computer may then input the times t_1 and t_2 shown in Figure 4. By performing a scan with the marker input disabled the total time t_3 may also be derived. Given this information, preferably repeated for several scans, the computer is able to determine how well the marker is centred in the alignment window. If the extent of the movement is roughly known and relatively linear, the computers can estimate the width of the marker seen which assists in the rejection of absurd data.

Complete System

A complete marker measurement system incorporating a t.t.l. buffer memory[2] is shown in Figure 5. In this system a single synchronous 'up' counter, comprising four SN74LS161 integrated circuits, is used to measure the times in Figure 4 which are then loaded into the t.t.l. r.a.m. for interrogation by the computer at a convenient time. The system is set up to accept data from 9 scans back and forth across the marker limb. The first 2 scans are made with the DIGITISED VIDEO disabled via gate G11 and serve to measure the total scan time (t_3) in the forward (t_{3f}) and reverse (t_{3r}) directions which will generally not be exactly equal. During this time the video comparison reference is also set up by the circuit in Figure 2. The remaining 7 scans are made with the DIGITISED VIDEO enabled and result in the measurement of seven times equivalent to t_1 and seven times equivalent to t_2. Thus buffer storage is required for 16 x 16 bit words which is conveniently provided by four SN7489 t.t.l. r.a.m.s.

Measurement of times for each scan is controlled by the COUNT SEQUENCER which comprises an SN74LS161 counter (N11) an SN74LS155 dual 1 to 4 line demultiplexer (N10) and associated control gates. The operating sequence for the system is listed in Table 1, and the representation of the alphabetical symbols used in this table are given in Table 2.

When the 9 scans have been completed the computer can input the data stored in the r.a.m. at any convenient time by applying strobe pulses to the READ DATA line to decrement the memory address counter. Since the write/enable line to the r.a.m. is at a logical '1', the required data appears at the r.a.m. output.

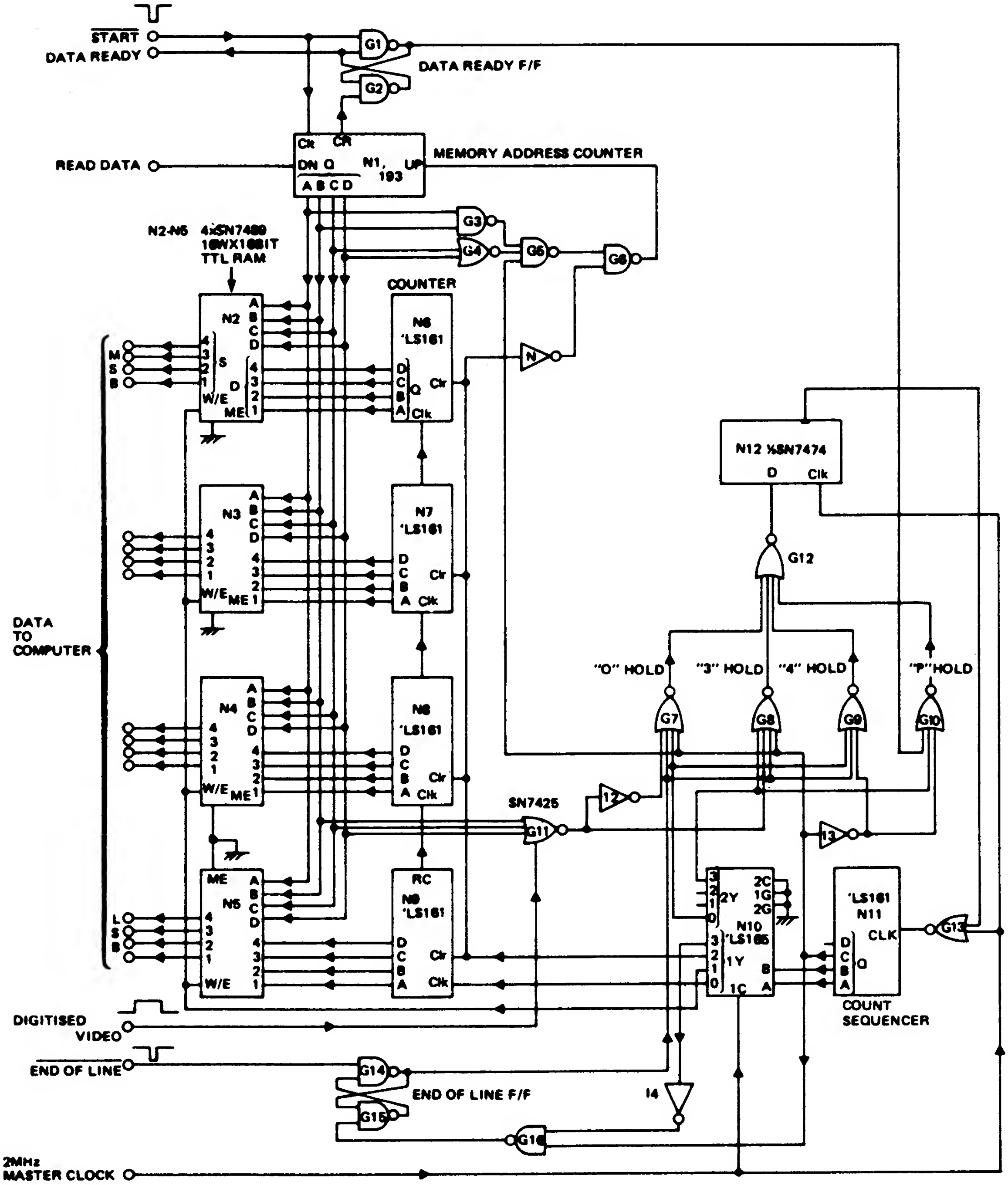
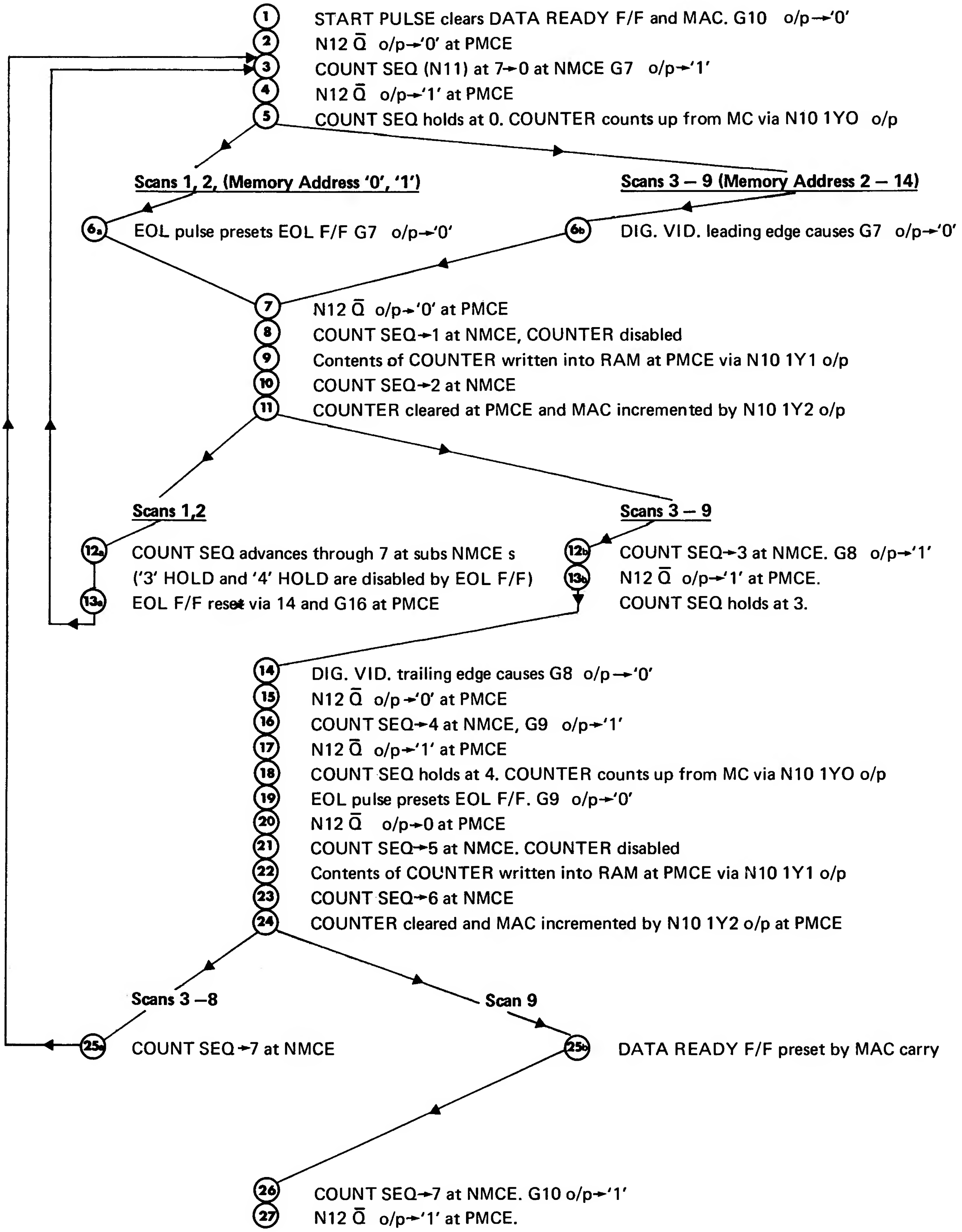

START
DATA READY
G1
G2
DATA READY F/F
READ DATA
Clk
CR
DN Q
N1, 193
UP
A B C D
MEMORY ADDRESS COUNTER
G3
G4
G5
G6
N2-N5 4xSN7489 16WX16BIT TTL RAM
COUNTER
N2
N3
N4
N5
N6 'LS161
N7 'LS161
N8 'LS161
RC N9 'LS161
W/E
ME
Clr
N
M S B
L S B
DATA TO COMPUTER
N12 ½SN7474
D Clk
G12
"0" HOLD
"3" HOLD
"4" HOLD
"P" HOLD
G7
G8
G9
G10
SN7425
G11
12
13
N10 'LS165
2Y
1Y
2C
1G
2G
1C
'LS161 N11
CLK
COUNT SEQUENCER
G13
DIGITISED VIDEO
END OF LINE
G14
G15
END OF LINE F/F
14
G16
2MHz MASTER CLOCK

FIGURE 5. Complete System with T.T.L. Buffer Memory

Table 1. Operating Sequence



① START PULSE clears DATA READY F/F and MAC. G10 o/p→'0'
② N12 $\bar{Q}$ o/p→'0' at PMCE
③ COUNT SEQ (N11) at 7→0 at NMCE G7 o/p→'1'
④ N12 $\bar{Q}$ o/p→'1' at PMCE
⑤ COUNT SEQ holds at 0. COUNTER counts up from MC via N10 1YO o/p

Scans 1, 2, (Memory Address '0', '1')

(6a) EOL pulse presets EOL F/F G7 o/p→'0'

Scans 3 – 9 (Memory Address 2 – 14)

(6b) DIG. VID. leading edge causes G7 o/p→'0'

⑦ N12 $\bar{Q}$ o/p→'0' at PMCE
⑧ COUNT SEQ→1 at NMCE, COUNTER disabled
⑨ Contents of COUNTER written into RAM at PMCE via N10 1Y1 o/p
⑩ COUNT SEQ→2 at NMCE
⑪ COUNTER cleared at PMCE and MAC incremented by N10 1Y2 o/p

Scans 1,2

(12a) COUNT SEQ advances through 7 at subs NMCE s ('3' HOLD and '4' HOLD are disabled by EOL F/F)
(13a) EOL F/F reset via 14 and G16 at PMCE

Scans 3 – 9

(12b) COUNT SEQ→3 at NMCE. G8 o/p→'1'
(13b) N12 $\bar{Q}$ o/p→'1' at PMCE.
COUNT SEQ holds at 3.

⑭ DIG. VID. trailing edge causes G8 o/p→'0'
⑮ N12 $\bar{Q}$ o/p→'0' at PMCE
⑯ COUNT SEQ→4 at NMCE, G9 o/p→'1'
⑰ N12 $\bar{Q}$ o/p→'1' at PMCE
⑱ COUNT SEQ holds at 4. COUNTER counts up from MC via N10 1YO o/p
⑲ EOL pulse presets EOL F/F. G9 o/p→'0'
⑳ N12 $\bar{Q}$ o/p→0 at PMCE
㉑ COUNT SEQ→5 at NMCE. COUNTER disabled
㉒ Contents of COUNTER written into RAM at PMCE via N10 1Y1 o/p
㉓ COUNT SEQ→6 at NMCE
㉔ COUNTER cleared and MAC incremented by N10 1Y2 o/p at PMCE

Scans 3 –8

(25a) COUNT SEQ→7 at NMCE

Scan 9

(25b) DATA READY F/F preset by MAC carry

㉖ COUNT SEQ→7 at NMCE. G10 o/p→'1'
㉗ N12 $\bar{Q}$ o/p→'1' at PMCE.

Table 2. Alphabetical Symbol Listing

COUNT SEQ = COUNT SEQUENCER
DIG VID = DIGITISED VIDEO
EOL = END OF LINE
F/F = Flip/flop (bistable multi-vibrator)
G10 etc. = Gate number 10 etc.
I2 = Inverter 2 etc.
MAC = Memory Address Counter
MC = MASTER CLOCK
N10 etc. = Integrated Circuit Network number 10 etc.
NMCE = next negative MASTER CLOCK edge
O/P = output
PMCE = next positive MASTER CLOCK edge
RAM = RANDOM ACCESS MEMORY
Subs = subsequent
→= goes to

REFERENCES

1. *'Semiconductor Circuit Design',* Vol. II, Texas Instruments Ltd., pp 148-149, April 1973.

2. *'Semiconductor Circuit Design',* Vol III, Texas Instruments Ltd., pp 31-48, April 1974.

XII A UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER

by
Paul R. Grünenfelder
Professor of Electrical Engineering
Brugg-Windisch Polytechnic, Switzerland

An important part of any data processing system is, obviously, the transmission and reception of information between the various functional blocks of the system, e.g. card or tape reader to control unit and vice versa, control unit to modem, etc. The TMS6011 is a universal asynchronous receiver transmitter (u.a.r.t.) m.o.s./l.s.i. subs system designed to provide the data interface between a serial communication link and data processing equipment, For transmission, the parallel data is converted to serial, and for reception serial data from a line is accepted and translated to parallel. This device was introduced in the previous volume[1] and a description is given there of its three sections, i.e. transmitter, receiver and control. However for completeness, an expanded version of this description has been included in the operation part of this chapter. Figure 1 shows a functional block diagram of the device. The serial word will have start, data and stop bits. Parity may be generated and verified. The receiver section will validate the received data transmission by checking the correct parity, start and stop bits and convert the data to

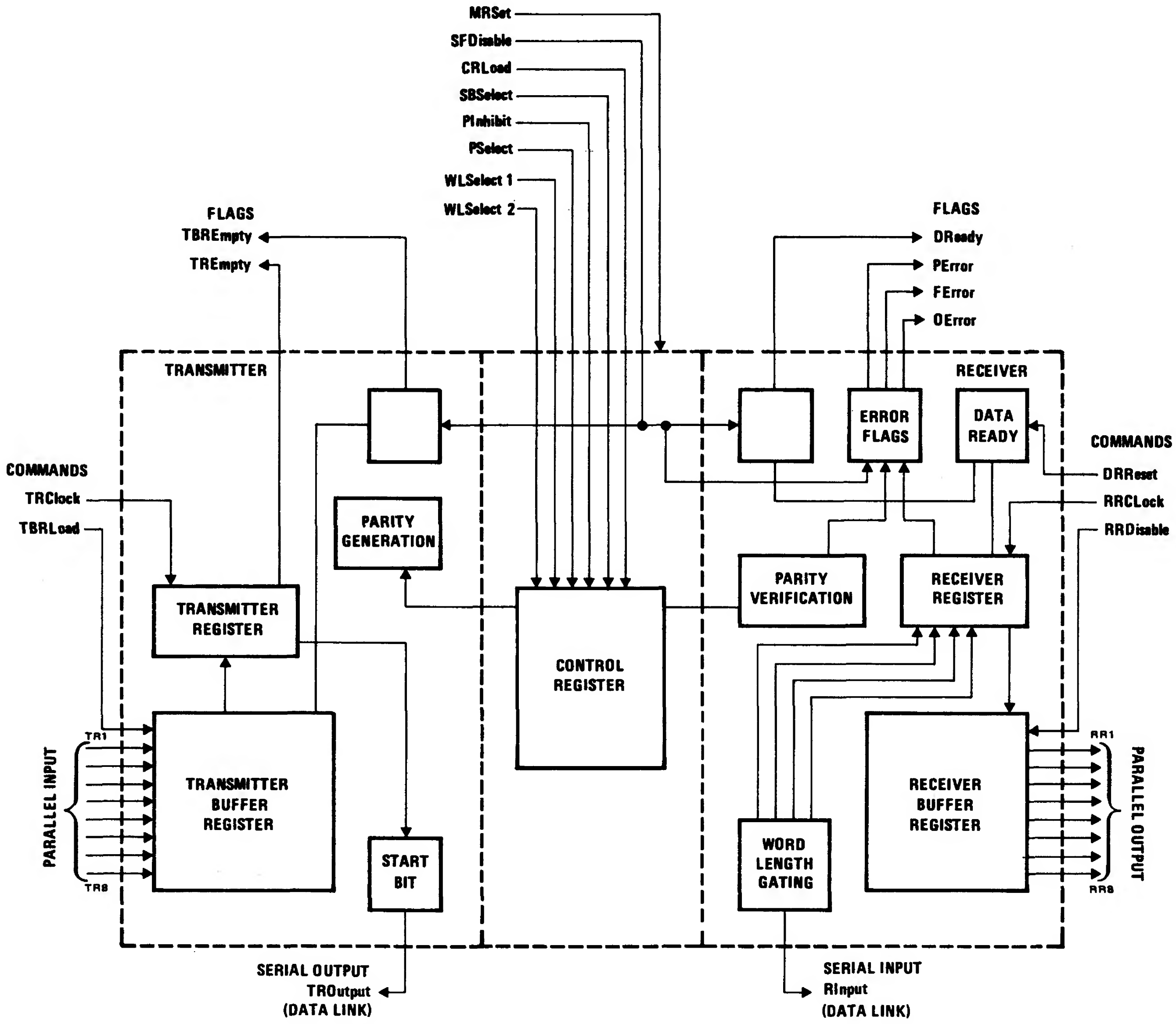

MRSet
SFDisable
CRLoad
SBSelect
PInhibit
PSelect
WLSelect 1
WLSelect 2
FLAGS
TBREmpty
TREmpty
FLAGS
DReady
PError
FError
OError
TRANSMITTER
RECEIVER
ERROR FLAGS
DATA READY
COMMANDS
DRReset
RRCLock
RRDisable
COMMANDS
TRClock
TBRLoad
PARITY GENERATION
TRANSMITTER REGISTER
CONTROL REGISTER
PARITY VERIFICATION
RECEIVER REGISTER
TR1
TR8
PARALLEL INPUT
TRANSMITTER BUFFER REGISTER
START BIT
WORD LENGTH GATING
RECEIVER BUFFER REGISTER
RR1
RR8
PARALLEL OUTPUT
SERIAL OUTPUT
TROutput
(DATA LINK)
SERIAL INPUT
RInput
(DATA LINK)

FIGURE 1. TMS6011 Functional Block Diagram

parallel. The transmitter section will accept parallel data, convert it to serial form and generate the start, parity and stop bits. Receiver and transmitter sections are separate and the device can operate in full duplex mode.

To allow maximum flexibility of operation; the device has also been designed as a fully programmable circuit, i.e. it can operate either in full duplex mode (simultaneous transmission and reception) or in half duplex mode (alternate transmission and reception). Also the data word may be externally selected to be 5, 6, 7 or 8 bits long. Figure 2 shows the format of an 8 bit word. The baud rate is externally governed by the clock frequency. The parity, which is generated in the transmit mode and verified in the receive mode, can be selected as either odd or even. It is also possible to disable the parity bit by inhibiting the parity generation and verification. The stop bits can be selected as either one or two bits. The data holding registers are static and will hold a data word until it is replaced by another word. To allow for a wide range of possible configurations, three state 'push-pull' buffers are used on all outputs except the transmitter register output, TROutput, and transmitter register empty, TREmpty, flag. They allow the device to be connected in the wired-OR configuration. P-channel enhancement-mode low threshold technology permits the use of standard power supplies (+5V, 0V, −12V) as well as direct interface with transistor-transistor and diode-transistor logic, t.t.l./d.t.l. No external components are needed.

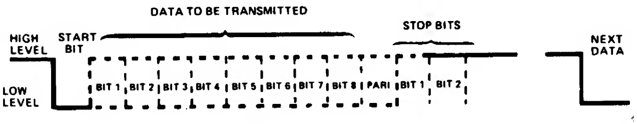


FIGURE 2. Word Format for the TMS6011

OPERATION

The operation of this device can best be understood by visualising it as three separate sections: 1) transmitter, 2) receiver, and 3) common control. The transmitter and receiver sections are independent while the control section directs both receive and transmit.

Transmitter Section

Parallel input data is received on the transmitter buffer register data inputs, TR1 to TR8. A 'low' on the transmitter buffer register load, TBRLoad, command terminal will load a character into the transmitter buffer register. The data is transferred to the transmitter register when TBRLoad terminal goes from a 'low' to a 'high'. If the transmitter section is already transmitting data, indicated by TREmpty being 'low', the loading of the transmitter register is delayed and the new data word is held in the transmitter buffer register until the transmission of the previous data word is completed, as shown in Figure 3.

Serial output data transmitted on the TROutput terminal is clocked out by the transmitter register clock, TRClock. The data rate is 16 times slower than the clock rate. When no data is transmitted the TROutput sits at a 'high'. The start of the transmission is defined as the transition of TROutput from a 'high' to a 'low'. Two flags are provided. A 'high' on the transmitter buffer register empty, TBREmpty, flag indicates that a word has been transferred to the transmitter register and that the transmitter buffer register is now ready to accept a new word. A 'high' on the TREmpty flag indicates that the transmitter section has completed the transmission of a complete word, including stop bits. The TREmpty flag will sit at a 'high' until the start of transmission of a new word. Both transmitter buffer register and transmitter register are static and will maintain stored data in the absence of clock pulses.

Receiver Section

The serial data from the receiver input, RInput, enters the receiver register at a point determined by the character length, the parity and the number of stop bits. RInput must be maintained 'high' when no data is being received. The data is clocked by the receiver register clock, RRClock. The clock rate is 16 times faster than the data rate. Data is transferred from the receiver register to the receiver buffer register and is presented in parallel form on the eight three-state data outputs RR1 to RR8. When a 'high' is applied to receiver register disable, RRDisable, terminal, the RR outputs are high impedance, RR1 is the least significant bit and RR8 is the most significant bit. A 'low' applied to the data ready reset, DRReset, terminal resets the data ready, DReady, output to a 'low'.

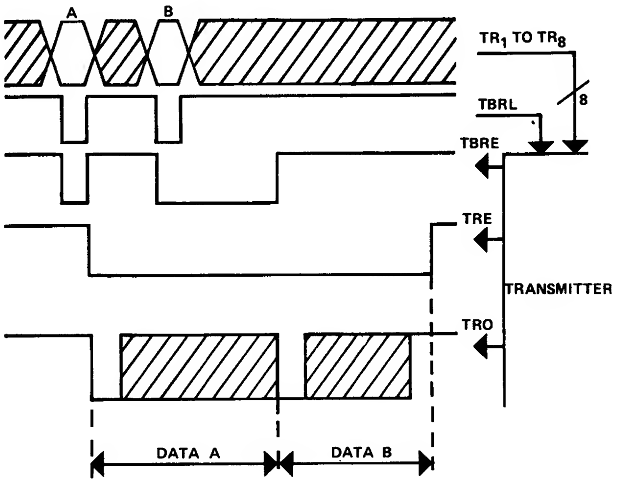


FIGURE 3. Transmitter Operation at High Word Rates

Four flags are provided in the receiver section i.e. three error flags (parity error, PError; framing error, FError; and overrun error, OError) and a data-ready, DReady, flag. All status flags may be disabled by a logic 'high' on the status flag disable, SFDisable, terminal. A 'high' on the PError terminal indicates an error in parity. A 'high' on the OError terminal indicates an overrun which occurs when the previous word was not read, i.e., when the DReady line was not reset before the current data was transferred to the receiver buffer register. A 'high' on the DReady terminal indicates that a word has been received, stored in the receiver buffer register and that the data is available on RR outputs.

Common Control Section

The initial reset of the device is performed through the master reset, MReset, terminal. The MReset is strobed 'high' after power turn 'on' to reset all registers and the TROutput line to a 'high'. All status flags (PError, FError, OError, DReady, TBREmpty) are disabled when the SFDisable is at a 'high'. When disabled, the status flags are in the high impedance state. The number of bits per word is selected by the word length select terminals, WLSelect 1 and WLSelect 2, to be 5, 6, 7 or 8 bits, as shown in Table 1.

A 'high' on the parity select, PSelect, line selects even parity and a 'low' odd parity. The parity will not be checked or generated if a 'high' is applied to parity inhibit, PInhibit; in this case the stop bit or bits will immediately follow the data bit. When a 'high' is applied to PInhibit, the PError status flag changes to a 'low', indicating a no-parity error since parity is disregarded in this mode. To select either one or two stop bits, the stop bit select, SBSelect, terminal is used. A 'high' on this terminal will result in two stop bits while a logic 'low' will produce only one. To load the control bits (WLSelect 1, WLSelect 2, PSelect, PInhibit, SBSelect), a 'high' is applied to the control register load, CRLoad, terminal. This terminal may be strobed or 'hardwired' to a 'high' level.

Table 1. Input Requirements

Pin	Symbol	Function	Requirement
1	V_{SS}	V_{SS} power supply	Voltage +5V
2	V_{GG}	V_{GG} power supply	Voltage −12V
3	V_{DD}	V_{DD} power supply	Ground
4	RRD	Receiver register disable	A 'high' disconnects RR from RBR. (The outputs of RBR are all high impedance). A 'low' connects RR to RBR and enables RR outputs. (Not used bits are 'low').
16	SFD	Status flags disable	A 'high' disables the outputs of the error and function indicators PE, FE, OE, DR and TBRE.
17	RRC	Receiver register clock	The RRClock rate is 16 times the received baud rate.
18	DRR	Data ready reset	A 'low' resets the DR output.
20	RI	Receiver input	Serial data from RI is entered into the RR according to the selected word length, parity and the number of stop bits. RI must be 'high' when not in use.
21	MR	Master Reset	A 'high' resets the registers and sets TRE, TRO and TBRE to a 'high' and DR, OE, FE and PE to a 'low'. MR is independent of clock. It does not reset the RBR.
23	TBRL	Transmitter buffer register load	A 'low' loads the word into the TBR. On the transistions 'low' to 'high' the word is transferred into the TR. If TR is still transmitting (i.e. TRE is 'low') the transfer is delayed until the transmission has been terminated. The serial transmission of that new word starts simultaneously with the transfer.
26-33	TR1-8	Transmitter register input	The 8 inputs are loaded into the TBR by TBRL. If the word length is selected to be less than 8 bits by WLS1 and WLS2 only the least significant bits are accepted. The least significant input is TR1. If the word length is n bits, then the (n + 1) data input must be held at a 'high' to prevent transition errors at the beginning of the parity bit at TRO.
34	CRL	Control register load	A 'high' loads the control bits WLS1, WLS2, PS, P1 and SBS into the control register. CRL may be strobed or 'hardwired'.
35	PI	Parity inhibit	A 'high' supresses the generation and detection of the parity bit. In this case the stop bits follow the data immediately and PE will be at a 'low'.
36	SBS	Stop bit select	A 'high' selects 2 stop bits, 'low' only one stop bit.
37-38	WLS	Word length select	WLS1 WLS2 Word length (data bits) 'low' 'low' 5 'low' 'high' 6 'high' 'low' 7 'high' 'high' 8
39	PS	Parity select	A 'high' selects even parity and a 'low' odd parity for transmission and reception.
40	TRC	Transmitter register clock	The TR clock rate is 16 times faster than desired transmission baud rate.

Table 2. Output Requirements

Pin	Symbol	Function	Requirement
5-12	RR1-8	RBR data output	If RRD is 'high' all outputs RR1-8 are high impedance. If RRD is 'low', not selected bits are 'low'. The received data appears on the remaining outputs. The least significant bit appears at RR1. A 'high' received is shown as a 'high'.
13	PE	Parity error	A 'high' indicates a detected parity error, 'odd' or 'even' determined by the PS input, if SFD is at 'low'. As the word is transferred from the RR to the RBR the PE indication will be cancelled.
14	FE	Framing error	A 'high' indicates a non valid stop bit, if SFD is at 'low'. As the word is transferred from the RR to the RBR, the FE indication will be cancelled.
15	OE	Overrun error	If SFD is at 'low', a 'high' on OE indicates that the preceeding word has not been read (DR has not been reset) before the new word was written into the RBR. The new word will take the place of the preceeding word in the RBR.
19	DR	Data ready	A 'high' indicates that a complete word has been received and transferred to the RBR.
22	TBRE	Transmitter buffer register empty	A 'high' indicates that the contents of the TBR have been transferred to the TR and that the TBR is now ready to accept a new word.
24	TRE	Transmitter register empty	A 'high' indicates that the transmitter section has completed the transmission of a complete word including stop bits. TRE will remain 'high' until the next start bit.
25	TRO	Transmitter register output	The start of a transmission is indicated by the first transition 'high' to 'low' of this serial output. When no transmission is performed, TRO sits at a 'high'. Transmission is either started by the transition 'low' to 'high' of the TBRL, or the termination of the transmission of the preceeding word.

Table 3. Abbreviations
(See also Tables 1 and 2)

Symbol	Function	Meaning
RR	Receiver register	Serial in, parallel out
RBR	Receiver buffer register	Parallel in, parallel out
TBR	Transmitter buffer register	Parallel in, parallel out
TR	Transmitter register	Parallel in, serial out
'L'		'low', low voltage, logic '0'
'H'		'high', high voltage, logic '1'
'H'-'L'		Transition from 'H' to 'L'
'L'-'H'		Transition from 'L' to 'H'
⎍		'H' pulse, strobe 'high'
⊔		'L' pulse, strobe 'low'
LSB		Least significant bit
MSB		Most significant bit

A summary of the inputs and output requirements is given in Tables 1 and 2. The flow diagram, Figure 4, explains the step sequence in the receiving and transmitting functions, and Table 3 lists the abbreviations used.

Timing

Figure 5 shows a timing diagram of the reception principle of a 5 data bit word with parity and two stop bits.

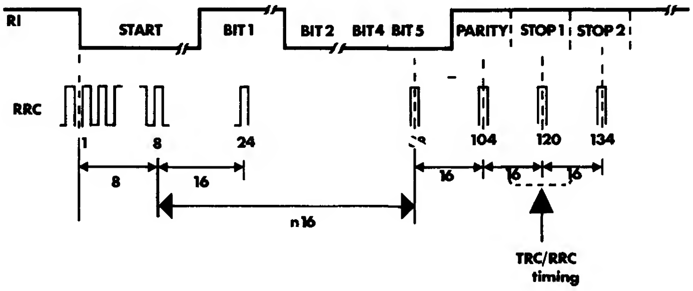


FIGURE 5. Reception Principle

Each transmitted bit is 16 clock periods in length. On the first transition 'high' to 'low' of the receiver input signal, an internal counter is reset and after 8 clock pulses the start bit is verified. After every 16 subsequent clock pulses, the serially incoming bits (data, parity, stop) are strobed and written into the receiver register RR. After the reception of the first stop bit, error conditions are detected and indicated (on the 'low' to 'high' transition of the clock) and the data is available (after the next 'high' to 'low' transition of the clock). Figures 6 and 7 show the timing conditions in more detail.

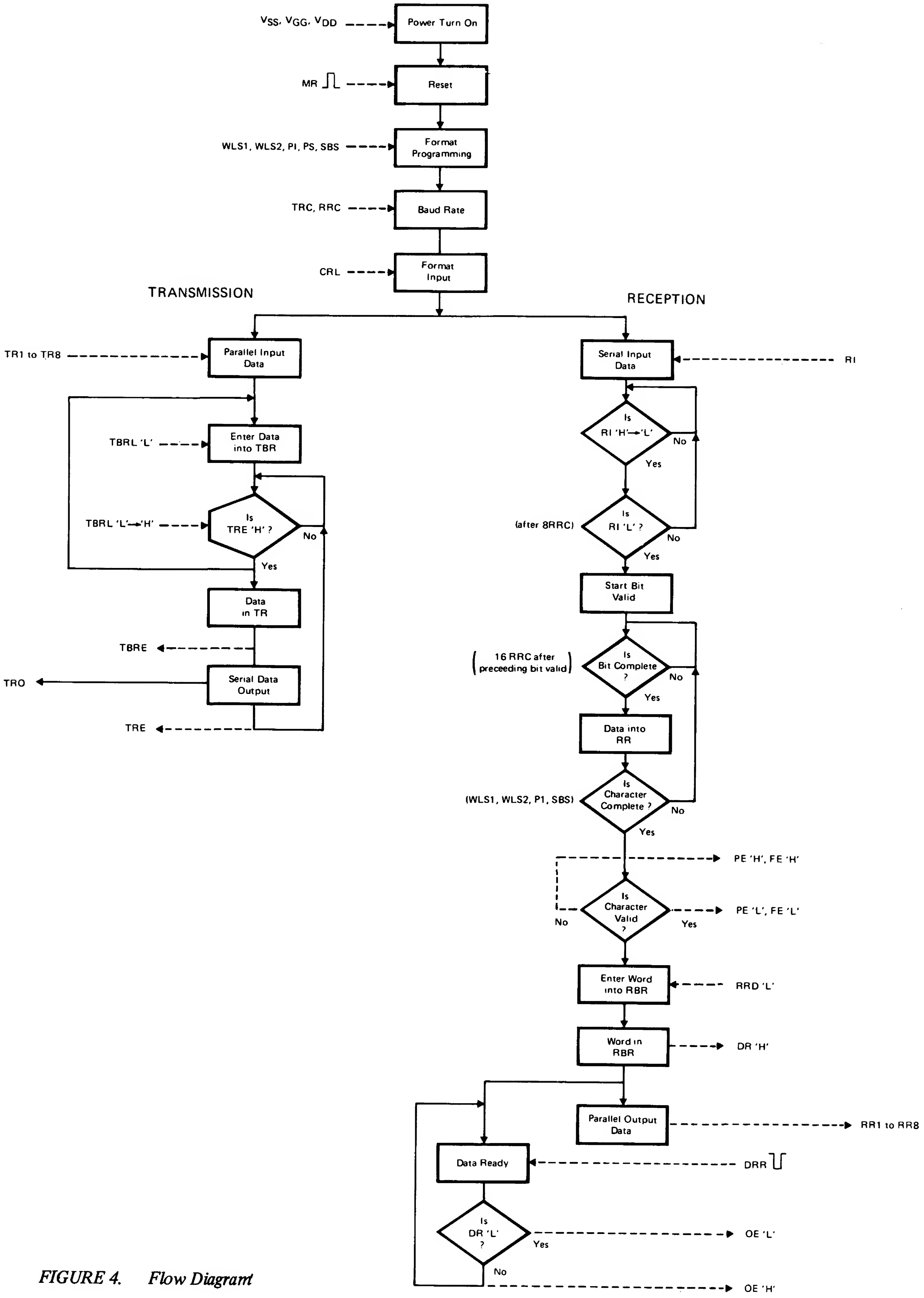

VSS, VGG, VDD
Power Turn On
MR
Reset
WLS1, WLS2, PI, PS, SBS
Format Programming
TRC, RRC
Baud Rate
CRL
Format Input
TRANSMISSION
RECEPTION
TR1 to TR8
Parallel Input Data
TBRL 'L'
Enter Data into TBR
TBRL 'L'→'H'
Is TRE 'H' ?
No
Yes
Data in TR
TBRE
TRO
Serial Data Output
TRE
Serial Input Data
RI
Is RI 'H'→'L'
No
Yes
(after 8RRC)
Is RI 'L' ?
No
Yes
Start Bit Valid
(16 RRC after preceeding bit valid)
Is Bit Complete ?
No
Yes
Data into RR
(WLS1, WLS2, P1, SBS)
Is Character Complete ?
No
Yes
PE 'H', FE 'H'
Is Character Valid ?
No
Yes
PE 'L', FE 'L'
Enter Word into RBR
RRD 'L'
Word in RBR
DR 'H'
Parallel Output Data
RR1 to RR8
Data Ready
DRR
Is DR 'L' ?
Yes
OE 'L'
No
OE 'H'

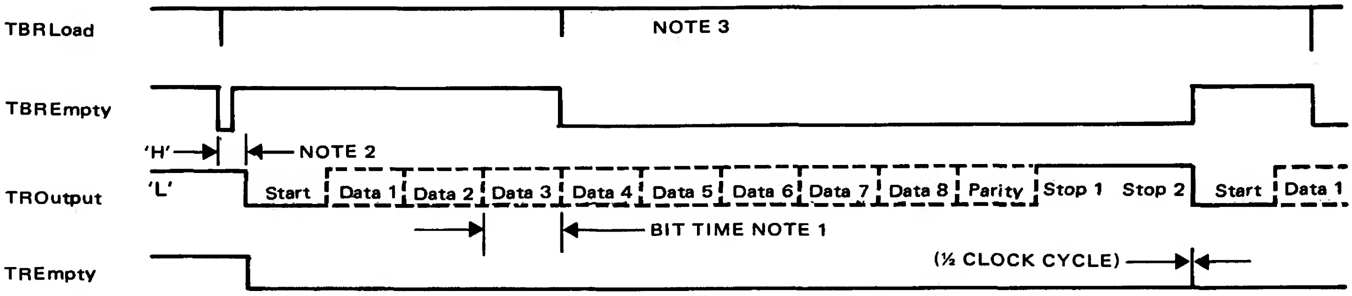
FIGURE 4. Flow Diagram

It should be noted that:—

– RR outputs and DReady become valid at a negative transition of the RRClock whereas error flags become valid at a positive transition.

–If during the transmission of a character, a new data strobe occurs, TBRLoad going from a 'low' to a 'high', the new character is transmitted immediately following the preceeding word. The TREmpty will be 'high' only during half a cycle of TRClock.

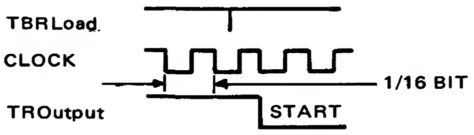
–Error flags are reset by MReset or overwritten by



TBRLoad
NOTE 3
TBREmpty
'H'
NOTE 2
TROutput
'L'
Start
Data 1
Data 2
Data 3
Data 4
Data 5
Data 6
Data 7
Data 8
Parity
Stop 1
Stop 2
Start
Data 1
BIT TIME NOTE 1
TREmpty
(½ CLOCK CYCLE)

Transmitter initially assumed inactive at start of diagram, shown for 8 level code and parity and 2 stops.

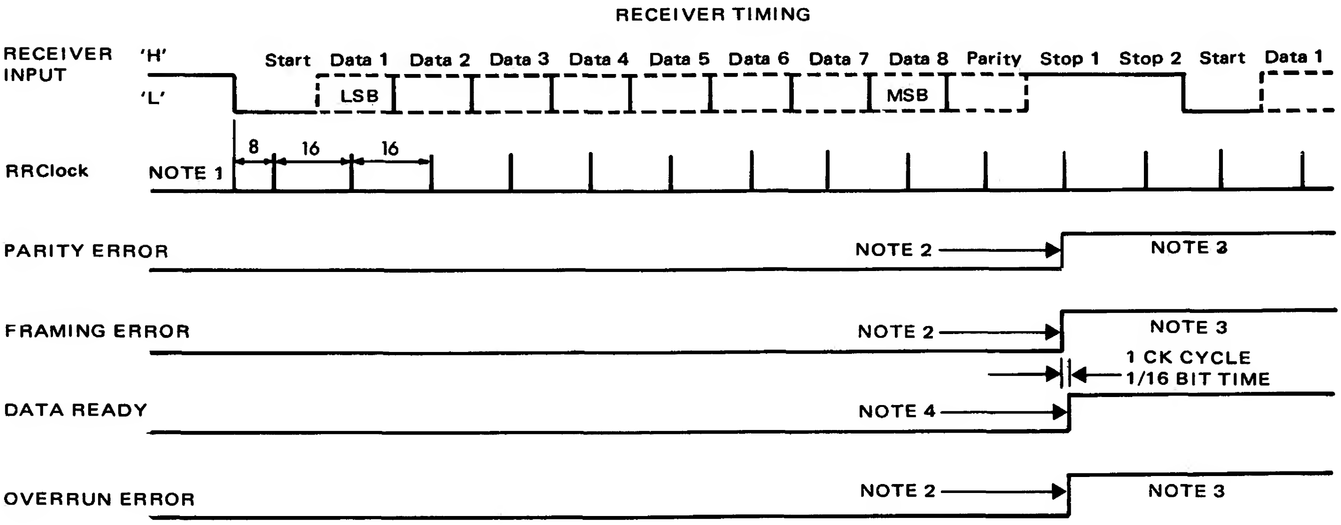
NOTES:
1. Bit time is 16 clock cycles.
2. If transmitter is inactive the start pulse will appear on line within one clock cycle of time data strobe occurs (see detail below).



TBRLoad
CLOCK
1/16 BIT
TROutput
START

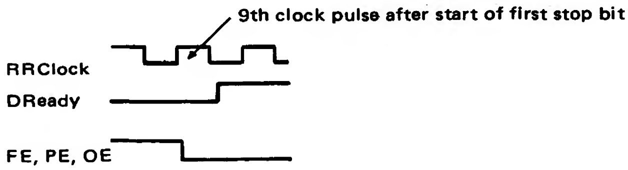
3. Because transmitter is double buffered, another data strobe can occur anywhere during transmission of character 1.

FIGURE 6. Details of Transmitter Timing



RECEIVER TIMING
RECEIVER INPUT
'H'
'L'
Start
Data 1
Data 2
Data 3
Data 4
Data 5
Data 6
Data 7
Data 8
Parity
Stop 1
Stop 2
Start
Data 1
LSB
MSB
8
16
16
RRClock
NOTE 1
PARITY ERROR
NOTE 2
NOTE 3
FRAMING ERROR
NOTE 2
NOTE 3
1 CK CYCLE
1/16 BIT TIME
DATA READY
NOTE 4
OVERRUN ERROR
NOTE 2
NOTE 3

NOTES:
1. Only every 16th clock pulse is shown.
2. This is the point at which the error condition is detected, if error occurs (see detail below).



9th clock pulse after start of first stop bit
RRClock
DReady
FE, PE, OE

3. Error flags are reset by MR or overwritten by next CORRECTLY received word.
4. DReady is SET only when received data has been transferred to the buffer register.

FIGURE 7. Details of Receiver Timing

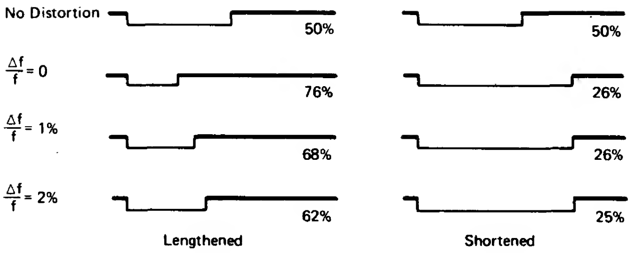


FIGURE 8.
Acceptable Pulse Width Distortion (Measured)

the next correctly received word.

–MReset does not reset the receiver buffer register.

The TRClock and the RRClock may be synchronous (frequency and phase) identical (frequency) or different in frequency and phase. Figure 5 also shows how the acceptable difference in frequency between TRClock and RRClock may be determined for a five data bit word with parity. The number of stop bits is not important as the error indication and the data available occur at the first stop bit. Assuming no distortion, the 120th clock must fall within the first stop bit, i.e. there is an allowable deviation of ±8 clock pulses. The difference between TRClock and RRClock is then 8 ÷120, i.e. 6.6% deviation. Similarly for an 8 data bit word the deviation is 8 ÷ 168, i.e. 4.76%. Hence with no distortion on the transmitting path the two clocks may differ in frequency up to 6.6% for a 5 data bit word, and 4.76% for an 8 data bit word. Table 4 shows measured acceptable frequency deviations for an 8 data bit word. As distortion of the transmitted character occurs, in practice less frequency deviation is acceptable. Figure 8 shows the acceptable pulse distortions for clock frequency deviations of 1% and 2%, as measured, for all possible 8 data bit plus parity characters. Figure 9 shows the clock to output time delays. For very high speed applications these delays must be taken into account. Worst case and typical values are given in the Data Sheet together with other operating conditions.

Table 4. Acceptable Frequency Deviation between TRC and RRC (no distortion) for an 8 data bit and parity character transmission

f (Hz)	200k	40k	4k	600	calculated
$\frac{\Delta f}{f}$ (%)	4.55	4.6	4.7	4.7	4.76

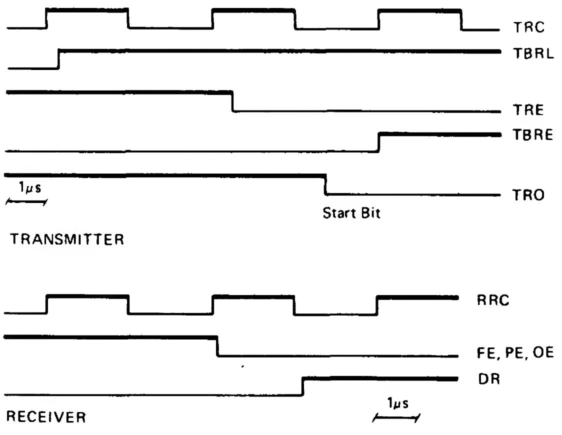


FIGURE 9. Clock to Output Time Delays (Measured)

SUPPLEMENTARY CIRCUITS

Clock Generation

As just described, the allowable frequency deviation between clocks varies between 4.76% and 6.6% dependent on word length. It is therefore not necessary to transmit clock separately or to relate clock phases at transmitter and receiver. It is however necessary to ensure that the clock frequencies are within 4% of one another, i.e. a tolerance of ± 2% on two nominally equal clocks is allowable. There are several methods of generating these clocks.

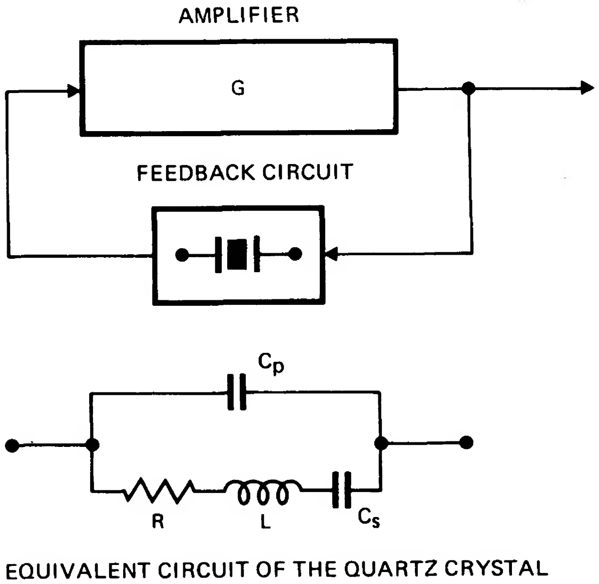


FIGURE 10. Crystal Oscillator

As shown in Figure 10 the equivalent circuit of a quartz crystal is that of a series RLC circuit in parallel with a capacitor C. The latter represents the inter-electrode capacitance of the crystal and its connections. Therefore, the crystal may resonate in a series or a parallel mode depending on the way it is excited. The oscillator circuits to be described use the crystal in the series mode. Digital devices may be used as the amplifier blocks of the oscillator circuits providing they are used in the linear portion of their transfer characteristic. This may be achieved by introducing a resistor from the output to the input of an inverter. As a crystal oscillator needs a non-inverting amplifier, two inverting stages may be used in cascade.

Figure 11 shows two simple oscillators using invertors employing low power and standard t.t.l. devices. The former may be used up to 1MHz, the latter up to about 10MHz. These oscillators are self starting and the frequency deviation as a function of supply voltage is less than 10 ppm/volt. For higher frequencies specially designed circuits may be used, e.g. the SN74S124 voltage controlled oscillator. The

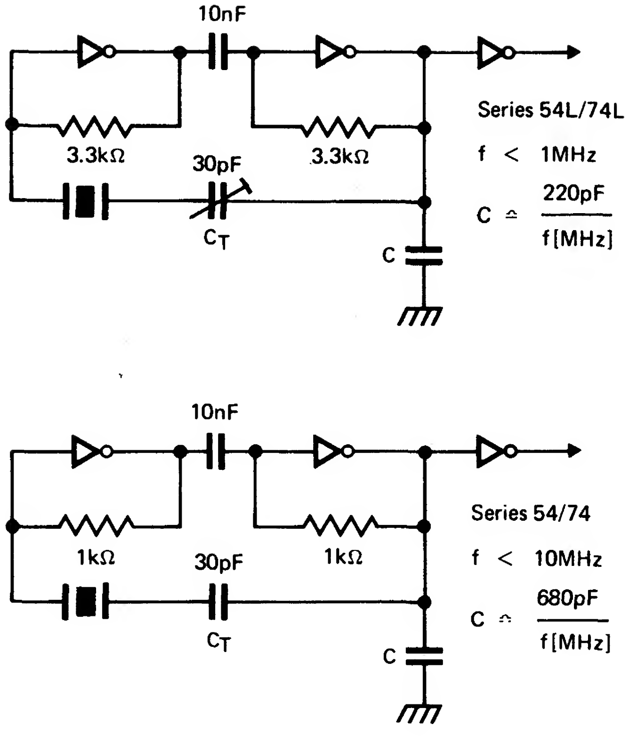


FIGURE 11. Crystal Oscillator using Series 74 Inverters

frequency deviation as a function of temperature is essentially determined by the quartz crystal itself. For example with a 10MHz oscillator a frequency deviation of 1 ppm/°C may be expected.

Figure 12 shows another way of generating the clock pulses using a SN75115 line receiver device. This solution is attractive when other line receivers are used in the system. As shown a 100kHz crystal has been used in the basic oscillator section. The output from this could be divided as shown, if required, to give lower frequencies for the clock to the UART and for a −12V generator.

Generation of −12V Supply

Normally a −12V supply is not available in a t.t.l. system. Instead of using an additional −12V power supply it is preferable to generate the −12V locally from the logic +5V supply. Figure 13 shows an unstabilized circuit which is useful when line driver devices are used in the system. Although the output from this circuit may not be within the data sheet limits given for the TMS6011 it is adequate for this system, bar the highest clock frequencies. The SN75113 line driver device, operating as a push-pull switch, supplies the current through the transformer to the rectifier circuit. The turns ratio is given by the input-output voltage ratio. The output voltage will be dependent on the +5V supply and to some extent the load. The main advantage of this circuit is that current transients are not introduced into the +5V supply as is the case with a switching power supply.

A second method using a switching circuit^2, is shown in Figure 14. The basic idea here is to magnetize an inductor, L, from the available supply via the switching transistor, VT1, then to discharge the stored energy into a capacitor, C, via the diode, D. A series stabilisation to allow for variations in load or supply voltage is provided by the zener diode, ZD, and the emitter follower transistor, VT2. The disadvantage of this circuit is the rather high current pulses on the supply rail, relatively high power dissipation, and, especially in telecommunication applications, the radiated interference.

To accommodate much larger variations in supply voltage or load, the circuit shown in Figure 15 may be used.^{3,4} This will supply an output current of between 6 and 20mA and uses an SN74121 monostable i.c. as the mark/space modulator. Feedback from the output to the mark/space modulator is provided via the zener diode ZD. Unlike the circuit in Figure 14, this self regulating circuit uses a sufficiently large inductor (L) so that the rate of change of current through the inductor is very much slower. Hence by varying the mark/space ratio of the switching waveforms to obtain regulation, the peak value of the inductor charging current is controlled. The input/

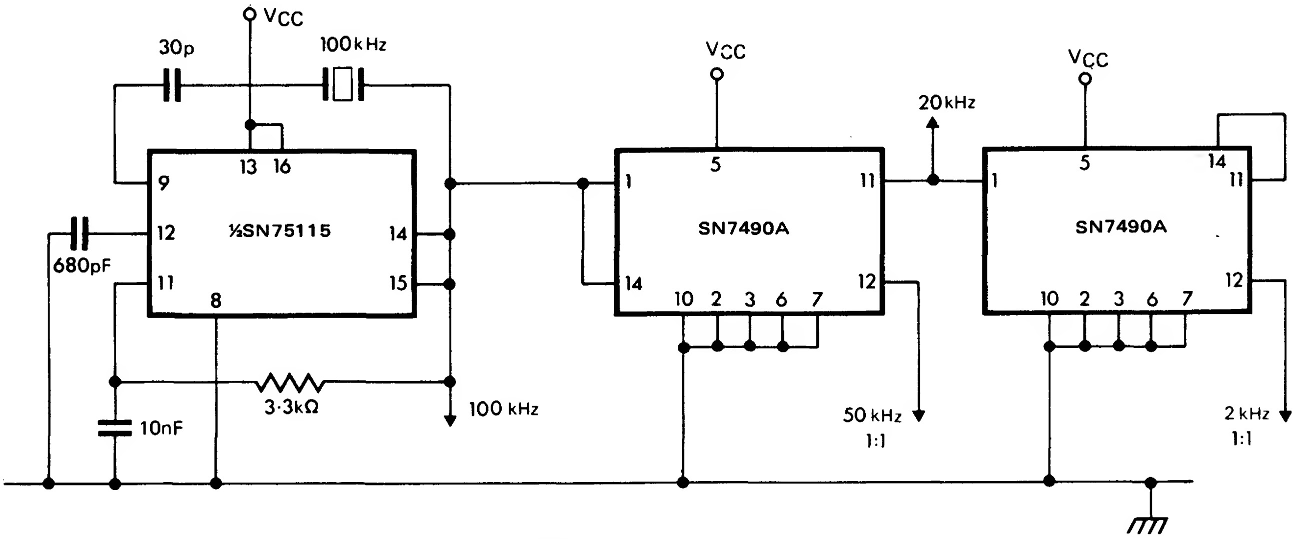


FIGURE 12. Multiple Frequency Clock Generator

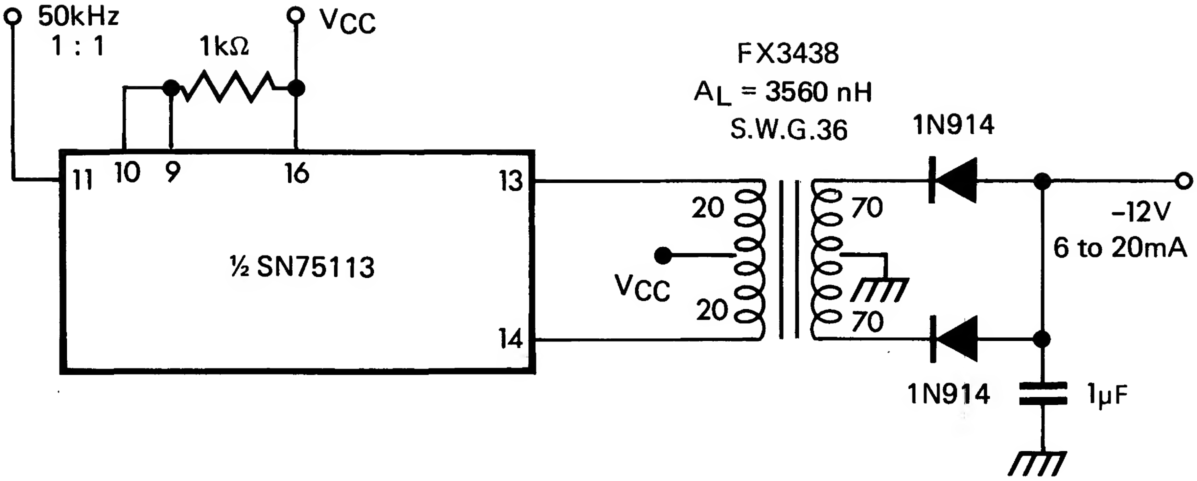

50kHz
1 : 1
1kΩ
VCC
11
10
9
16
13
14
½ SN75113
FX3438
A_L = 3560 nH
S.W.G.36
1N914
20
20
VCC
70
70
-12V
6 to 20mA
1N914
1μF

FIGURE 13. −12V Supply for the TMS6011

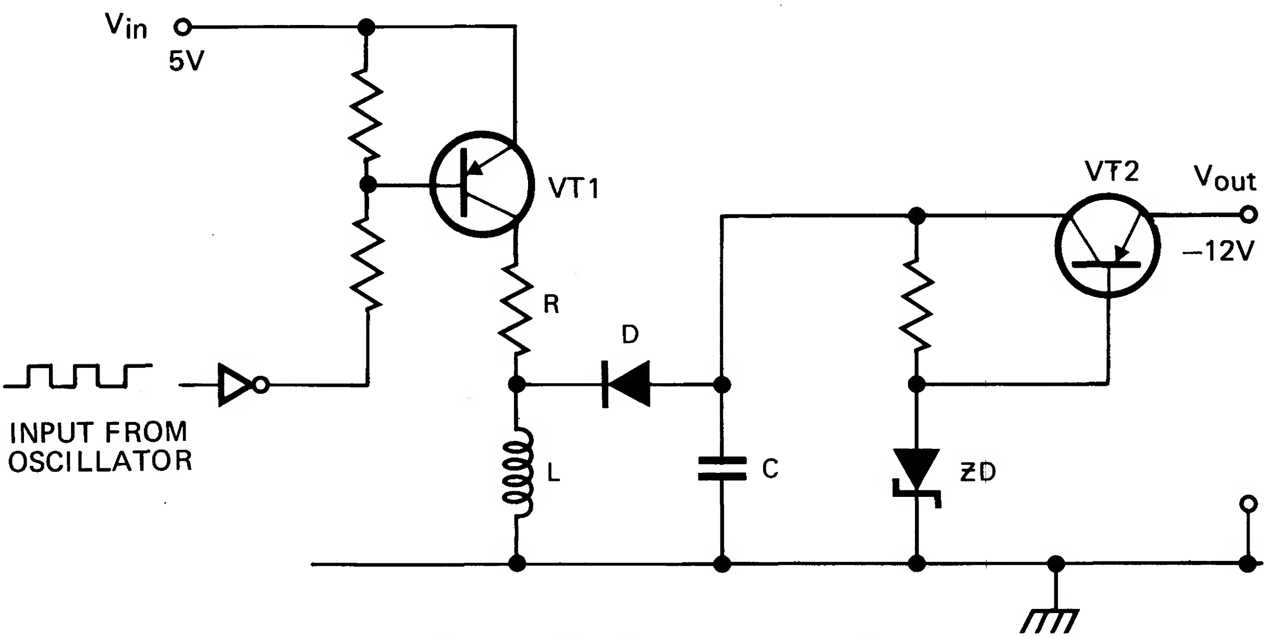
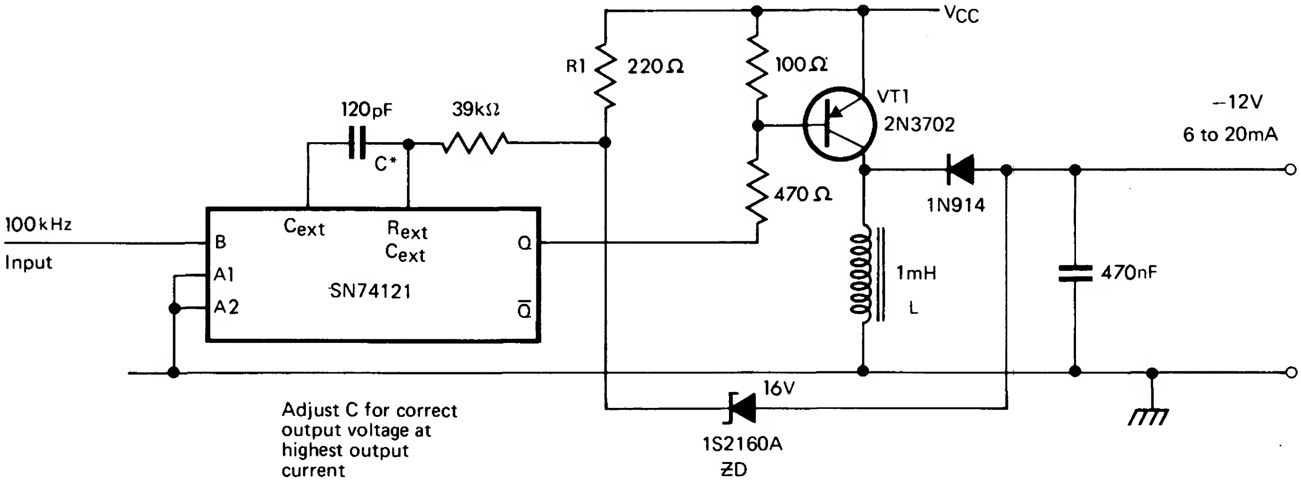

Vin
5V
VT1
R
D
L
C
ZD
VT2
Vout
−12V
INPUT FROM
OSCILLATOR

FIGURE 14. 'Pump' type +5V/−12V Converter


VCC
R1
220Ω
100Ω
VT1
2N3702
120pF
39kΩ
C*
470Ω
1N914
−12V
6 to 20mA
100kHz
Input
B
A1
A2
Cext
Rext
Cext
SN74121
Q
Q̄
1mH
L
470nF
16V
1S2160A
ZD

Adjust C for correct output voltage at highest output current

FIGURE 15. +5V/−12V D.C. Converter

output voltage ratio is directly related to the 'on'/'off' ratio of the switch; as is also the supply current/load current ratio. Since the peak currents are smaller and rate of change of current slower, considerably less radiated interference occurs. The mark/space modulator regulator renders the series regulator unnecessary and therefore the dissipation is considerably reduced.

APPLICATIONS

Transmission Modes

Undirectional Transmission: The transmission of characters is from a data source to a data sink, and is achieved using the TMS6011 device as shown in the top section of Figure 16. An example of the use of this mode would be, for example, from a mini-computer to a print-out peripheral.

Bidirectional Transmission: Data is exchanged in both directions each station being both transmitter and receiver. The ease with which they may be achieved, using the TMS6011 device, is indicated in the lower section of Figure 16. The data rate and format must be identical at both ends. Examples of this mode are the access to a teletype or a tape store. Figure 17 shows the principle of the latter application.

Multidirectional Transmission: Often many data sources and sinks must have interconnections between them. A controller is necessary to direct the exchange of all the information which passes through it. Hence a multidirectional transmission comprises by two bidirectional transmissions, i.e. between source and controller, and between controller and sink. A typical example of such an application is the interface of several peripherals to a computer as indicated in Figure 18. In some cases one of the sources or sinks may do the job of a controller, as shown in Figure 19. The interconnections may be through one channel per line or by a party-line system.[5] Thus a method for sharing a single transmission line by several sources and sinks needs either time multiplex or a frequency multiplex equipment.

Digital Data Acquisition System

Structure: To collect data occurring at different places and to transfer this data to an acquisition centre (processor) is a common problem in large distributing, signalling or surveying systems. An example is the collection of the meter readings in a power distributing system. The measured data may be locally stored in a scaler or register (data source). The data then has to be transmitted to the acquisition centre and stored in a memory (data sink). Figure 19 shows the principle of such an acquisition system using party-line connections[5] between metering stations and acquisition centre.

In order to understand this principle assume that:— the data will not exceed 3 digits, there will be up to 4,000 metering stations, transmission speed is not essential. In the metering stations (Figure 20) the pulses from the metering circuit are counted in a 3 digit decimal counter (accumulator). In the acquisition centre the data will be stored in a memory, whose addresses correspond to the metering station addresses. As the collected data is the basis of charging the subscriber, utmost care must be taken not to lose information, not to accumulate erroneous information or to ascribe it to the wrong address. A parity check

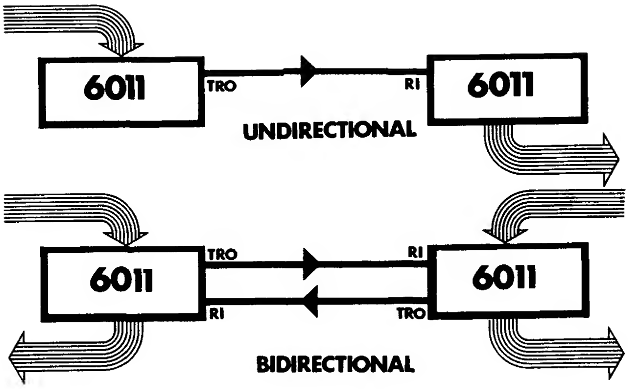


FIGURE 16. Transmission Using the TMS6011

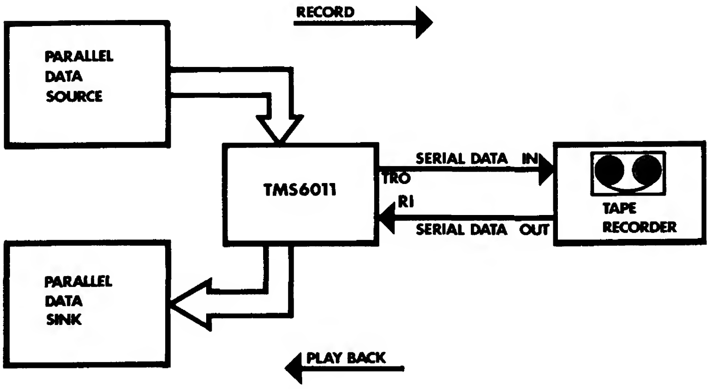


FIGURE 17. Application in a Digital Tape Recorder

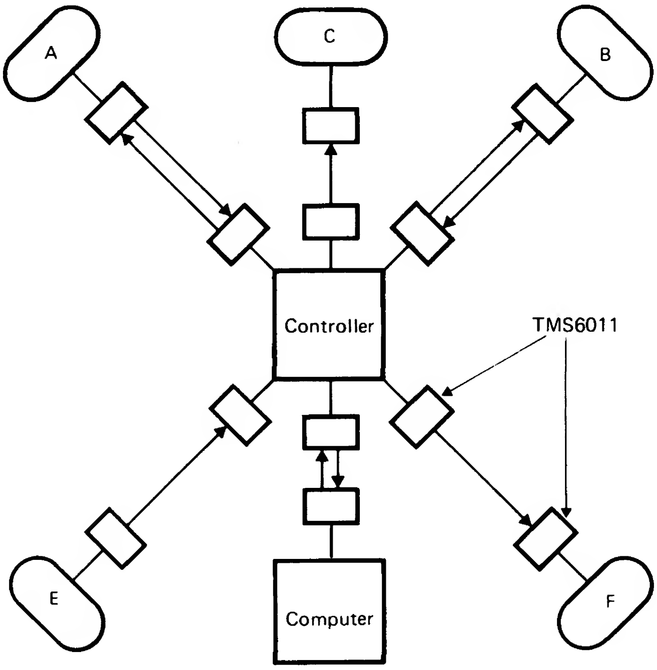


FIGURE 18.
Interconnection of Several Peripherals by a Controller

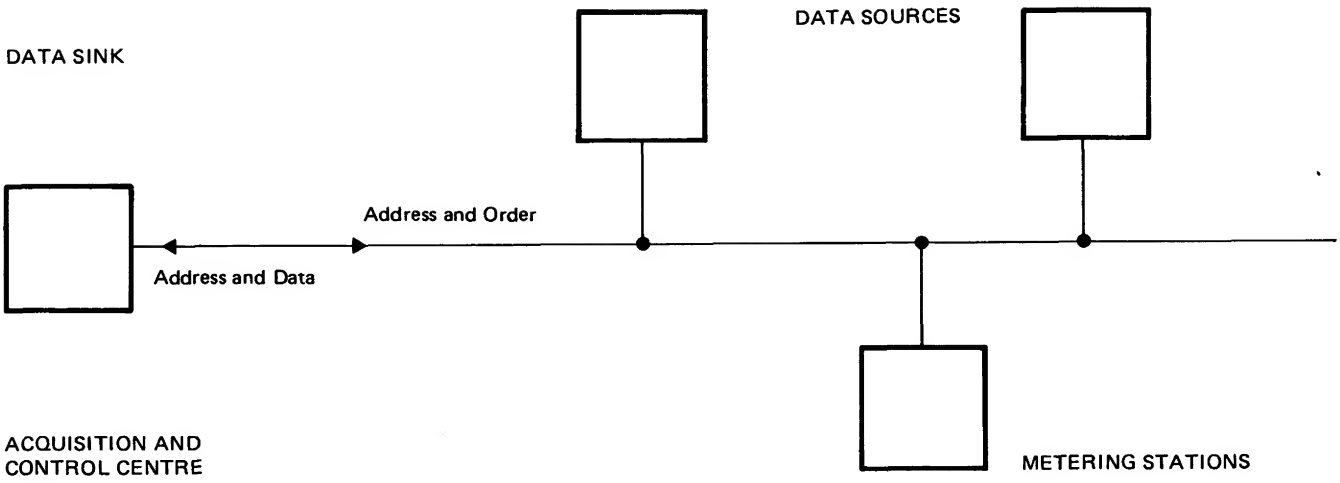

DATA SINK
DATA SOURCES
Address and Order
Address and Data
ACQUISITION AND CONTROL CENTRE
METERING STATIONS

FIGURE 19. Digital Data Acquisition System

covering both the data and the address, and also the link between the data and address on the transmission path, is essential. As the normal data length is 8 bits, it is not possible to transmit the whole 3 digit data (i.e. 16 bits) or the 12 bit address in one operation. Address and data must therefore be split up in sequence for transmission, but interlaced so as not to lose the link between the data and the address. The acquisition centre has to command the commencement of transmission from source to sink and also the reset of the accumulators.

If the data word format for the transmission from the metering station to the acquisition centre is, say XXXX:YYYY, the 4 bits represented by X designate one third of the address (of the source) and the 4 bits represented by Y, contain the decade to be transmitted. The bit arrangement not required for a BCD number (10 to 15) may be used to denote a transmission error from the acquisition centre to the metering stations. It is assumed that the lower significant decades, or parts of addresses, are transmitted before the more significant decades and parts of addresses. If the data word format for the transmission from the acquisition centre to the metering stations is, say, UUUUUU:VW, the 6 bits marked U designate half of the metering station addresses, and the V indicates the lower significant part of the address ('low') or the more significant part ('high'). The bit W is the order bit, commanding the source to transmit the accumulated data ('low') or to reset the accumulator ('high').

The whole data transmission needs, therefore, 5 cycles; 2 cycles for addressing and ordering the source, 3 cycles for transmitting the data from source to sink (acquisition centre).

For example, if the acquisition centre sends to metering station:

1 0 1 1 1 0 : 0 0
1 0 1 0 1 0 : 1 0 it means that

metering station number 2734 has to transmit accumulated data. The metering station replies to the acquisition centre:

1 1 1 0 : 1 0 0 0
1 0 1 0 : 0 1 1 0
1 0 1 0 : 0 0 1 1 indicating

that the metering station number 2734 reads 368.

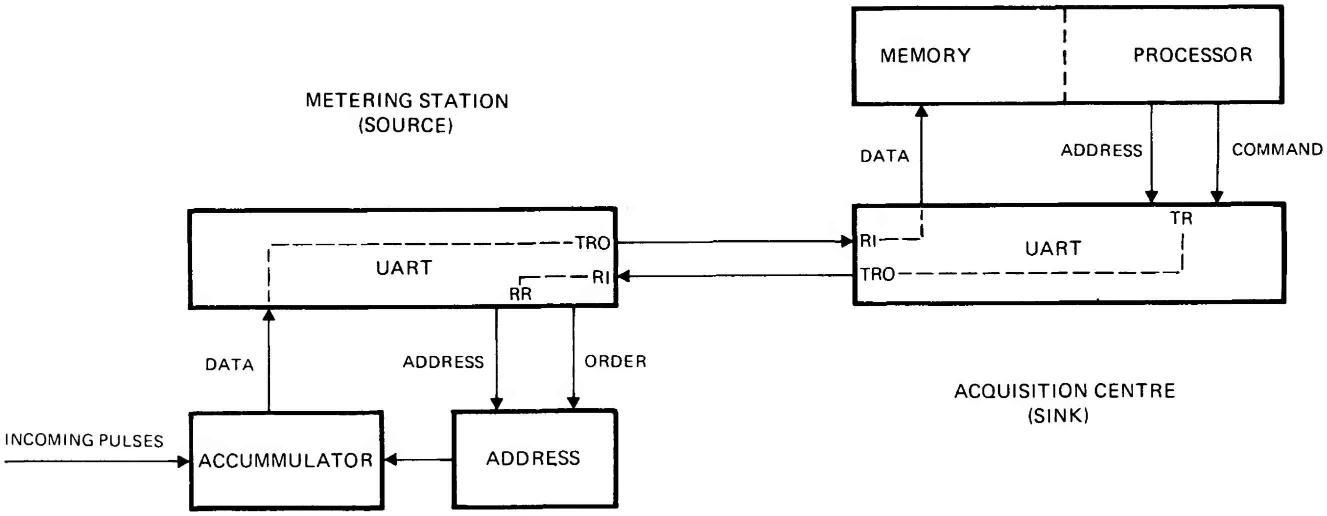

MEMORY
PROCESSOR
METERING STATION (SOURCE)
DATA
ADDRESS
COMMAND
TRO
UART
RI
RR
TR
RI
UART
TRO
DATA
ADDRESS
ORDER
ACQUISITION CENTRE (SINK)
INCOMING PULSES
ACCUMMULATOR
ADDRESS

FIGURE 20. Principle of Operation

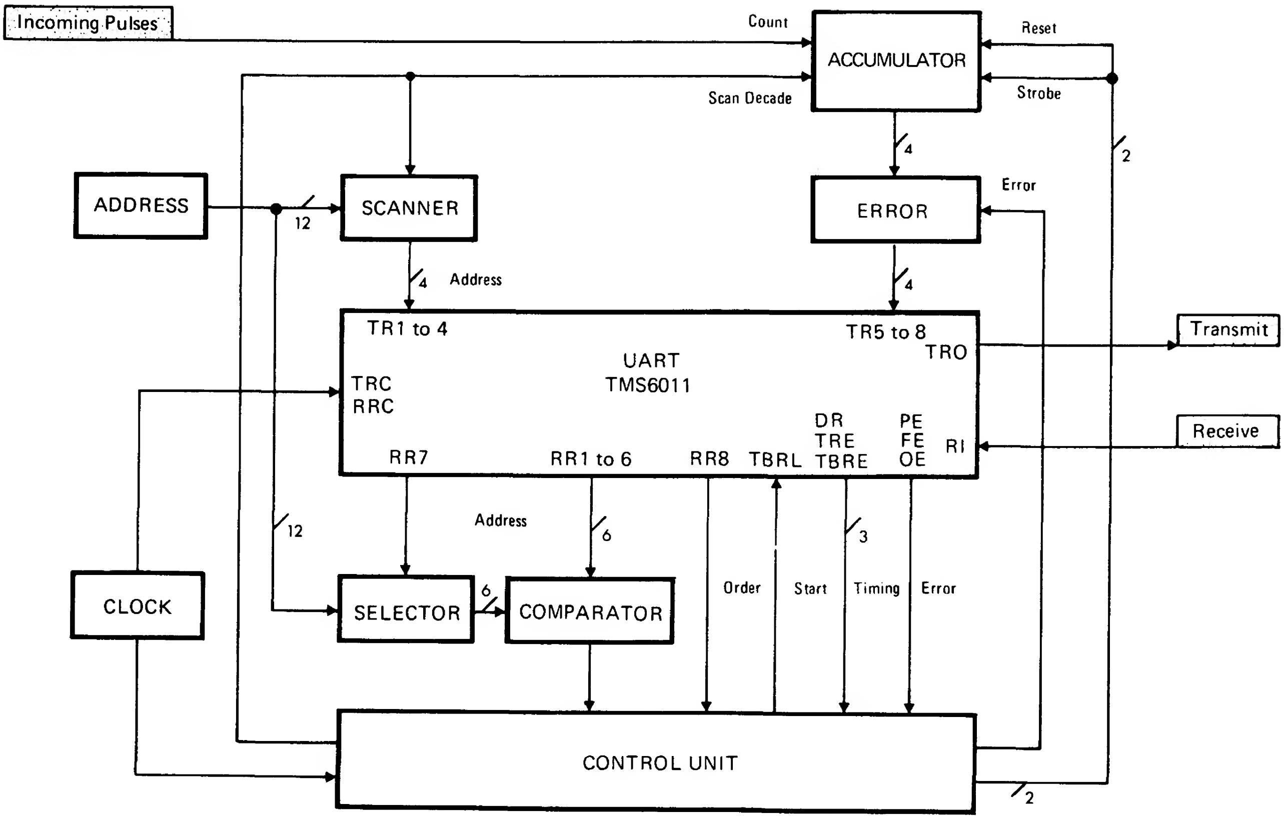

Incoming Pulses
Count
ACCUMULATOR
Reset
Scan Decade
Strobe
4
2
ADDRESS
12
SCANNER
ERROR
Error
4
Address
4
TR1 to 4
UART
TMS6011
TR5 to 8
TRO
Transmit
TRC
RRC
DR
TRE
TBRE
PE
FE
OE
RI
Receive
RR7
RR1 to 6
RR8
TBRL
12
Address
6
3
CLOCK
SELECTOR
6
COMPARATOR
Order
Start
Timing
Error
CONTROL UNIT
2

FIGURE 21. *Source Section of the Digital Data Acquisition System*

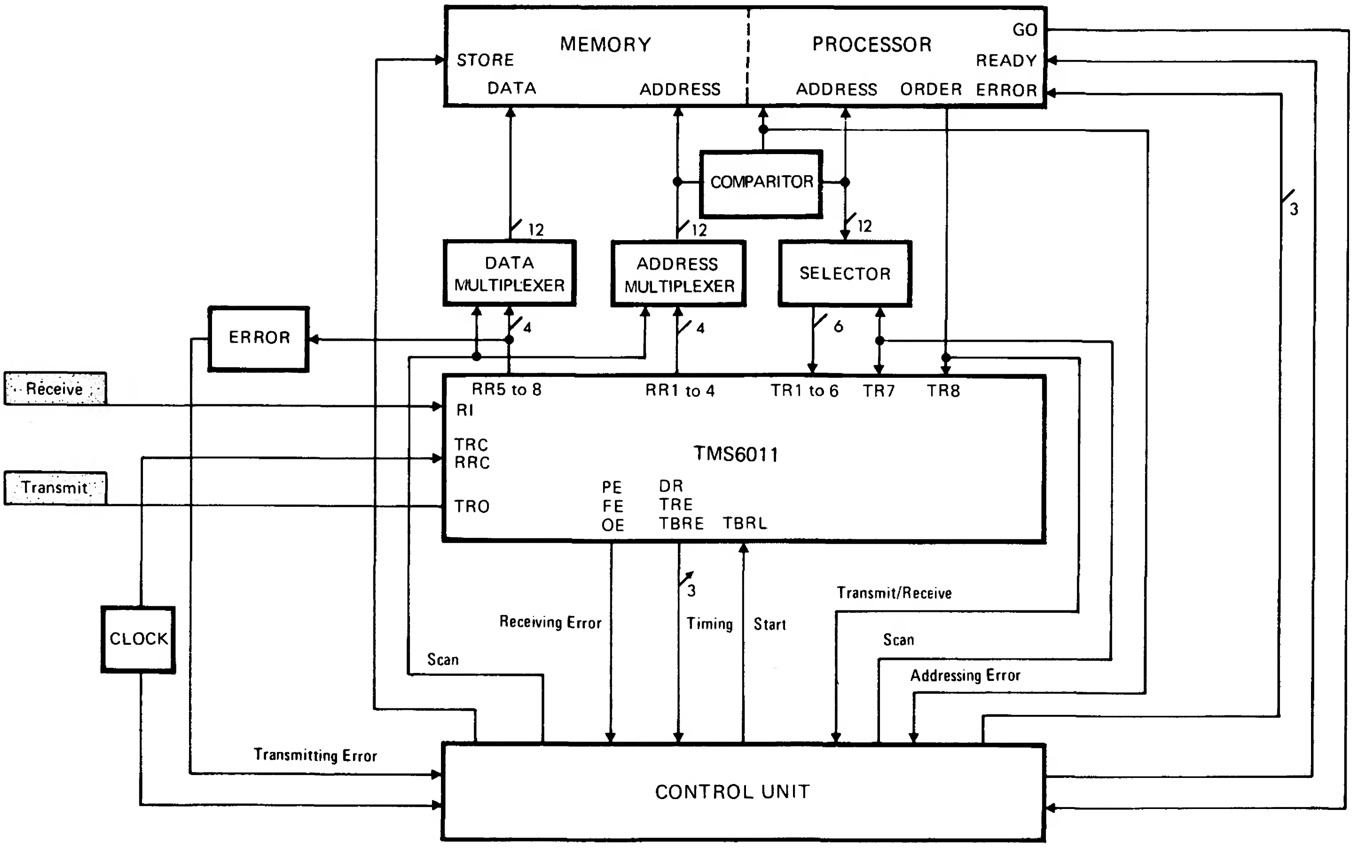

MEMORY
STORE
DATA
ADDRESS
PROCESSOR
GO
READY
ADDRESS
ORDER
ERROR
COMPARITOR
3
12
12
12
DATA
MULTIPLEXER
ADDRESS
MULTIPLEXER
SELECTOR
ERROR
4
4
6
Receive
RR5 to 8
RI
RR1 to 4
TR1 to 6
TR7
TR8
TRC
RRC
TMS6011
Transmit
TRO
PE
FE
OE
DR
TRE
TBRE
TBRL
CLOCK
3
Receiving Error
Timing
Start
Transmit/Receive
Scan
Scan
Addressing Error
Transmitting Error
CONTROL UNIT

FIGURE 22. *Sink Section of the Digital Data Acquisition System*

Practical Implementation: Figures 21 and 22 show the block diagrams of the source and sink sections of the proposed data acquisition system. The central role of the UART can easily be seen, it performing all the timing, parity checking, parallel to serial conversion and vice-versa, and the error detection.

Source Section (Metering Station): The functional blocks of the source section as shown in Figure 21, are:–

–the ACCUMULATOR, which consists of a 3 decade counter, a 3 decade latch, and a multiplexer to route the output of each decade to the output of the device. Such counter/latch/multiplexers could be one i.c. package.

–the ADDRESS, which holds the metering stations, 'hard-wired' address.

–the SCANNER, which routes the address in 3 parts into the UART.

–the SELECTOR, which routes the address in 2 parts into the address comparator.

–the COMPARATOR, which compares the received address with the 'hard-wired' address and determines whether they coincide.

–the ERROR, which alters the transmitted data whenever a receiving error has occurred.

–the UART, which transmits, receives and checks the data flow, and also gives the required timing to the control unit.

–the CONTROL UNIT, which connects together the above mentioned parts. As the timing is performed in the UART, only a small amount of logic is needed.

–the CLOCK, which supplies the UART and the CONTROL UNIT with the appropriate clock pulses and, if needed, the former with the –12V supply.

Sink Section (Acquisition Centre): The functional blocks of the sink section, as shown in Figure 22, are:–

–the PROCESSOR, which is used to evaluate the acquired data and also directs the whole operation.

–the MEMORY, which stores the acquired data.

–the COMPARATOR, which compares the required address with the address that identifies the received data.

–the DATA MULTIPLEXER, which assembles the 3 sequentially transmitted decades to the 3 digit data.

–the ADDRESS MULTIPLEXER, which assembles the 3 sequentially transmitted address parts to the whole address.

–the ERROR, which detects any error configuration transmitted by the metering station.

–the SELECTOR, which selects the lower or more significant half of the address for command of the metering station.

–the CONTROL UNIT which connects the above mentioned parts. As the timing is performed by the processor and the UART, only a few gates are needed to build the control unit.

–the UART, which transmits, receives and checks the data flow, and also gives the required timing to the Control Unit.

–the CLOCK, which supplies the UART and the Control Unit with the appropriate clock pulses and, if needed, the former with the –12V supply.

REFERENCES

1. *'Semiconductor Circuit Design',* Volume III, Texas Instruments Limited, pp 9-12, April 1972.
2. *'Semiconductor Circuit Design',* Volume I, Texas Instruments Limited, Chapters VII and X, April 1972.
3. *'Semiconductor Circuit Design',* Volume 1, Texas Instruments Limited, Chapter IX, April 1974.
4. Chapter IV
5. *'Semiconductor Circuit Design',* Volume III, Texas Instruments Limited, pp 75-90, April 1974.

ACKNOWLEDGEMENTS

The author would like to thank Texas Instruments Limited and Bryan Norris, Applications Manager, for the opportunity of performing this work at Texas Instruments, Bedford. Thanks are also due to Howard Cook for help in editing.

During preparation and work on the report reference was made to various publications on the TMS6011 from the applications laboratory in Nice of Texas Instruments France.

XIII BINARY AND DECIMAL RATE MULTIPLIERS

by
Bob Parsons

Some processing does not need the power of a c.p.u. or a complete microprocessor. Function generation or a simple arithmetic operation can be performed economically with a rate multiplier. A rate multiplier is a device which can perform a wide variety of mathematic operations such as add, subtract, multiply, divide and rooting and exponential, sine and cosine generation. It needs very few other logic elements except perhaps a clock source and an up-down counter. There is no setting up or timing requirement and no involvement in software.

This chapter is relevant to both binary rate multipliers (b.r.m.) and decimal rate multipliers (d.r.m.) although most of the description and applications will concern b.r.m.s (SN7497). To perform the equivalent decimal application merely substitute a d.r.m. (SN74167) and decimal versions of the counters.

DESCRIPTION

Rate Multiplier Principles

The rate multiplier has two inputs; a pulse train of average input rate, r, and a parallel number input X where $0 \leqslant X < 1$. The output of the rate multiplier is a pulse train of average frequency equal to the product of its two inputs, i.e. r.X.

The principle of the rate multiplier is best illustrated by means of Figures 1 and 2. The multiplier consists of a binary counter whose outputs are fed to pulse differentiators ('one-shots') which trigger when the binary outputs change from a logical '0' to a logical '1'. The output of each differentiator is ANDed with a control bit of the multiplier x. The outputs of these AND gates are, therefore, of pulse repetition frequency (p.r.f.) r/2, r/4, r/8 and r/16. Figure 2 shows that no two gate outputs can be coincident. It is, therefore, possible to use an OR function to algebraically add the pulse outputs from the AND gates. The output from the OR gate is therefore a pulse train of rate equal to the sum of the input rates, i.e.

$$\text{Rate output} = r(x_4/2 + x_3/4 + x_2/8 + x_1/16)$$
$$= x.r.2^{-n}$$

The multiplier can be represented diagramatically as shown in Figure 3.

The logical implementation of Figure 1 suffers from several disadvantages. The ripple counter introduces delays

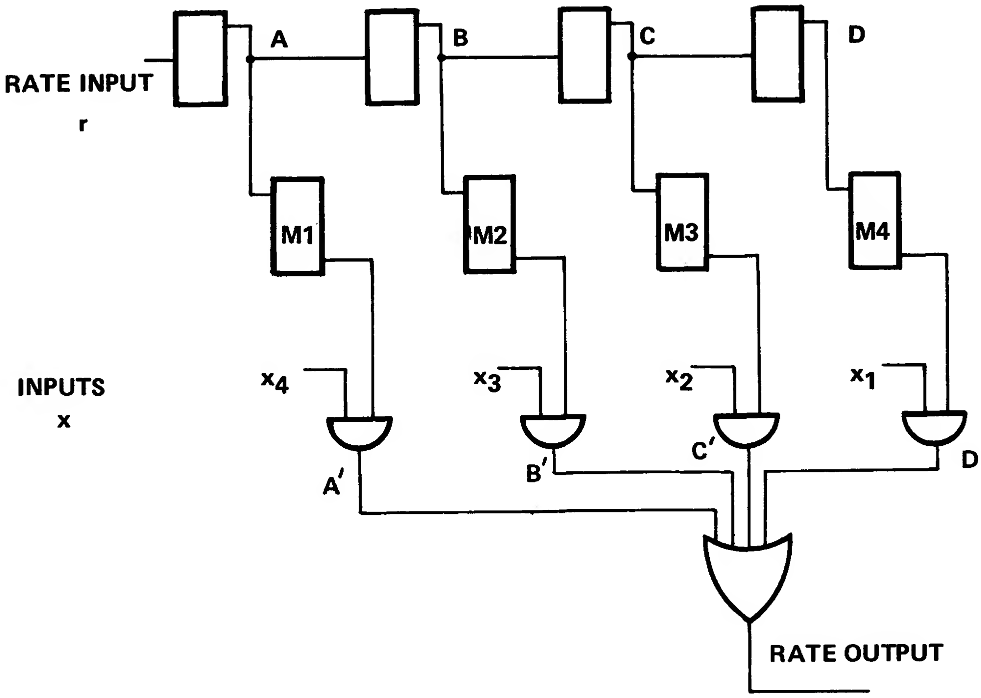


FIGURE 1. Basic Circuit of a Rate Multiplier.

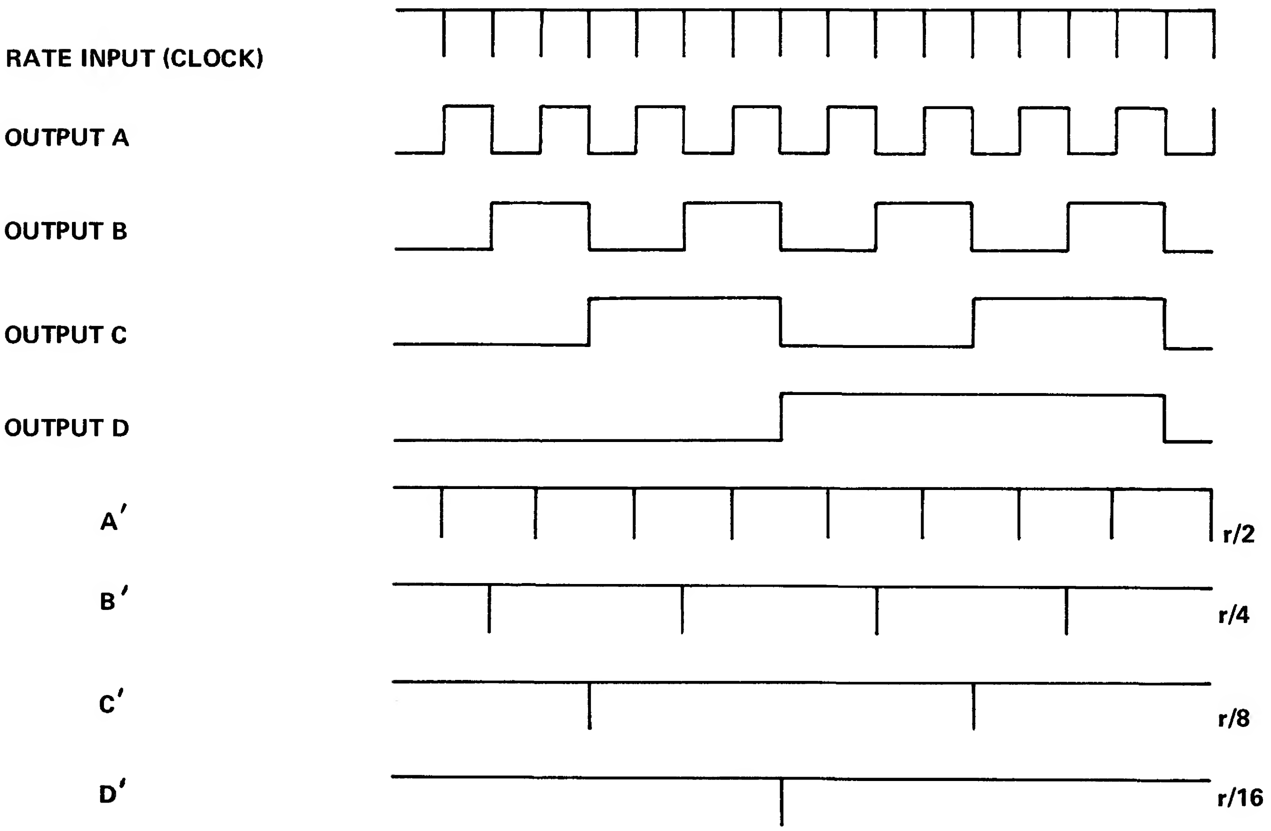


FIGURE 2. Rate Multiplier Operating Waveforms.

that seriously limit the maximum input frequency for any multiplier of reasonable length. The output pulses being of fixed duration, must be the minimum width concurrent with the highest operating frequency. Also, probably the most important point, the pulse differentiators are not easily constructed using m.s.i. t.t.l. techniques.

The logic diagrams of Figure 4 show the internal arrangement of both the SN7497 binary rate multiplier and the SN74167 decimal rate multiplier. The circuit configurations adopted are such that the disadvantages outlined above had been eliminated.

Device Implementation

In the binary rate multiplier the counter section consists of six synchronously clocked J.K. master slave bistables. There is an internal inverting clock buffer. The binary count sequence is controlled by the parallel enable logic associated with each bistable. This also allows an external enable signal to inhibit the counter. There is an internal inverting enable buffer. The all '1's or carry state is detected by a seven input NAND gate. The seventh input being used in conjunction with the external enable signal. This facility allows several b.r.m.s to be cascaded whilst maintaining a fully synchronous count. The required pulse differentiation is performed logically by detecting counter states, i.e. the following gate functions are generated:

$A' = (\text{Clock}).\bar{A}$	giving	32	pulses	per	counter	cycle
$B' = (\text{Clock}).A.\bar{B}.$	"	16	"	"	"	"
$C' = (\text{Clock}).A.B.\bar{C}.$	"	8	"	"	"	"
$D' = (\text{Clock}).A.B.C.\bar{D}.$	"	4	"	"	"	"
$E' = (\text{Clock}).A.B.C.D.\bar{E}.$	"	2	"	"	"	"
$F' = (\text{Clock}).A.B.C.D.E.\bar{F}.$	"	1	"	"	"	"

These functions are gated with the multiplier bits x_n and then ORed to produce the rate output. Note, the most significant bit (m.s.b.) of the multiplier x is gated with A and the lowest significant bit (l.s.b.) with F. A to F inclusive are also gated by a strobe input which defines the output pulse timing and removes any spurious outputs due to differential propagation delays. The output waveforms of the SN7497 for various multiplication rates are shown in the Appendix I. It should be noted that the output pulses

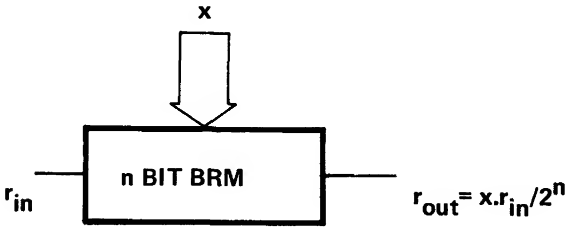
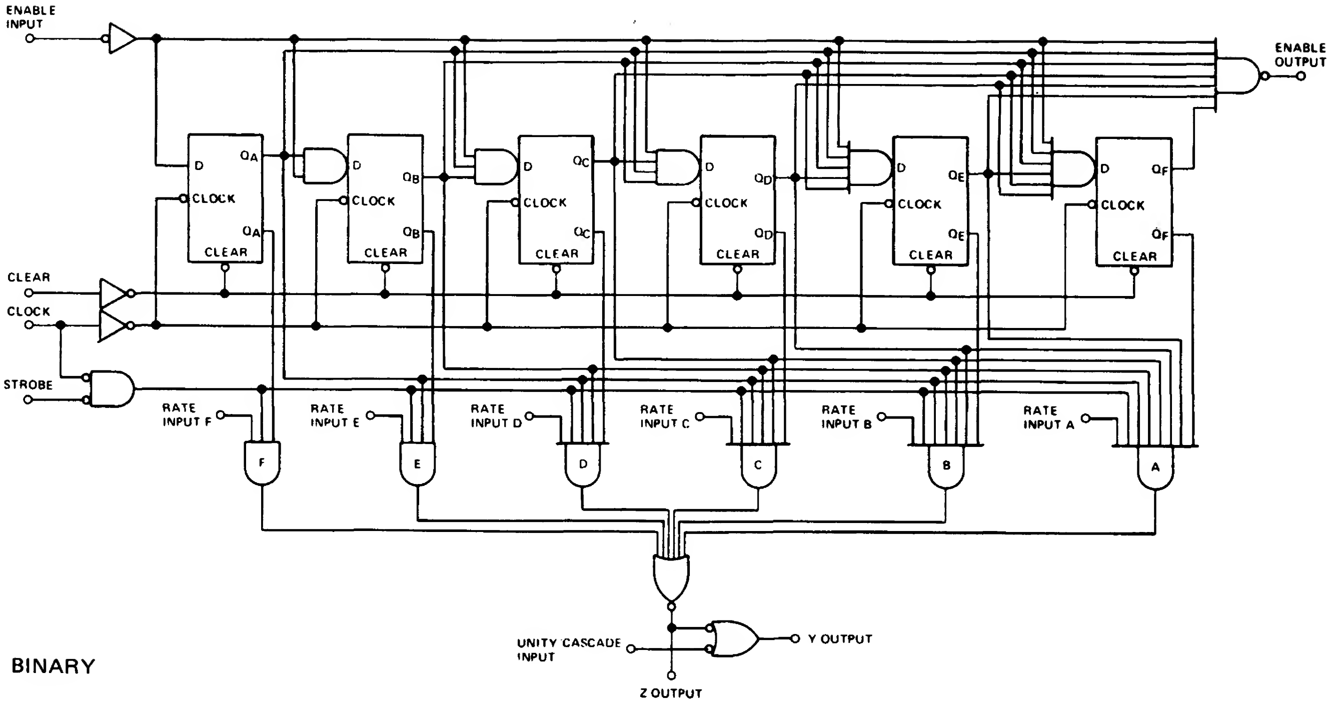
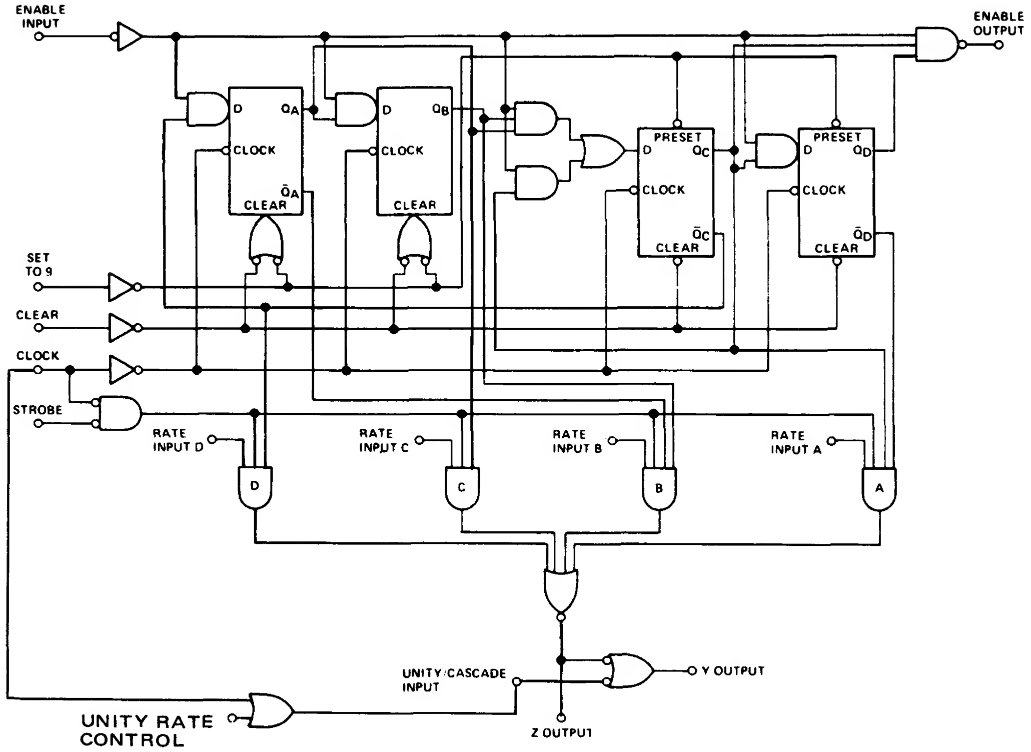


FIGURE 3. Diagrammatic Representation.


ENABLE INPUT
ENABLE OUTPUT
D
CLOCK
CLEAR
QA
QB
QC
QD
QE
QF
CLEAR
CLOCK
STROBE
RATE INPUT F
RATE INPUT E
RATE INPUT D
RATE INPUT C
RATE INPUT B
RATE INPUT A
F
E
D
C
B
A
UNITY CASCADE INPUT
Y OUTPUT
Z OUTPUT

BINARY


ENABLE INPUT
ENABLE OUTPUT
D
CLOCK
CLEAR
PRESET
QA
QB
QC
QD
SET TO 9
CLEAR
CLOCK
STROBE
RATE INPUT D
RATE INPUT C
RATE INPUT B
RATE INPUT A
D
C
B
A
UNITY CASCADE INPUT
Y OUTPUT
Z OUTPUT
UNITY RATE CONTROL

DECIMAL

FIGURE 4. Rate Multiplier Internal Logic Diagrams.

are synchronised with the clock input, the rate multiplier gating only allowing certain of the clock pulses through to the output. Although the output frequency in the long term is the correct multiple of the input rate there is a certain amount of jitter from pulse to pulse. This effect is reduced if the output rate is fed into a counter to integrate out the jitter, the longer the counter the better the integration. (Alternatively the short term randomness can be used to advantage as it is in machine tool control.) Two rate outputs are provided, output and $\overline{\text{output}}$; the inversion being carried out by a 2 input NAND gate functioning as an OR gate for '0's. The other input is used as an OR input when two or more b.r.m.s are cascaded. The maximum output p.r.f. is $(2^n-1)/2^n$ i.e. 63/64 times the input p.r.f. If required, the output frequency can be made the same as the input clock frequency by gating it into the unity/cascade input as shown in Figure 4. There is a common buffered clear operating on a logical '1' level. This is useful for setting initial conditions when the b.r.m. is used as part of an integrator loop.

The decimal rate multiplier works on the same principle but has a four bit b.c.d. counter instead of a six bit binary counter.

Cascading

There are two modes of operation in which devices may be cascaded:

a) Combination of two or more b.r.m.s to produce an m bit b.r.m. When cascaded to perform 12 bit rate multiplication the enable output is connected to the enable input and strobe of the next stage. Output of one stage is connected to the unity/cascade input of the other, the submultiple p.r.f. being taken from the associated output or outputs as shown in Figure 5. If the multiplier, x, contains more than 12 bits then any number of rate multipliers may be cascaded by feeding the pulse output from each group into a multi input NAND gate functioning as an OR gate for '0's as shown dotted in Figure 5.

b) B.r.m.s connected to form serial rate multiplication. In many systems serial rate multiplication of two or more variables is required, this is achieved as shown in Figure 6. The clock input to the second b.r.m. is derived from output of the first b.r.m. In systems where a reversible counter is to be driven all strobe inputs should be gated by the first clock. This ensures that the output pulse width from the final b.r.m. is determined by the clock width into the first stage and not by the time intervals between edges of the rate output from the previous unit.

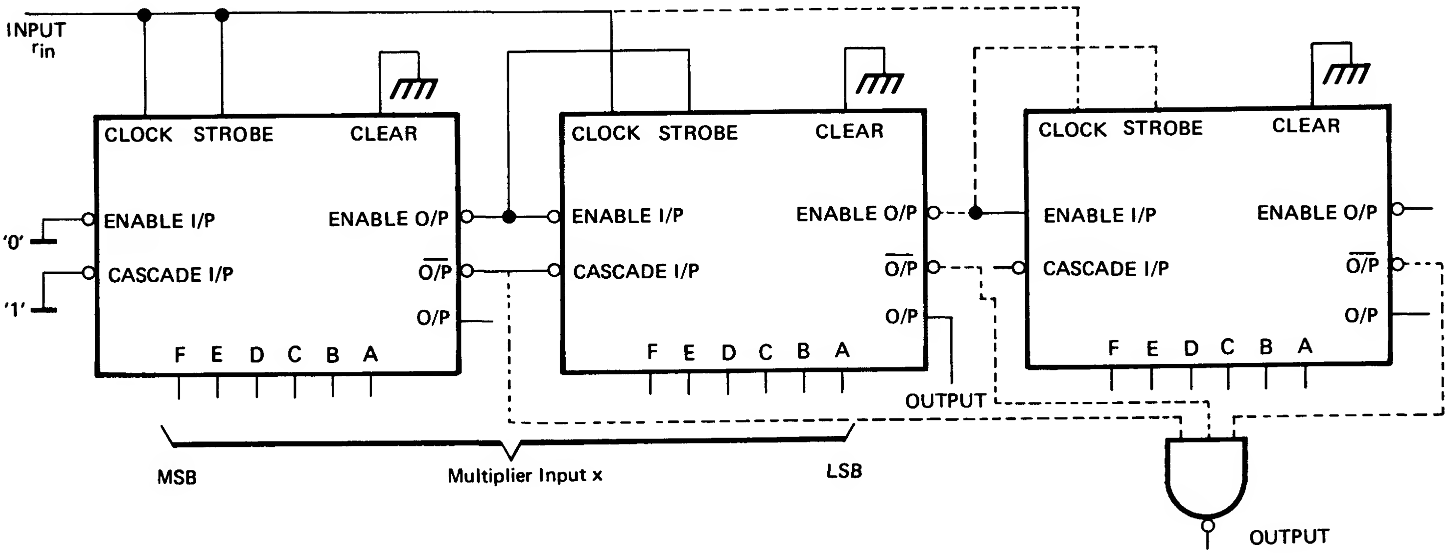

INPUT r_{in}
CLOCK STROBE CLEAR
ENABLE I/P
ENABLE O/P
CASCADE I/P
$\overline{O/P}$
O/P
F E D C B A
'0'
'1'
OUTPUT
MSB
Multiplier Input x
LSB
OUTPUT

FIGURE 5. SN7497 B.R.M.s Cascaded to Form a 12 Bit Multiplier.

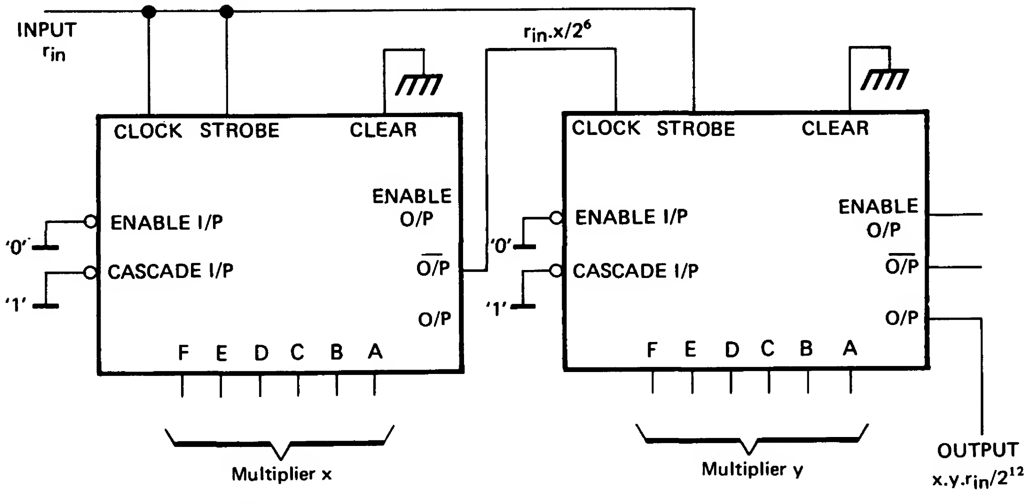

INPUT r_{in}
$r_{in}.x/2^6$
CLOCK STROBE CLEAR
ENABLE I/P
ENABLE O/P
CASCADE I/P
$\overline{O/P}$
O/P
F E D C B A
'0'
'1'
Multiplier x
Multiplier y
OUTPUT $x.y.r_{in}/2^{12}$

FIGURE 6. SN7497 Connected to Perform Rate Multiplication of Two Variables.

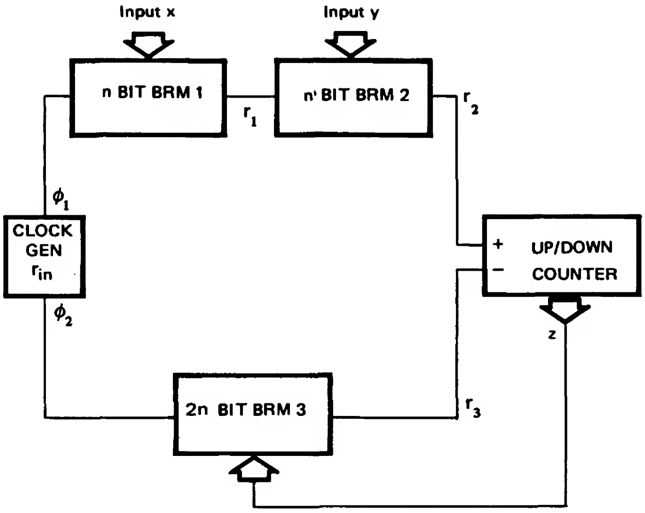


FIGURE 7. B.R.M. Product Generator.

ARITHMETIC OPERATIONS

Arithmetic operations are usually carried out using the b.r.m. as part of a pulse rate feedback loop. Contained in the loop is an up/down counter operating as a null detector, the output of which finally settles to the required value.

Multiplication

Both multiplication and division are very easily carried out using b.r.m.s. The method used is shown in Figure 7. The two numbers x and y, whose product is required, feed the parallel inputs of b.r.m.s 1 and 2. If the input p.r.f. to the first. b.r.m. is r_{in}, its average pulse rate output will be:

$$r_1 = r_{in}.x/2^n$$

similarly the rate output of b.r.m. 2 will be:

$$r_2 = (r_{in}.x/2^n).(y/2^n)$$

The rate output r_2 of b.r.m. 2 is fed into the 'up' input of a reversible counter. The 'down' input of the counter is driven from the rate output of b.r.m. 3 whose parallel multiplier input is the output of the reversible counter. This counter acts as a null detector whose output, z, changes until its two rate inputs r_2 and r_3 are equal. Then:

$$r_3 = r_{in}.z/2^{2n}, \quad r_2 = r_{in}.x.y/2^{2n} \quad \text{and } r_2 = r_3$$

$$\therefore \; = r_{in}.z/2^{2n} = r_{in}.x.y/2^{2n}$$

i.e. $z = x.y$

The rate inputs to b.r.m.s 1 and 3 should be derived from a two phase clock source. This ensures that pulses are not present at both inputs of the 'up-down' counter simultaneously.

In the system described above the reversible counter receives alternate 'up' and 'down' pulses as its output approaches the product x.y. This causes an oscillatory error in the output z. This can be removed by inserting a digital low-pass filter between the outputs of the b.r.m.s and the reversible counter. Such a filter could consist of the circuit shown in Figure 8. This circuit requires two or more consecutive pulses on the r_1 or r_2 input in order to produce an output r_3 or r_4. The circuit operation is as follows:

The first r_1 pulse clears bistable B and clocks bistable A so that output A is at a logical 1, enabling NAND gate G1. Further r_1 pulses are routed through G1 unless bistable A is reset by an r_2 pulse. The r_2 channel operates in a similar manner. The waveforms associated with Figure 8 are shown in Figure 9.

Division

Division is carried out in a similar way to multiplication and is shown in Figure 10.

Pulse rates r_1, r_2 and r_3 are:

$$r_1 = r_{in}x/2^{2n}, r_2 = r_{in}.y/2^n$$

$$r_3 = r_{in}.y.z/2^{2n}$$

When the system has reached equilibrium $r_1 = r_3$

$$\therefore r_{in}.x/2^{2n} = r_{in}.y.z/2^{2n}$$

i.e. $z = x/y$

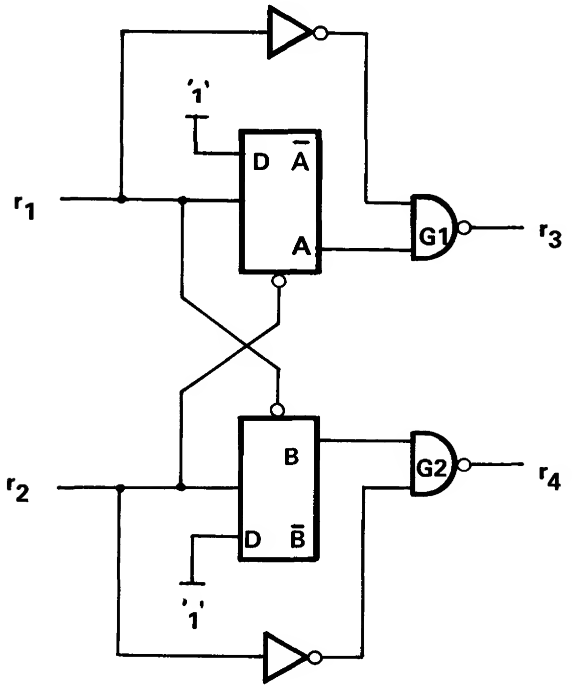


FIGURE 8. Digital Filter.

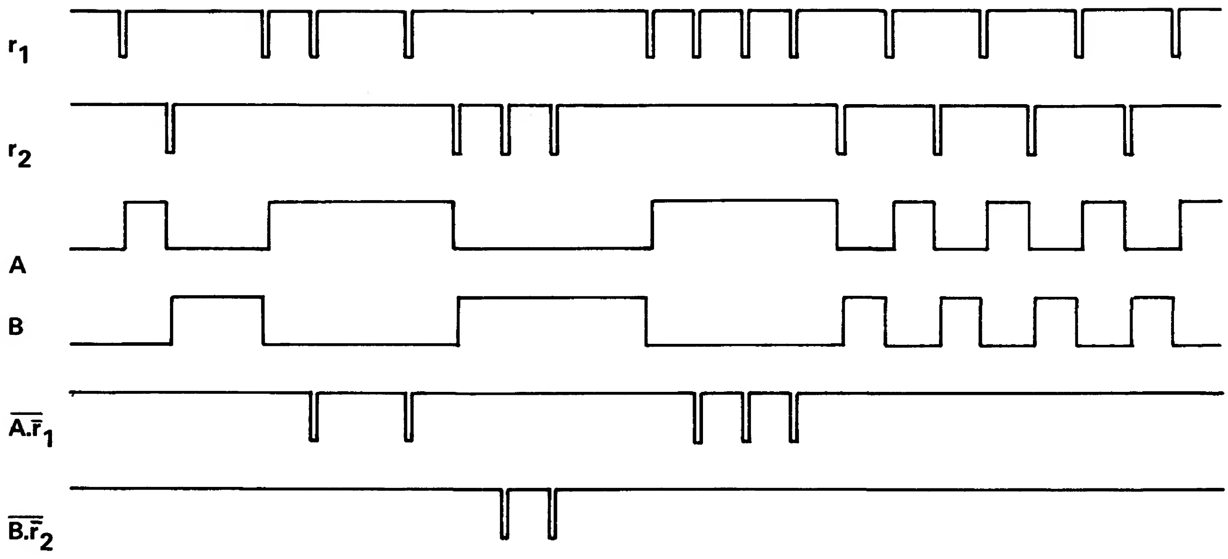

r1
r2
A
B
A.r̄1
B.r̄2

FIGURE 9. Digital Filter Waveforms.

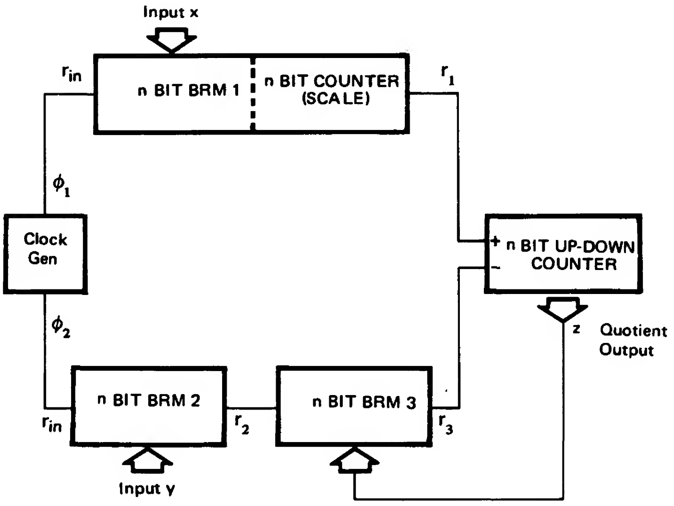

Input x
rin
n BIT BRM 1
n BIT COUNTER (SCALE)
r1
φ1
Clock Gen
φ2
+ n BIT UP-DOWN
– COUNTER
z
Quotient Output
n BIT BRM 2
rin
Input y
r2
n BIT BRM 3
r3

FIGURE 10. B.R.M. Quotient Generator.

Combined Multiplication and Division

Multiplication and division can be carried out simultaneously as shown in Figure 11. In order to obtain a stable system the number of division stages from the clock input to both inputs of the 'up-down' counter must be the same. This requires an additional scaling counter in the upper signal path of the system shown.

At equilibrium $r_1 = r_2$

$$r_1 = r_{in}(x/2^n).(y/2^n).(1/2^{2n})$$

$$r_2 = r_{in}.(w/2^n).(v/2^n).(z/2^{2n})$$

$$\therefore\ z = x.y/w.v.$$

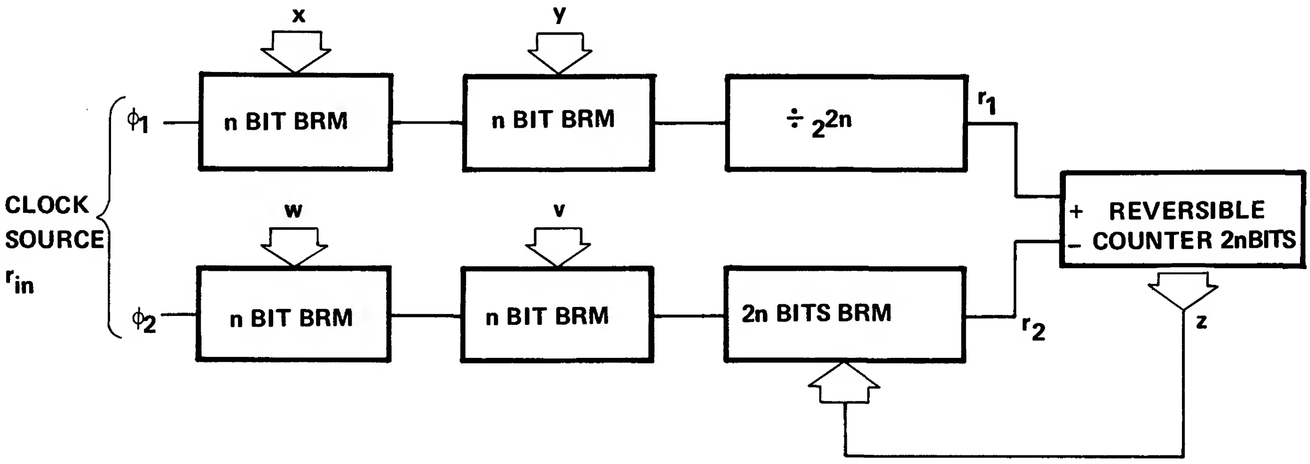

x
y
φ1
n BIT BRM
n BIT BRM
÷ 2^2n
r1
CLOCK SOURCE
rin
w
v
+ REVERSIBLE
– COUNTER 2nBITS
φ2
n BIT BRM
n BIT BRM
2n BITS BRM
r2
z

FIGURE 11. Simultaneous Multiplication and Division.

Addition and Subtraction

These functions are carried out by using an OR gate to sum the rate outputs of two or more b.r.m.s as shown in Figure 12.

$$r_3 = r_1 + r_2 \qquad r_4 = r_{in}.z/2^n$$

$$\therefore r_3 = (r_{in}.x/2^n) + (r_{in}.y/2^n)$$

$$= r_{in}.(x + y)/2^n$$

At equilibrium $r_3 = r_4$

$$\text{i.e. } r_{in}.(x + y)/2^n = r_{in}.z/2^n$$

$$\therefore \qquad z = x + y$$

Subtraction is identical to addition except that the OR gate is placed in the signal path to the down input of the reversible counter.

Combined Addition and Subtraction

The arrangement for simultaneous addition and subtraction is shown in Figure 13.

$$r_3 = r_1 + r_2$$

$$r_6 = r_4 + r_5$$

At equilibrium $r_3 = r_6$

$$\therefore r_1 + r_2 = r_4 + r_5$$

$$\therefore z = x + y - v$$

Square Roots

The circuit diagram for generating square roots (Figure 14) illustrates the basic method for fractional indices.

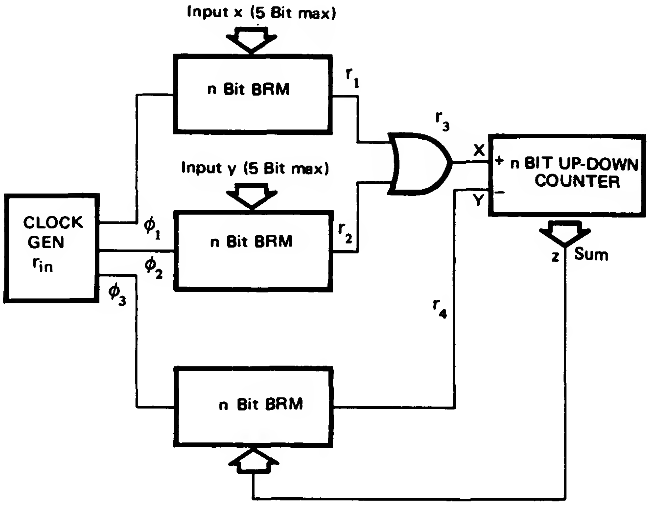

Input x (5 Bit max)
n Bit BRM
r_1
r_3
X
+ n BIT UP-DOWN COUNTER
Y
-
Input y (5 Bit max)
CLOCK GEN r_{in}
ϕ_1
ϕ_2
ϕ_3
n Bit BRM
r_2
z
Sum
r_4
n Bit BRM

FIGURE 12. Adder.

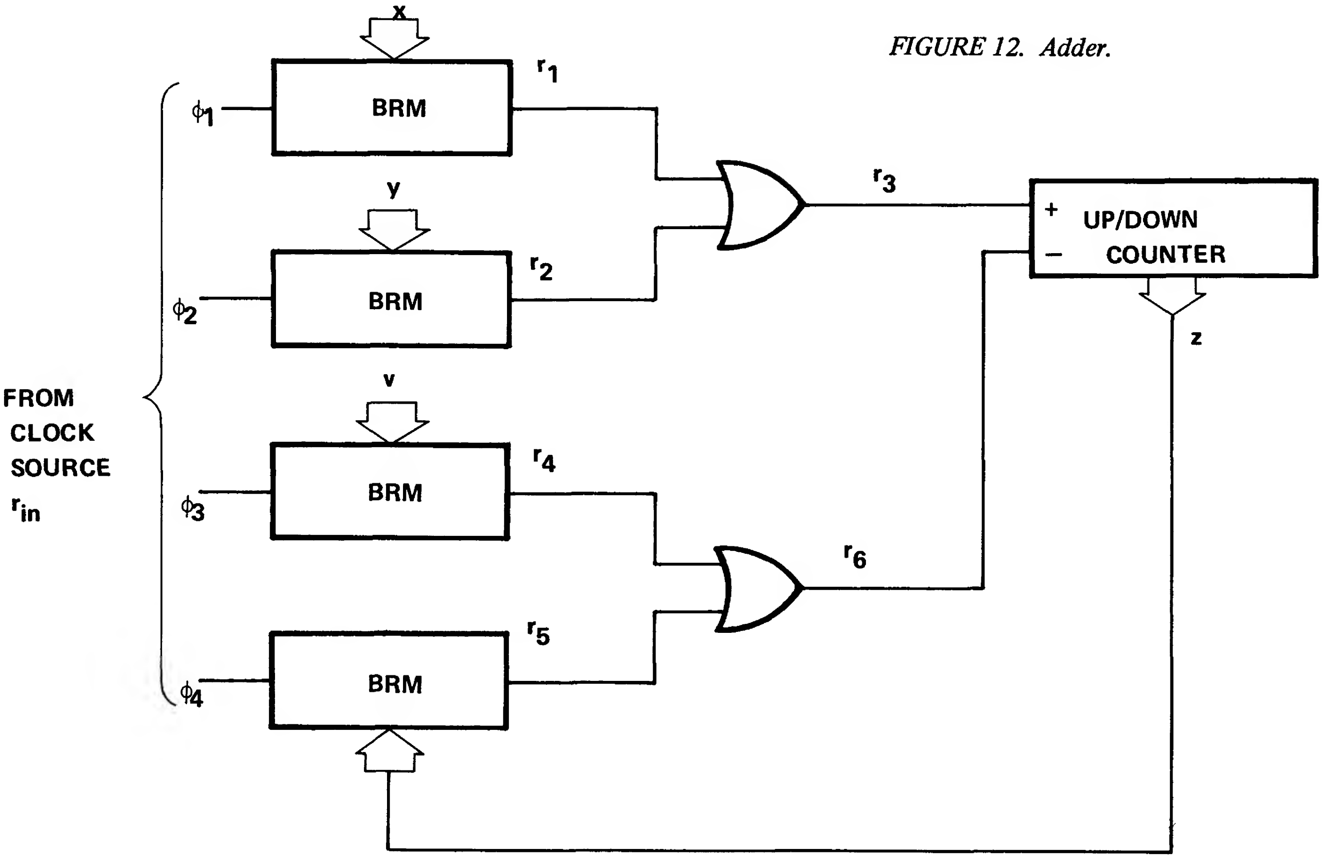

x
BRM
r_1
ϕ_1
y
BRM
r_2
ϕ_2
r_3
+ UP/DOWN
– COUNTER
z
v
FROM CLOCK SOURCE r_{in}
BRM
r_4
ϕ_3
r_6
r_5
BRM
ϕ_4

FIGURE 13. Simultaneous Addition and Subtraction.

$$r_1 = r_{in}.x/2^{2n}, \quad r_2 = r_{in}.z^2/2^{2n}$$

At equilibrium $r_1 = r_2$

$$\text{i.e. } z^2 = x$$

$$z = x^{½}$$

Non Integer Roots

The above method can be extended to cover more complex roots of the form $x^{a/b}$. As an example, the arrangement to obtain $x^{2/3}$ is shown in Figure 15.

$$r_1 = r_{in}.x^2/2^{3n}, \quad r_2 = r_{in}.z^3/2^{3n}$$

At equilibrium space $r_1 = r_2$

$$\therefore z = x^{2/3}$$

When several functions are combined, variables can in many cases be represented by pulse rates. This is shown in Figure 16 where $z = (x^2 + y^2)^{½}$

$$r_1 = (r_{in}.x^2/2^{2n}) + (r_{in}.y^2/2^{2n}), r_2 = r_{in}.z^2/2^{2n}$$

At equilibrium

$$r_{in}.z^2/2^{2n} = (r_{in}.x^2/2^{2n}) + (r_{in}.y^2/2^{2n})$$

$$\therefore z = (x^2 + y^2)^{½}$$

The system shown in Figure 16 can, with slight modification be used. to solve equations of the form $x^2 + y^2 = z^2$. Hence it is possible to generate the cartesian coordinates of any point on a circle as shown in Figure 17. For display purposes this is not the ideal method of circle generation, since the locus of the point (x,y) does not move with constant angular velocity. (As given later a better solution to this problem is to solve the parametric equations $y = R \cos \theta$; $x = R \sin \theta$ where R is the radius.)

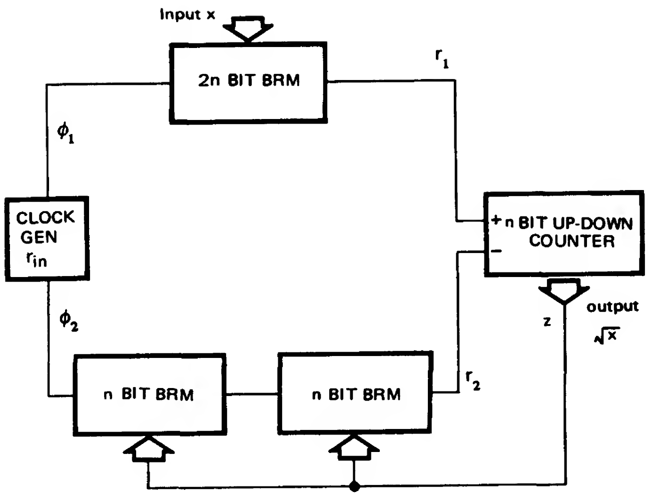

Input x
2n BIT BRM
r_1
ϕ_1
CLOCK GEN r_{in}
+ n BIT UP-DOWN COUNTER
−
output
z
$\sqrt{x}$
ϕ_2
n BIT BRM
n BIT BRM
r_2

FIGURE 14. Generation of $x^{½}$.

At equilibrium $r_1 = r_2$

$$(r_{in}.x^2/2^{2n}) + (r_{in}.y^2/2^{2n}) = (r_{in}.R^2/2^{2n})$$

$$\therefore x^2 + y^2 = R^2$$

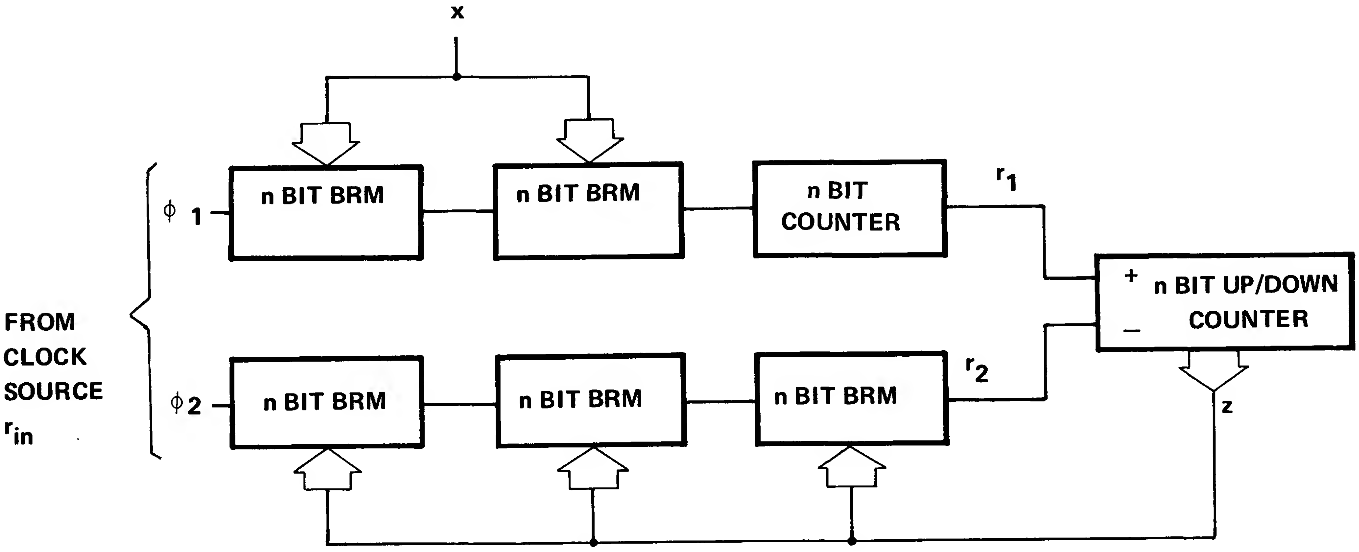

x
n BIT BRM
n BIT BRM
n BIT COUNTER
r_1
ϕ 1
FROM CLOCK SOURCE r_{in}
+ n BIT UP/DOWN COUNTER
−
ϕ 2
n BIT BRM
n BIT BRM
n BIT BRM
r_2
z

FIGURE 15. Generation of Non Integer Roots.

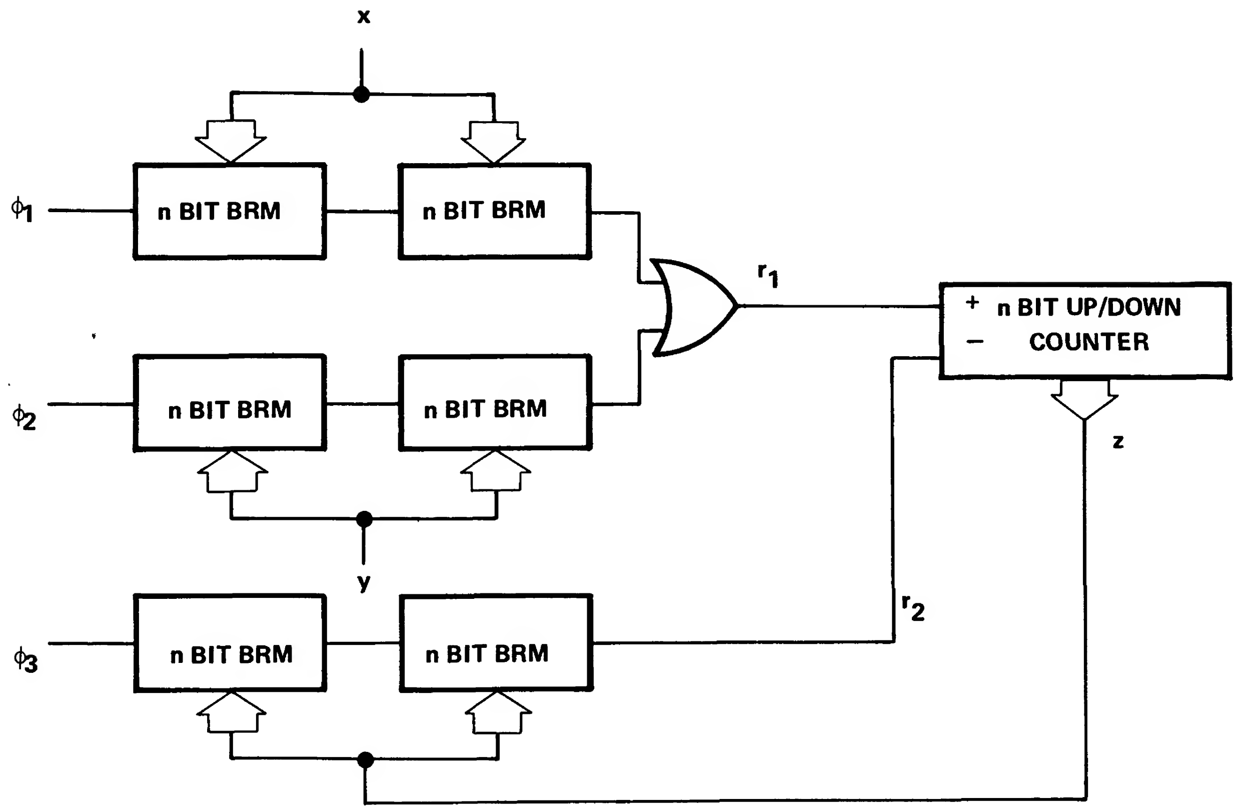

x
φ1
n BIT BRM
n BIT BRM
r1
+ n BIT UP/DOWN
– COUNTER
φ2
n BIT BRM
n BIT BRM
z
y
r2
φ3
n BIT BRM
n BIT BRM

FIGURE 16. Generation of Combined Functions $z = (x^2 + y^2)^{1/2}$.

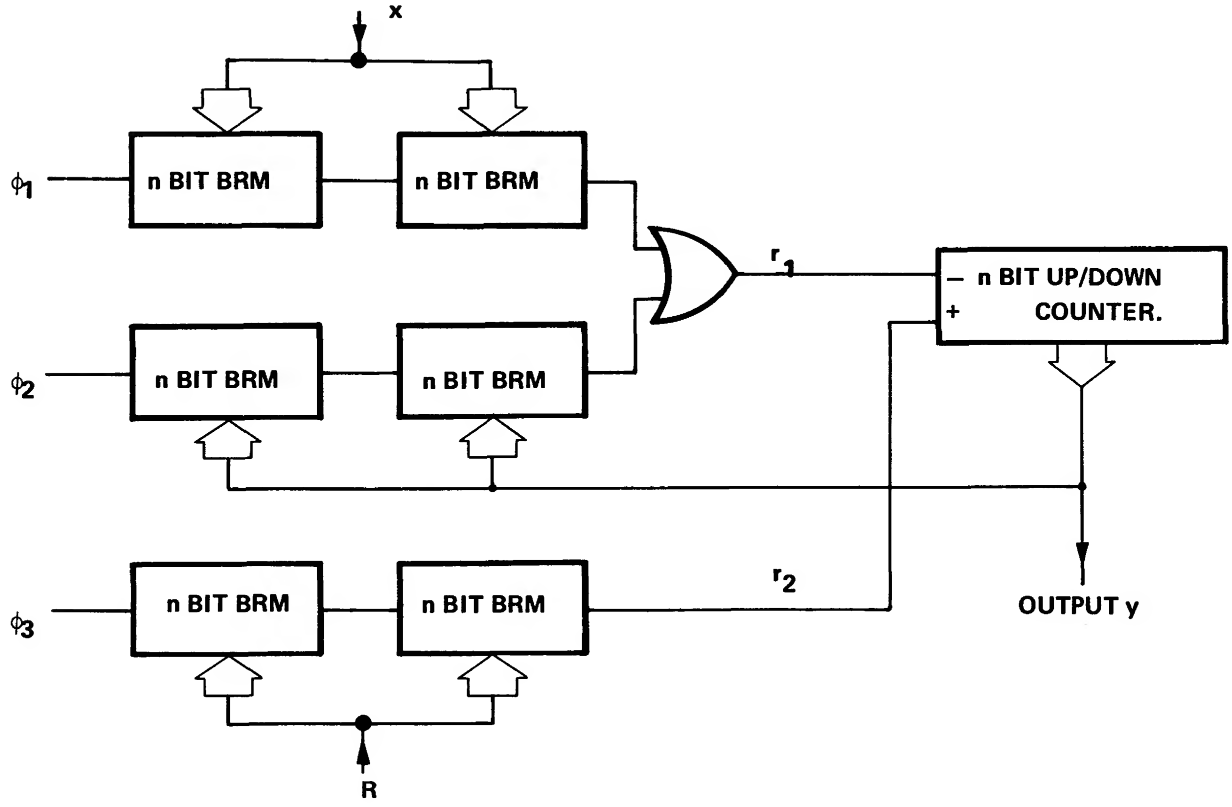

x
φ1
n BIT BRM
n BIT BRM
r1
– n BIT UP/DOWN
+ COUNTER.
φ2
n BIT BRM
n BIT BRM
φ3
n BIT BRM
n BIT BRM
r2
OUTPUT y
R

FIGURE 17. Generation of Combined Function $x^2+y^2 = R^2$.

Frequency Ratio

The block diagram of a system for determining the ratio of two frequencies is shown in Figure 18. Such a system could form the basis of a continuously reading frequency meter.

$r_1 = f_1/2^n$

$r_2 = f_2.y/2^n$

At equilibrium $r_1 = r_2$

$\therefore y = f_1/f_2$ where

$63f_2 \geqslant f_1 \geqslant f_2$ if a 2^n scaler is used.

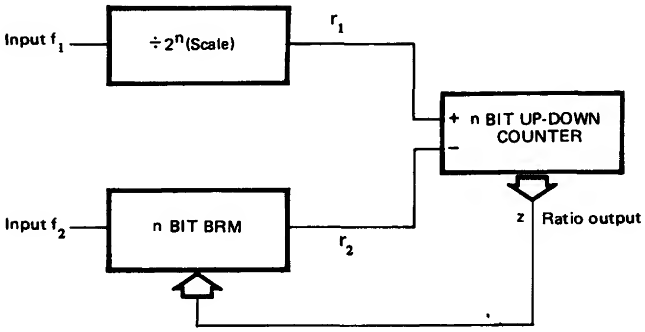


FIGURE 18. Frequency Ratio.

Input pulses to the up/down counter should not be coincident. f_1 and f_2 are asynchronous and should be retimed to a two phase clock. A suitable circuit is shown in Figure 19. The two phase clock frequency should be at least four times the highest input frequency.

MATHEMATICAL OPERATIONS

Integration

Integration is performed by counters. If the input to a counter is a pulse train, then each pulse can be considered to represent an amount Δx. Over a time, t, the counter will then accumulate $\Sigma_0^t \Delta x$. If the counter is large so that Δx represents only a small fraction of the total counter contents then $\Delta x \rightarrow dx$ and the counter accumulates $\int_0^t dx$. If the input is considered to be a pulse rate f(t) pulses/unit time then the counter contents represent $\int_0^t f(t)\, dt$. The counter can only operate as an integrator if the input is in pulse form, it cannot accumulate increments of more than the least significant bit as is the case with a Digital Differential Analyser integrator. The input variable is usually in the form of a parallel binary number and must be converted to pulse rate form before integration. This is achieved by means of a b.r.m. as shown in Figure 20. The b.r.m. is clocked at constant rate k pulses per second

$r_1 = k.x/2^n$ and $y = k/2^n \int_0^t x.dt.$

This operation forms the basis of a digital integrator. By using a reversible counter $y = \pm(k/2^n)\int_0^t x.dt$ may be computed.

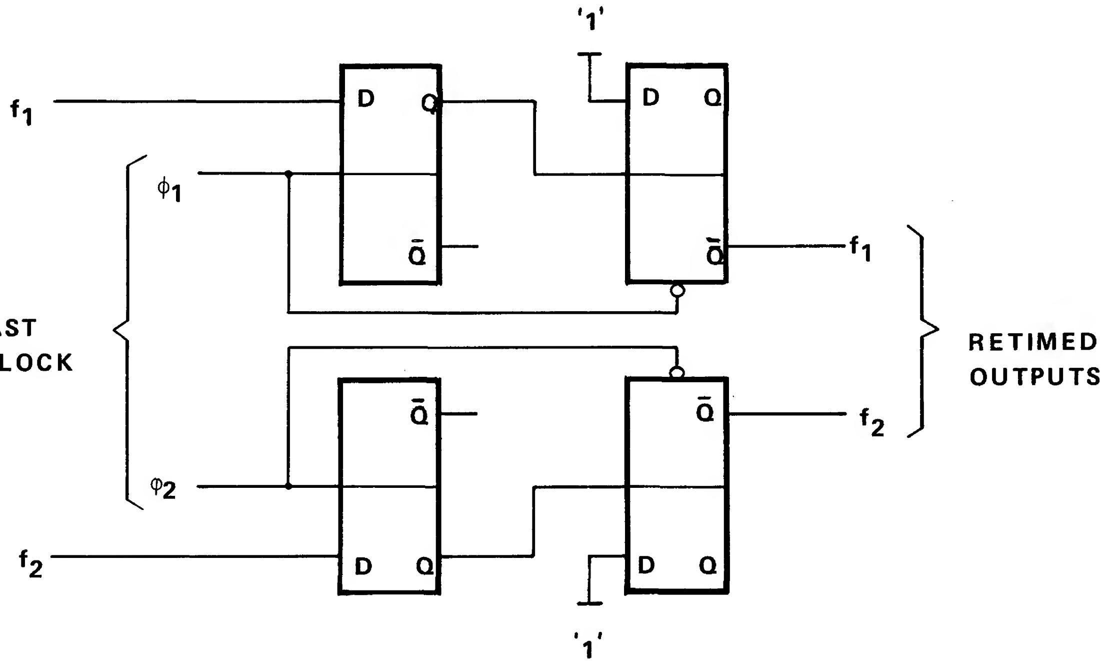


FIGURE 19. Input Pulse Processor.

Use of Integrators

The digital integrator may be used in a similar manner to analogue integrators for solving differential equations and function generation. For example, if in Figure 20 the output y of the counter is taken to the x input of the b.r.m. and initially $x = 1$,

then $x = y$

$$x - 1 = K \int_0^t x.dt, \text{ where } k/2^n = K$$

$$\therefore x = \epsilon^{Kt}$$

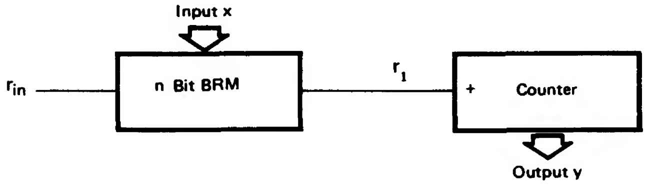


FIGURE 20. Digital Integrator.

By having the counter reversible $x = \epsilon^{\pm Kt}$ can be computed. If the total number of input pulses during the computation time is accumulated in a second counter, then it will contain $\log_\epsilon x.2^n$.

This method of function generation can be extended to trigonometrical functions as shown in Figure 21.

$$y = K \int_0^t x \, dt \qquad x = -K \int_0^t y \, dt$$
$$\dot{y} = K x \qquad \dot{x} = -K y$$
$$x = \dot{y} / K \ldots (1) \qquad y = -\dot{x}/K \ldots (2)$$

Substituting equation (2) into (1) gives

$$x = -\ddot{x} / K^2$$
$$\ddot{x} + K^2 x = 0$$
$$x = A.\epsilon^{jKt} + B.\epsilon^{-jKt}$$

Substituting equation (1) into (2)

$$y = -\ddot{y} / K^2$$
$$\ddot{y} + K^2 y = 0$$
$$y = C.\epsilon^{jKt} + D.\epsilon^{-jKt}$$

If the initial conditions set in the x and y counters are $x = 1$ and $y = 0$, then after a time t

$$y = \sin Kt \qquad \text{and} \qquad x = \cos Kt$$

The x and y counters must be reset after the first quadrant has been generated since, due to the non uniform output pulse rate from the b.r.m.s, x may not be at zero when $y = 1$. If the x counter is replaced by an 'up' counter then $y = \sinh Kt$ and $x = \cosh Kt$ can be generated. Sine and cosine functions may be generated over four quadrants by using

$$\sin (x)_0^{\pi/2} = \sin (x)_0^{\pi/2}$$
$$\sin (x)^{\pi}_{\pi/2} = \cos (x)_0^{\pi/2}$$
$$\sin (x)_{\pi}^{3\pi/2} = -\sin (x)_0^{\pi/2}$$
$$\sin (x)_{3\pi/2}^{3\pi} = -\cos (x)_0^{\pi/2}$$

The change from generating sine x to cos x is achieved by reversing the inputs to the up/down counters.

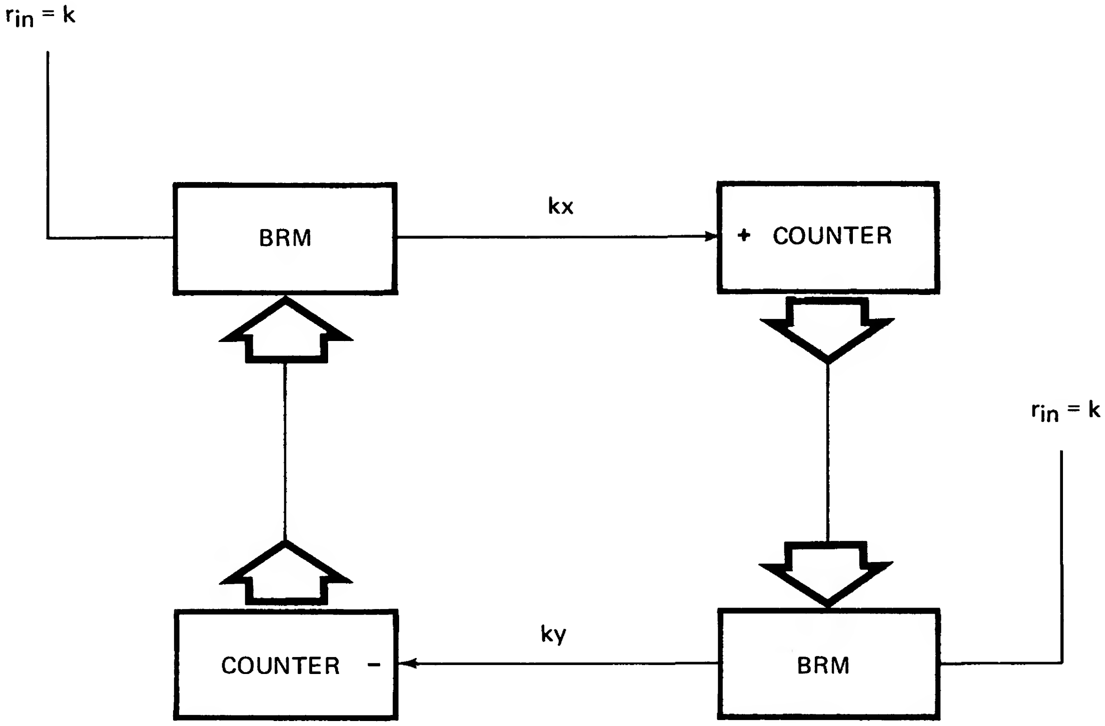


FIGURE 21. Sine and Cosine Generation.

Rotating Vector Generation

The system may be extended further to produce a rotating vector display as used, for example, in radar, Figure 22. The functions required to produce a rotating Plan Position Indicator type of display are:

$$x = R_{(t)} \sin\theta$$

$$y = R_{(t)} \cos\theta$$

where $R_{(t)}$ increases linearly with time, Figure 22.

Outputs z and w are $\sin\theta$ and $\cos\theta$ respectively as in Figure 22. The clock inputs to the two lower multiplier b.r.m.s represent dR/dt.

The outputs of the x and y integrators are therefore:

$$x = K.\sin\theta.\int_0^t dR \qquad y = K.\cos\theta.\int_0^t dR$$

$$x = K.R_{(t)}.\sin\theta \qquad y = K.R_{(t)}.\cos\theta$$

which are the required functions.

If the x integrator is reset to zero when $y = y_{max}$ and the y integrator when $x = x_{max}$ then a rectangular or square display can be generated.

The practical implementation of the above system is shown in Figure 23.

PRACTICAL CONSIDERATIONS

The following comments should be noted with respect to the systems described in this chapter. As previously mentioned the output pulse rate of a b.r.m./d.r.m. is not regular since the n^{th} stage contributes a rate of $2^{-n}.r_{in}$ to the output, and, in general, an irregular pulse sequence results. When the input rate is regular the instantaneous fluctuations in output rate are not large and are reduced considerably if the output rate is integrated. An indication of the possible output waveforms is given in Appendix I.

An integrator would consist of an additional counter acting as a smoothing element. If the period of the input rate to the counter is (t ±Δ t) where t is the average period and Δt is the possible time duration of any pulse, then the frequency

$$f_{in} = 1/t(1 \pm \Delta t/t) = (1 \pm \Delta t/t)/t$$

If the integration counter divides by z then the period of the rate out of the counter is (zt ± Δt) and the frequency

$$f_{out} = 1/zt(1 \pm \Delta t/zt) = (1 \pm \Delta t/tz)/zt.$$

Thus the output rate of the counter is proportional to the input rate with a scaling factor of 1/z, but the percentage of frequency jitter is also reduced by a factor of 1/z.

In the examples on mathematical integration it has always been assumed that integration has been carried out

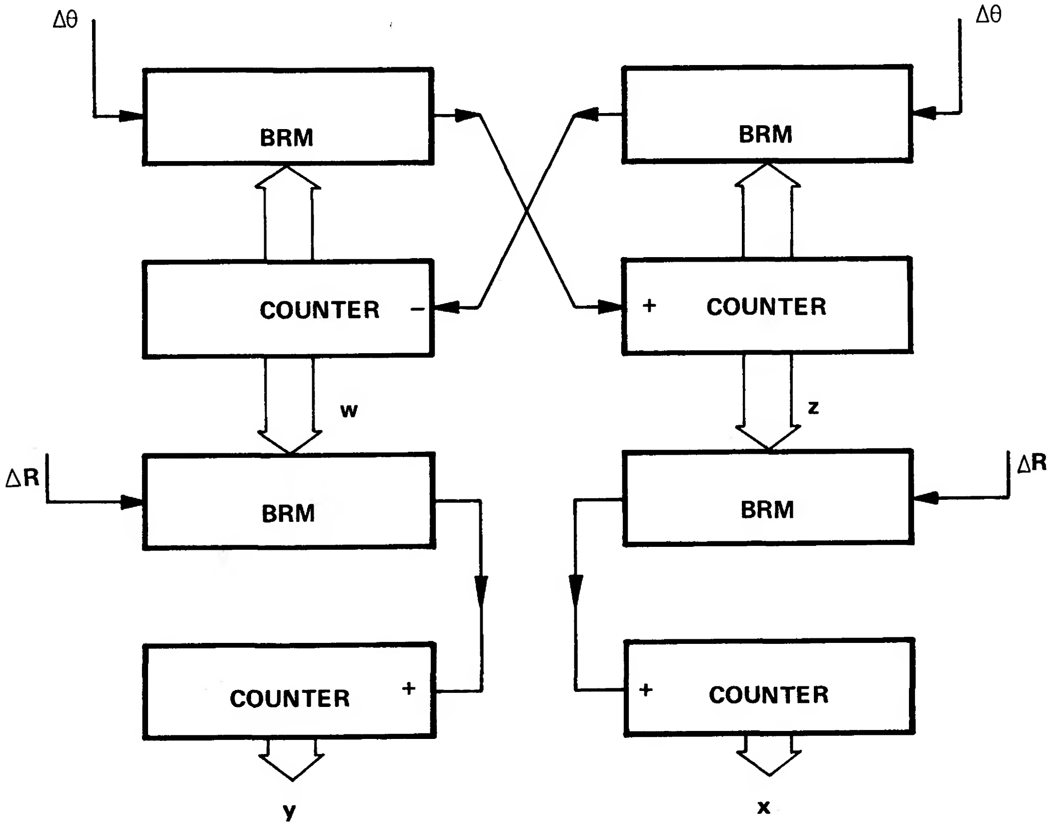


FIGURE 22. Vector Generation.

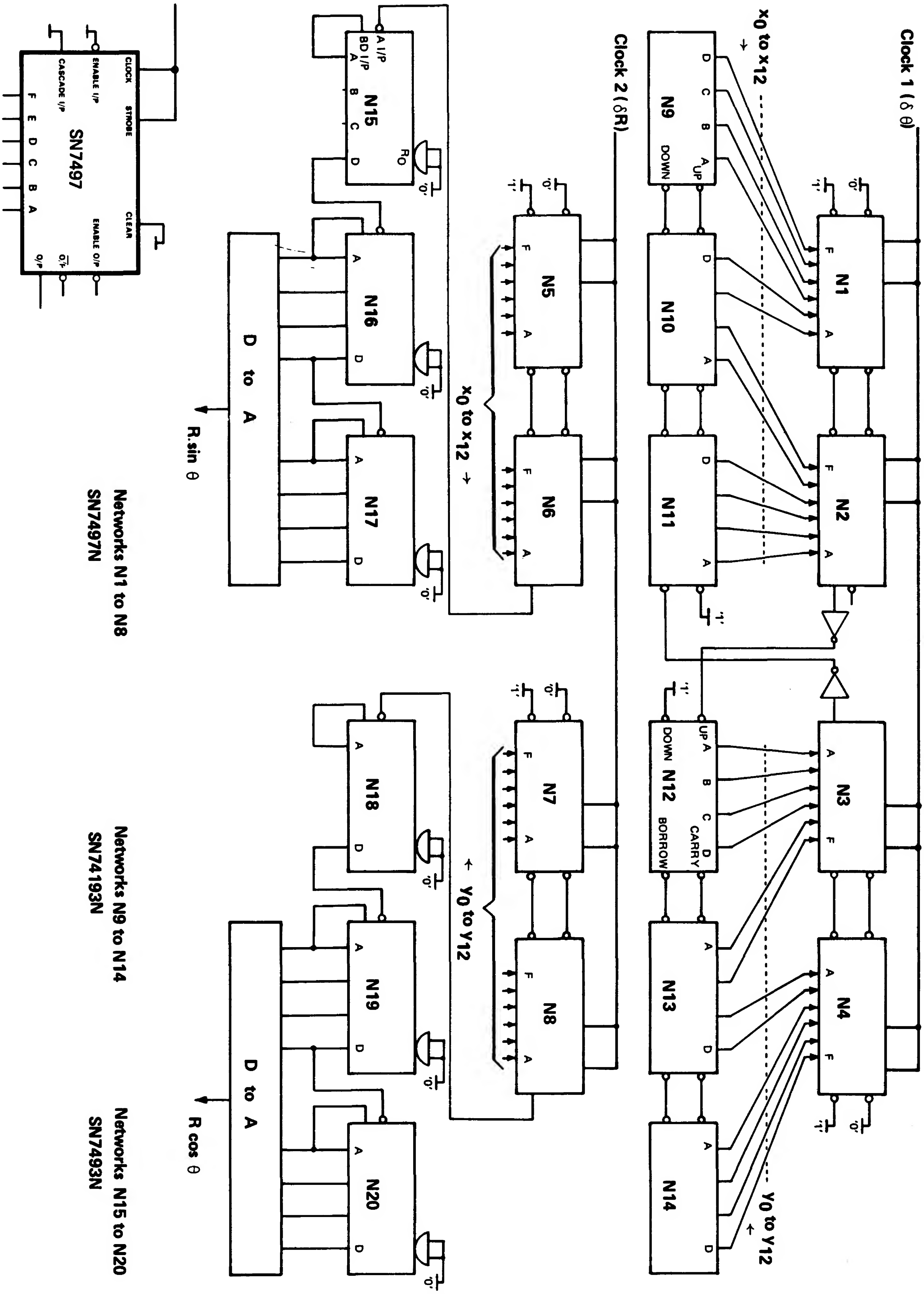

Clock 1 (δθ)
Clock 2 (δR)
x0 to x12
Y0 to Y12
x0 to x12
Y0 to Y12
N1
N2
N3
N4
N5
N6
N7
N8
N9
N10
N11
N12
N13
N14
N15
N16
N17
N18
N19
N20
UP
DOWN
CARRY
BORROW
A I/P
BD I/P
R0
A
B
C
D
F
'0'
'1'
D to A
D to A
R.sin θ
R cos θ
SN7497
CLOCK
STROBE
CLEAR
ENABLE I/P
ENABLE O/P
CASCADE I/P
O/P
F E D C B A
Networks N1 to N8
SN7497N
Networks N9 to N14
SN74193N
Networks N15 to N20
SN7493N

FIGURE 23. Practical Rotating Vector Generation.

with respect to (w.r.t.) time, t,–this is a generalisation. Integration may be carried out w.r.t. any variable. If the input pulses δx, say, to the b.r.m. which feeds the integrator counter are accumulated in another counter, then the contents of this second counter give the value of x at any time. By inspecting the contents of this second counter the integration may be terminated at any value of x. The input pulse rate dx/dt can itself be a function of time thus enabling integration to be carried out w.r.t. any variable.

So far no mention has been made of the time required for a system to settle to the final solution. A method is outlined below which does, however, assume that fluctuations in signal rates occur over a large number of input pulses. This enables standard calculus to be used. The example chosen is the frequency ratio meter described earlier and shown in Figure 18. By converting this figure to a signal flow diagram, setting up the relevant equations and obtaining their general solution, as shown in Appendix II, the time constant for the output to reach its final value is obtained. Negative numbers may be represented by a sign bit followed by the 'two's complement' notation. This adds, sometimes considerable, complexity to a system since controlled complementers are required. However, with m.s.i. devices this requires only one or two additional packages. Alternatively the problem may be approached in a different manner by suitably scaling the input variables.

REFERENCES

1. Wood, P. *Frequency meter with continuous digital presentation.* J. Brit. Instn. Radio Engineers, 26 No. 2, p.109-113, August 1963.

2. Martin, J. D. *Signal Processing and Computation using pulse rate techniques.* The Radio and Electronic Engineer, 38 No. 6, p.329-334, December 1969.

3. Lundh, Y. *Digital techniques for small computations.* J. Brit. Instn. Radio Engineers, 9, No. 1, p.439-449, January 1959.

4. Yang, H.Z. *Determination of maximum error of a binary multiplier.* Automation and Remote Control, 21 No. 7, p.709-713, 1961.

N.B. Reference 2 contains an excellent list of further references.

APPENDIX I

The diagram in this appendix is designed to show the sequences of pulses that are produced by a b.r.m. for various rate input settings. The state of the counter determines the production of output pulses. The clear facility can therefore be useful in ensuring that the same sequence is always produced and that the same number of output pulses are produced for a given number of clock input pulses.

MSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
Internal Counter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
of Rate Multiplier	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
LSB	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Rate Inputs F E D C B A																																									
000000																																									
000001																																I									
000010																I																									
000011																I																I									
000100								I																I																I	
000101								I																I								I								I	
000110								I								I								I																I	
000111								I								I								I								I								I	
001000				I								I								I								I								I					
001001				I								I								I								I				I				I					
001010				I								I				I				I								I								I					
001011				I								I				I				I								I				I				I					
001100				I				I				I								I				I				I								I				I	
001101				I				I				I								I				I				I				I				I				I	
001110				I				I				I				I				I				I				I								I				I	
001111				I				I				I				I				I				I				I				I				I				I	
010000		I				I				I				I				I				I				I				I				I				I			
010001		I				I				I				I				I				I				I				I		I		I				I			
010010		I				I				I				I		I		I				I				I				I				I				I			
010011		I				I				I				I		I		I				I				I				I		I		I				I			
010100		I				I		I		I				I				I				I		I		I				I				I				I		I	
010101		I				I		I		I				I				I				I		I		I				I		I		I				I		I	
010110		I				I		I		I				I		I		I				I		I		I				I				I				I		I	
010111		I				I		I		I				I		I		I				I		I		I				I		I		I				I		I	
011000		I		I		I				I		I		I				I		I		I				I		I		I				I		I		I			
011001		I		I		I				I		I		I				I		I		I				I		I		I		I		I		I		I			
011010		I		I		I				I		I		I		I		I		I		I				I		I		I				I		I		I			
011011		I		I		I				I		I		I		I		I		I		I				I		I		I		I		I		I		I			
011100		I		I		I		I		I		I		I				I		I		I		I		I		I		I				I		I		I		I	
011101		I		I		I		I		I		I		I				I		I		I		I		I		I		I		I		I		I		I		I	
011110		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I				I		I		I		I	
011111		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I	
100000			I		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I		I		
100001																																									
100010																																									

APPENDIX II

In Figure 18 if one of the input frequencies, f_2, say, is constant then α represents the proportionality constant between z and the rate output, r_2, of the lower b.r.m. Figure 18 can be converted to the signal flow diagram shown in Figure 24.

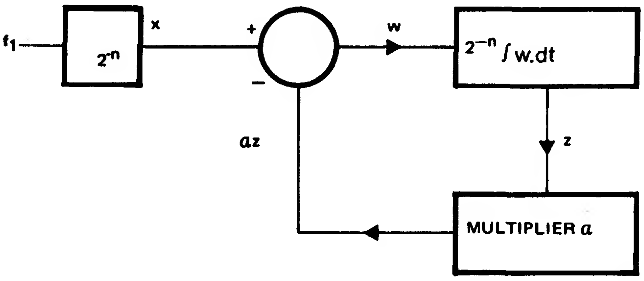


FIGURE 24. Signal Flow Diagram for Frequency Ratio.

From this:

$$w = x - \alpha z$$

$$z = 2^{-n}.\int_0^t w.dt$$

$$= 2^{-n}.\int_0^t (x - \alpha z).dt$$

$$= 2^{-n}.\int_0^t xdt - \alpha.2^{-n}.\int_0^t z.dt$$

$$z = 2^{-n}.\ x.t. - \alpha.2^{-n}.\int_0^t z.dt$$

$$\text{i.e. } dz/dt \doteq 2^{-n}.x - \alpha 2^{-n}.z$$

This differential equation has as a general solution:

$$z = C.\ \epsilon^{(-\alpha 2^{-n}.t)} + x/\alpha$$

when $t = 0 \quad z = 1 \quad \therefore \quad C = -x/\alpha$

$$\therefore z = (1 - \epsilon^{-\alpha 2^{-n}.t}).\ x/\alpha$$

But $x = f_1/2^n$ and $\alpha = f_2.\ 2^{-n}$

$$\therefore z = [1 - \exp(-f_2.\ 2^{-2n}.t)].\ f_1/f_2 \quad \text{..........} \ \text{A}$$

Thus giving a time constant of $1/f_2.2^{-2n}$. From equation A the time taken for the value of z to settle to any accuracy can be determined.

XIV PERIPHERAL CIRCUITS

by

David A. Bonham and Bob Parsons

Some of the circuits which may be used around a typical process control system are described in this chapter. They include keyboard encoders and a circuit for establishing priority such as required, say, for Interrupt. These can be considered as input circuits. The output circuits described are digital to analogue converters and a programmable triangular function generator. The latter will produce an approximate sinewave by the addition of a suitable low pass filter. Several of the circuits discussed have a priority encoder as an important constituent.

PRIORITY ENCODERS

A priority encoder is a device that will encode the highest order input data line into a numerically weighted code, irrespective of all lower order inputs. For example, a b.c.d. encoder, with ten input lines would encode the presence of a logic input on input line five as '0101' i.e. b.c.d. five. This output code is produced even if other inputs lower than five are also present.

Device Description

The SN74147N is a ten line to b.c.d. encoder. The logic diagram and truth table for this device are shown in Figure 1 and Table 1 respectively. There is no input line representing zero. A zero is interpreted as the absence of data on all other data input lines, and is encoded accordingly. All input lines are buffered and are equivalent to a single t.t.l. load.

The SN74148 is a binary version of the '147. It has additional inputs and outputs that are used when devices are cascaded. The logic diagram and truth table for this device are shown in Figure 2 and Table 2.

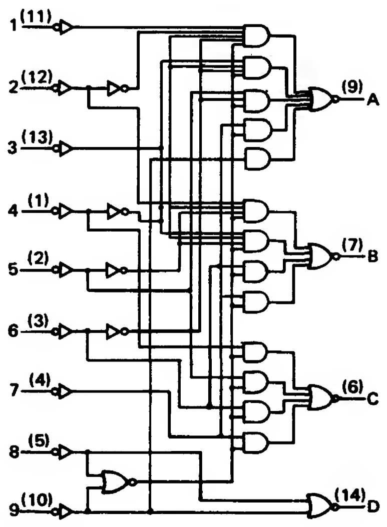


FIGURE 1. Logic Diagram of the '147 Priority Encoder I.C.

Table 1. SN74147 Truth Table

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Table 2. SN74148 Truth Table

INPUTS									OUTPUTS				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant

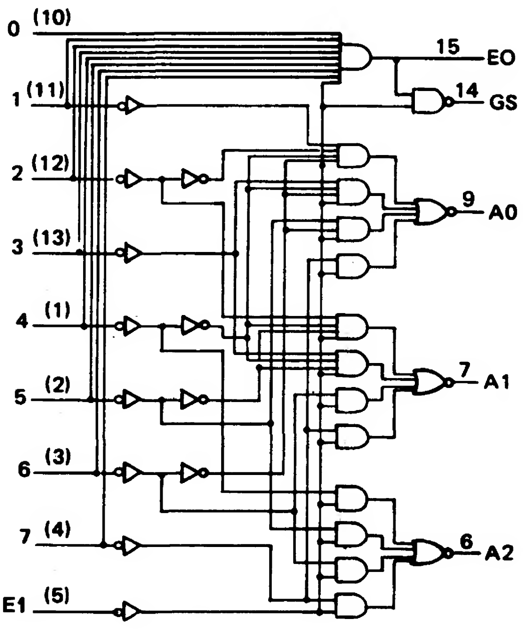


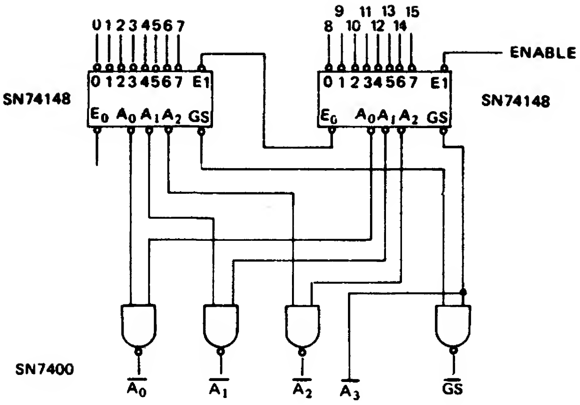
FIGURE 2. Logic Diagram of the '148 Priority Encoder I.C.

Encoder Expansion

The encoders may be cascaded in series or parallel. Series cascading is the simplest but it is slow. Parallel cascading, however, gives high speed but with increased complexity. In order to facilitate cascading additional inputs and outputs are provided, i.e. an ENABLE INPUT which when at a logical '0' forces all outputs to a logical '1', and two additional outputs, ENABLE OUT and GROUP STROBE. The enable output is active 'low' and is produced if all data input lines are at a logical '1'. An active 'low' GROUP STROBE is produced if the encoder is enabled and if at least one input line is at a logical '0'. When cascading, two levels of encoding are required for up to 64 inputs and three levels for 65 to 512 inputs.

Serial Cascading: A two level encoder for 16 input lines is shown in Figure 3. Here the enable output of the highest order encoder feeds the enable input of the next lowest order device. An active low data input to a device will cause the lower order encoder to be inhibited. Since this method of connection only allows an output to be produced from one encoder, selection of this output may be achieved by ORing like outputs of both encoders. This is carried out by two input AND gates operating as OR gates for zeroes. The most significant output data bit of the 16 line encoder is obtained from the GROUP STROBE output of the most significant package. This output is active for input lines 8 to 15.

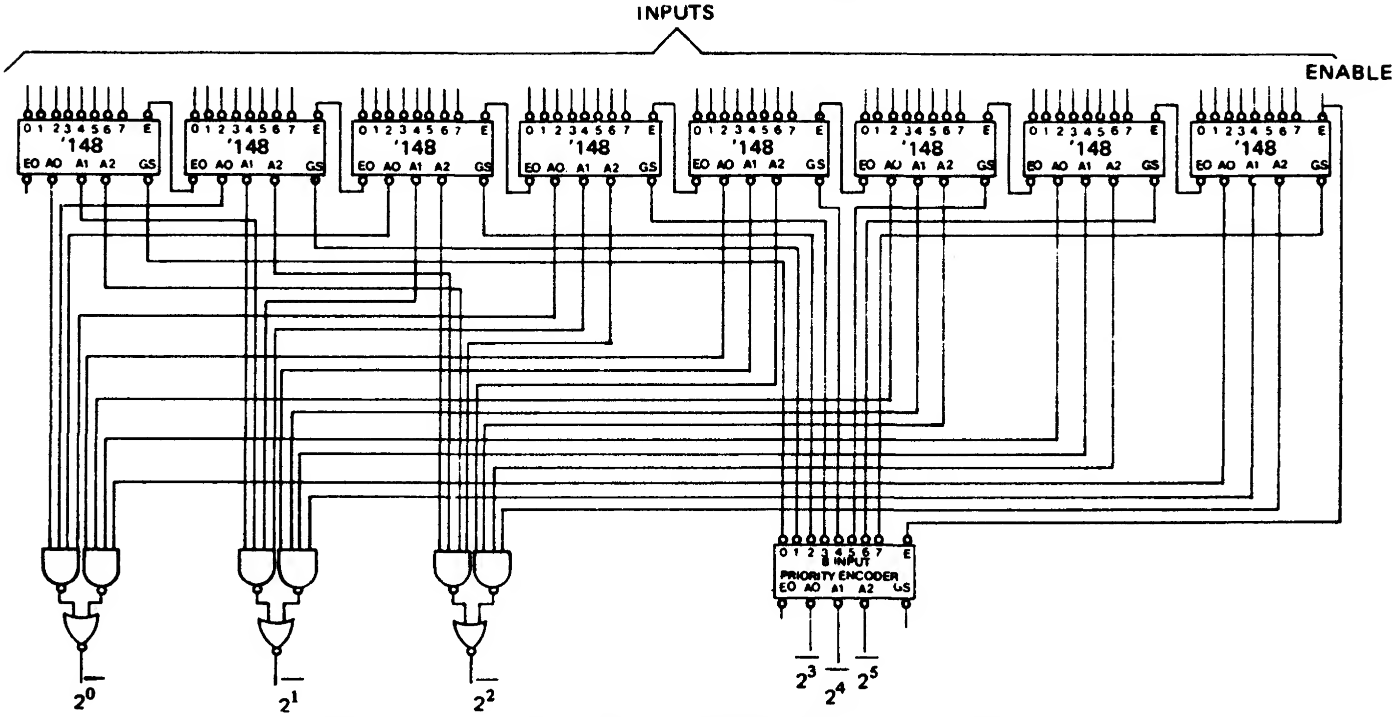
The 64 line encoder, again two level, shown in Figure 4 operates in a similar manner to the previous example. The lower significant bit outputs are ORed by means of NAND and NOR gates, operating as OR gates for zeroes. The higher order most significant bits the GROUP STROBES are encoded by means of an additional 8 line encoder.



0 1 2 3 4 5 6 7
9 11 13 15
8 10 12 14
ENABLE
SN74148
0 1 2 3 4 5 6 7 E1
E0 A0 A1 A2 GS
SN74148
SN7400
$\overline{A_0}$
$\overline{A_1}$
$\overline{A_2}$
$\overline{A_3}$
$\overline{GS}$

FIGURE 3. Encoder Expansion to 16 Lines using Serial Cascading

Parallel Cascading: A high speed 64 line parallel encoder is shown in Figure 5. Here each decoder operates in isolation. All GROUP STROBES are encoded by a separate priority encoder, the input of which addresses the select inputs of three 8 line to 1 line multiplexers. These select the outputs of the highest order encoder that has an active input. The most significant output bits are obtained from a separate group strobe priority encoder. The two level parallel encoder illustrated will encode 64 lines within 60ns, and is suitable for producing the addresses of interrupting inputs from peripherals and, at the same time, give them an order of priority as assigned by their order of connection to the encoder.



INPUTS
ENABLE
0 1 2 3 4 5 6 7 E
'148
EO AO A1 A2 GS
0 1 2 3 4 5 6 7 E
8 INPUT PRIORITY ENCODER
EO AO A1 A2 GS
$\overline{2^0}$
$\overline{2^1}$
$\overline{2^2}$
$\overline{2^3}$
$\overline{2^4}$
$\overline{2^5}$

FIGURE 4. Encoder Expansion to 64 Lines using Serial Cascading

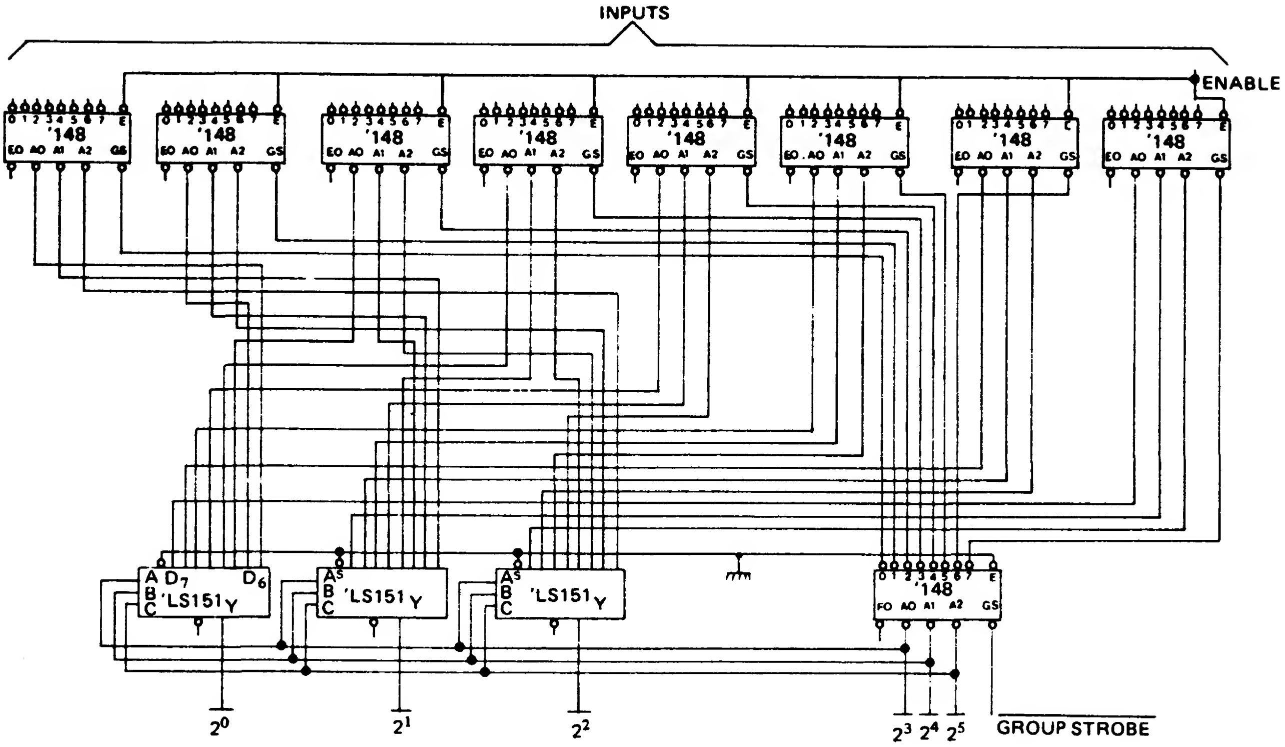

INPUTS
ENABLE
'148
0 1 2 3 4 5 6 7 E
EO A0 A1 A2 GS
'LS151
A B C
D7 D6
Y
2^0
2^1
2^2
2^3 2^4 2^5
GROUP STROBE

FIGURE 5. Encoder Expansion to 64 Lines using Parallel Cascading

KEYBOARD ENCODERS[1]

Using Priority Encoders

Figure 6 shows how a single device may be used as a keyboard encoder. Each key operates by grounding the appropriate encoder input. As shown in Table 1, the '147 priority encoder i.c. has 'active low' inputs and outputs. Anti-bounce protection is given by a dual monostable type SN74221. This is triggered if either the zero key is closed or if any one of the four output data lines changes from a logical '1' to a logical '0'. The monostable trigger signal is produced by cascaded AND gates operating as NOR gates for zeroes. In this example a ten key keyboard can be encoded. Larger keyboards can be encoded by cascaded devices as described until the overall priority encoder has the right number of inputs.

Using Multiplexers and Counters

The basis of another method of keyboard encoding is shown in Figure 7. This technique uses a multiplexer and two counters, one of which operates as a four bit latch and also produces a strobe signal. The system is operated by a

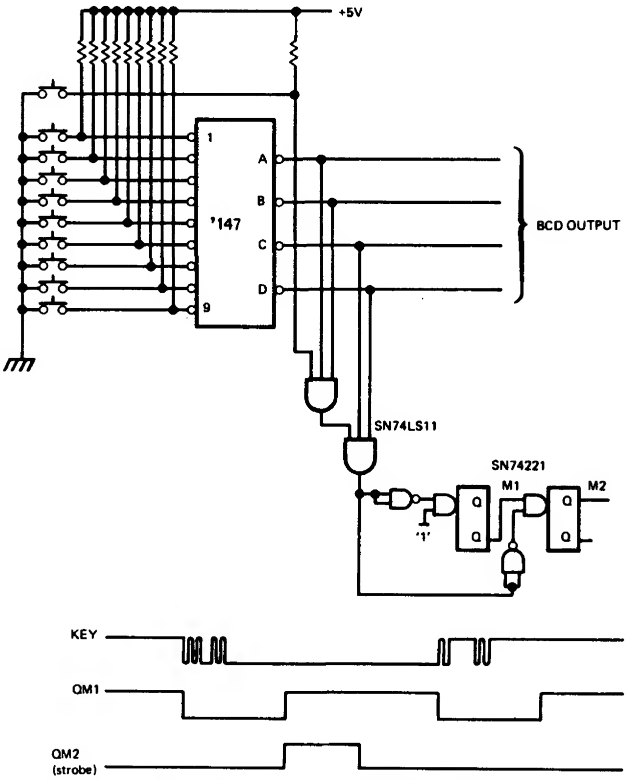

+5V
1
9
'147
A
B
C
D
BCD OUTPUT
SN74LS11
SN74221
M1
M2
Q
Q
'1'
KEY
QM1
QM2
(strobe)

FIGURE 6. Logic Diagram and Operating Waveforms for Keyboard Encoder

clock which drives the first counter. The counter output is the address to the multiplexer so that each input of the multiplexer is selected in sequence. The output and therefore the selected input of the multiplexer is connected to the CLEAR and LOAD terminals of the first and second counters respectively. If no key has been depressed then all the inputs, except the last, will be logical '1' and only when the address from the first counter reaches 1111 will the CLEAR and LOAD inputs be taken 'low'. When the LOAD input of the second counter is taken 'low', then, on the next clock pulse, the counter will be loaded with the address of the multiplexer. In this case it is 1111 and this will appear on the output. The output of 1111 and CET taken to a logical '1' produces a carry signal. This is, therefore, the only input for which a carry signal is produced, and the absence of a carry can be used as a strobe. If at some time, a key is pressed, then the multiplexer will scan through until that input takes the load and clear of the counters 'low'. On the next clock pulse the address, as produced by the first counter, is loaded into the second counter, so that the key address appears at the output. The CARRY output returns to a logical '0' indicating that a key has been selected. At the same time the first counter is cleared to 0000. Therefore, as long as a key is depressed, the first counter never reaches 1111 and a strobe signal is available from the CARRY output. A feature of this system is that key bounce is suppressed and does not affect the output. Using the components shown in Figure 7, a 15 way keyboard can be encoded, but this technique can also be extended by using wider multiplexers and longer counters.

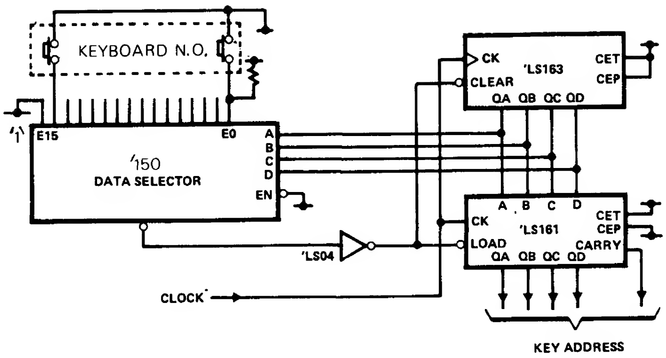

KEYBOARD N.O.
'1'
E15
E0
'150
DATA SELECTOR
A
B
C
D
EN
'LS04
CLOCK
CK
'LS163
CLEAR
CET
CEP
QA QB QC QD
A B C D
CK
'LS161
LOAD
CET
CEP
CARRY
QA QB QC QD
KEY ADDRESS

FIGURE 7. Keyboard Encoder using Multiplexers and Counters

DIGITAL TO ANALOGUE CONVERTERS

Many methods of digital to analogue conversion require the use of precision resistor ladder networks and their associated analogue switches and control logic. Two methods that use a minimal number of analogue components are given here. Both use pulse duration modulation (p.d.m.) techniques, the first employing priority encoders and the second comparators.

Using Priority Encoders

This method is useful if several conversions are required to be carried out simultaneously. Each additional data channel only requires the addition of a multiplexer and integrator as shown in Figure 8. The bits of the binary word that are to be converted into analogue form are sampled by an 8 to 1 line multiplexer. The priority encoder selects the bits in an order such that the most significant bit is selected for 50% of the counter cycle time, and the next least significant bit for 25%, and so on. This method of selection gives the required binary weighting and a well interleaved pulse train that requires the minimal amount of integration to recover the analogue signal. To obtain a high degree of accuracy it is advisable to retime the multiplexer to the counter clock to minimise errors due to circuit delays. This is carried out by D-type latches.

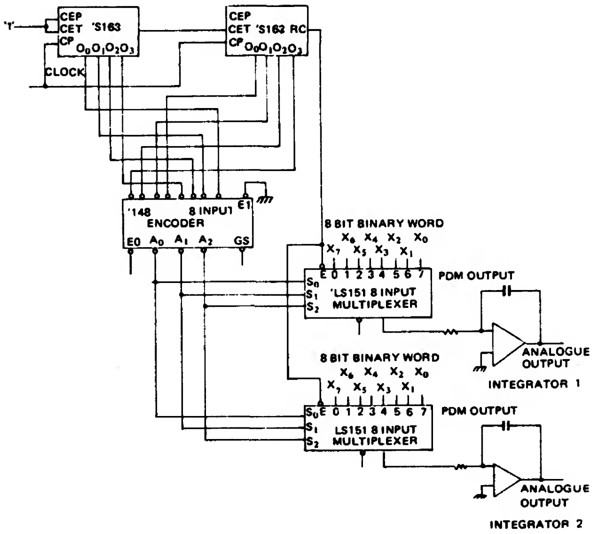

'1'
CEP
CET 'S163
CP $O_0O_1O_2O_3$
CLOCK
CEP
CET 'S163 RC
CP $O_0O_1O_2O_3$
'148 8 INPUT ENCODER
E1
E0 A_0 A_1 A_2 GS
8 BIT BINARY WORD
X_6 X_4 X_2 X_0
X_7 X_5 X_3 X_1
S_0 E 0 1 2 3 4 5 6 7
S_1 'LS151 8 INPUT MULTIPLEXER
S_2
PDM OUTPUT
ANALOGUE OUTPUT
INTEGRATOR 1
8 BIT BINARY WORD
X_6 X_4 X_2 X_0
X_7 X_5 X_3 X_1
S_0 E 0 1 2 3 4 5 6 7
S_1 LS151 8 INPUT MULTIPLEXER
S_2
PDM OUTPUT
ANALOGUE OUTPUT
INTEGRATOR 2

FIGURE 8. Digital to Analogue Converter using Priority Encoders

Using Comparators

The second method of generation, which will achieve at least ten bit accuracy, is not applicable to high speed conversion, although a procedure for increasing the conversion rate is outlined. As already mentioned the principle by which the system operates is one of p.d.m.. A repetitive waveform of fixed frequency but of varying mark to space ratio is produced. The mark duration is directly proportional to the digital input code that is to be converted into an analogue voltage. The mean value of such a repetitive waveform is also proportional to the digital input code and is easily obtained by partial integration of the waveform with a low pass filter network.

The logic of the basic converter is shown in Figure 9. Low power Schottky components have been employed in order to obtain high speed with low power dissipation. A synchronous counter connected in the high speed parallel enable mode counts continuously. This may count in either binary or b.c.d. depending on the coding of the input that is to be converted into analogue form. A synchronous counter must be used in this application in order to minimise errors due to differential propagation delays between the clock input and the counter outputs. For b.c.d. input coding the SN74LS160 should be used and for binary use the 'LS161. The number in the counter, at any instant in time, is continuously compared by means of four bit comparators with the input code being converted. The comparators have three outputs A>B, A<B, and A = B. In this application the A<B output is used. This output remains at a logical '1' for the period when the counter contents are numerically less than the input code being converted. Small 'glitches' can appear at the comparator output due to differential propagation delays, caused by the serial cascading of the comparators. For high accuracy conversion these 'glitches' can be removed by retiming the comparator output with a D-type latch 'clocked' from the counter clock. In order to recover the analogue output, the comparator feeds a high speed precision switch whose output switches between two reference levels; one of which is normally ground. The switch is formed by a complementary pair of transistors operating in the inverted mode to give a low offset voltage. A CR network on the output of the switch forms a partial integrator from which the analogue output is obtained. The required integrator time constant is a function of the counter clock rate and the maximum ripple allowable on the analogue output.

One method of reducing the output ripple, for a given time constant, is to replace the incrementing counter by a counter that counts pseudo-randomly through all the possible output states. Such a device could be a feedback shift register pseudo-random number generator (p.n.g.) using modulo two feedback. In such a system, as shown in Figure 10, the p.n.g. consists of two 'LS195 four bit shift registers arranged as an eight bit register with modulo two feedback taken from stages four, five, six and eight. The modulo two sum of these outputs is formed by cascading 'LS86 two input exclusive OR gates. This type of feedback will give a counting cycle of maximal length 2^n-1, where n is the number of register stages. The remaining state, $2^n-(2^n-1)$, is the all zeros state and will cause the counter to 'stick' because the feedback will enter a zero if this condition is reached. This may occur due to switch-on transients etc. To alleviate this problem the all zeros state is detected by using 'LS27 NOR gates as AND gates for zeros. Their outputs are then 'ANDed' by an 'LS11 three input AND, the output of which is a logical '1' only when all register stages contain zero. This controls one input of an exclusive OR in the register feedback path. The exclusive OR acts as a controlled inverter, inverting the register input when the all zeros state is detected, thereby forcing the register into the maximal length count sequence.

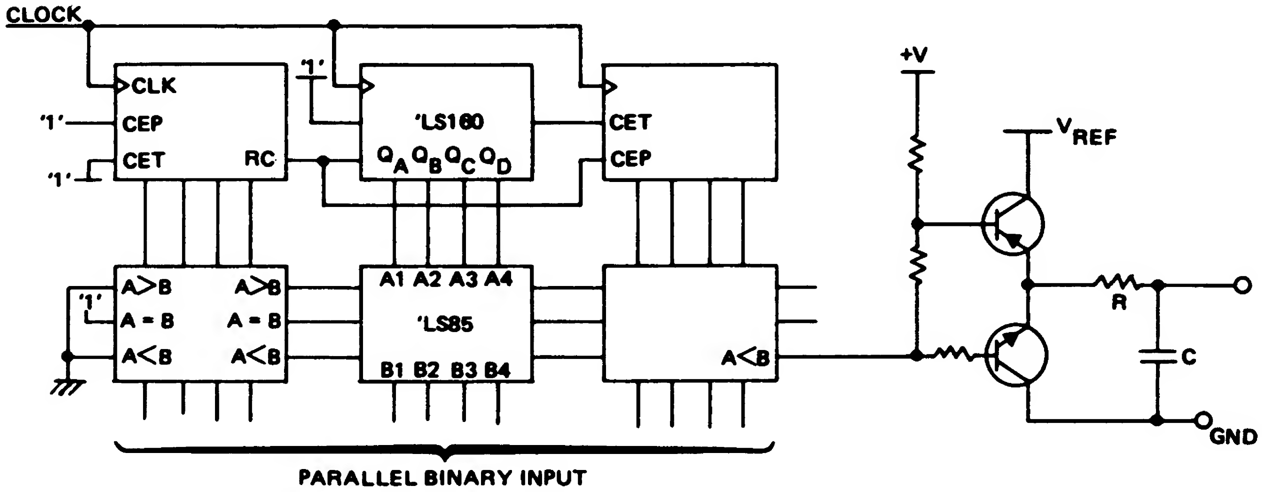


FIGURE 9. Digital to Analogue Converter using Comparators

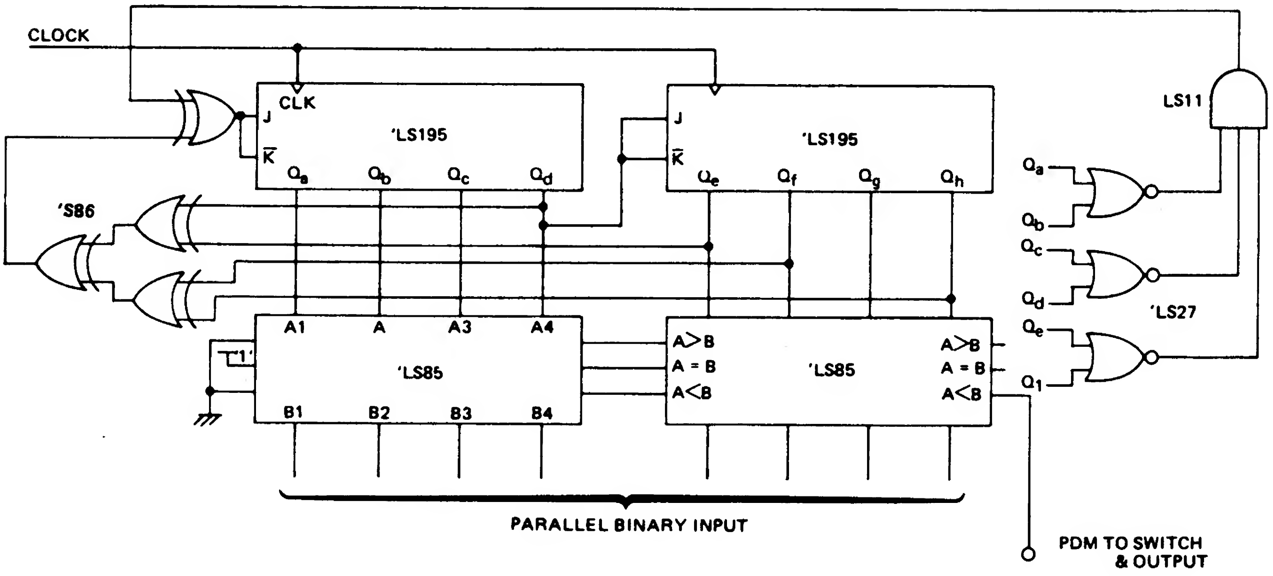


FIGURE 10. Digital to Analogue Converter using P.N.G.

Such a method is possible for a binary conversion. However, for b.c.d. conversion, the output from the shift register, or whatever feeds the comparators, must always be a valid three digit b.c.d. number. This is difficult to perform with a p.n.g. but an improvement to the output can be achieved by rotating the order of the digits so that the m.s.d. is changed for the l.s.d., etc.

PRECISION TRIANGULAR FUNCTION GENERATOR

Another system possibility is that, instead of producing an analogue voltage from the digital output of a processor, a frequency is required or even a repetitive waveform. The following circuit produces a highly linear triangular function generator, using low power Schottky programmable counter i.c.s. Such a precision generator may be used as sweep and function generators. For example, when used in conjunction with a diode shaping network most non linear functions may be generated. This system again uses digital techniques to generate the desired waveform. Waveforms with a very low repetition rate may be produced, i.e. <0·1 Hz, without the need for large time constants as would be required if an analogue method were used. If a standard frequency clock generator is employed, then the output frequency of the generator may be digitally programmed so that a source of swept frequency may be produced.

Figure 11 shows the block diagram of the system and Figure 12 illustrates the associated operating waveforms. In order to generate a stable low frequency output, digital frequency mixing is adopted. A stable high frequency clock is counted down by two dividers M and N. The M divider is programmable, i.e. its division ratio is determined by means of preset digital inputs. The outputs from these two dividers are mixed in an exclusive OR so as to generate the sum and difference frequency components. With reference

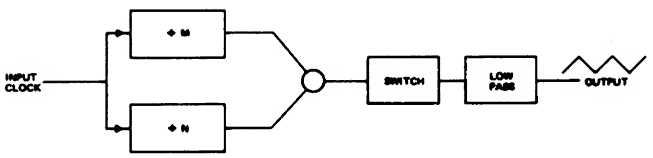


FIGURE 11. Block Diagram of Precision Triangular Function Generator

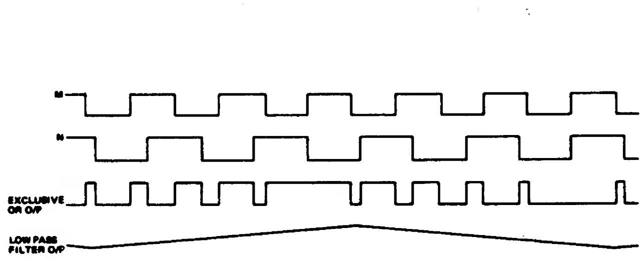


FIGURE 12. Simplified Operating Waveforms

to Figure 12 it can be seen that the output of the exclusive OR gate is a series of pulses whose mark to space ratio varies cyclically at the difference frequency. If a triangular output waveform of defined amplitude is required then the exclusive OR should be followed by a precision analogue switch and an active low pass filter. If, however, this is not required, then a simple CR filter can follow the exclusive OR gate.

Figure 13 shows the logic diagram of a practical system which uses the low power Schottky devices in order to obtain high speed with low power consumption. The two dividers, one fixed, the other programmable, are obtained by cascading SN74LS163N 4-bit synchronous binary counters. These are fully programmable, i.e. their outputs may be synchronously preset to any state by means of the load and parallel data inputs. Each 4-bit counter is provided with serial and parallel enable inputs, and a carry output. These allow counter cascading whilst still maintaining a high count rate. By enabling the load inputs with the carry output from the last stage and setting up data on the parallel data inputs a programmable divider is produced. Parallel data present on the data inputs is transferred through to the outputs on the next clock pulse following the load command. The inputs to the exclusive OR mixer gate should have a 1:1 mark space ratio in order to obtain from it the maximum amount of energy at the difference frequency. The carry outputs from each counter are of a width equal to that of the clock period and must be converted into symmetrical square waves before being mixed. Since the carry outputs may contain 'glitches' this is best achieved by using synchronous T-type flip-flops. Standard D-types are used with modulo two feedback to obtain T-type operation.

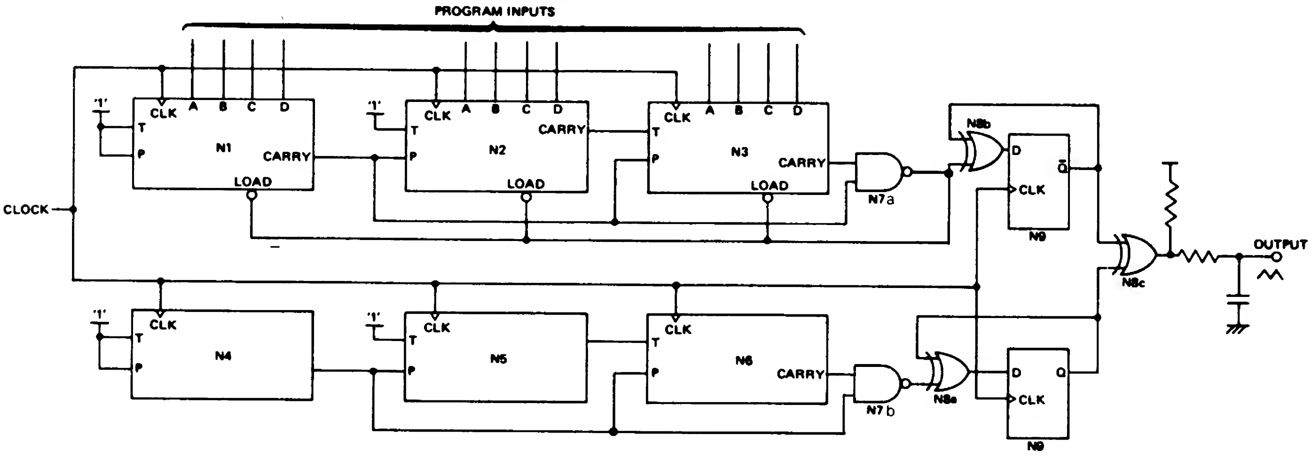
If x is the binary number corresponding to the program inputs and if r is the maximum division ratio for each counter then the period t of the triangular output is given by,

$$t = r . (r-x)/f_{in}$$

where f_{in} is the input clock frequency.

REFERENCE

1. *'Semiconductor Circuit Design'* Volume III, Texas Instruments Ltd., pp 27-29, April 1974.



N1, N2, N3, N4, N5, N6.	SN74LS163N
N7	SN74LSOON
N8	SN74LS86N
N9	SN74LS74N

Note all unused inputs must be connected to a defined logic level

FIGURE 13. Circuit Diagram of Precision Triangular Function Generator

XV DISPLAY AND COUNTING CIRCUITS

by
David A. Bonham

After processing the information in a system it is usually necessary to display the results. The replacement of the incandescent display by the visible light emitting diode (v.l.e.d.) has been widespread due, mainly, to the latter's compatibility with integrated circuits, reliability and small physical size. Circuits which couple the v.l.e.d. to i.c. counter circuits have been described in a previous volume[1]. Also introduced there, were some of the new products which further simplify the design of systems using both counting and digital read-out. These devices combine an l.e.d. display, so that counting, storing, and display can all be performed in one device. This chapter describes the construction, operation and a number of applications of these devices.

CONSTRUCTION

V.l.e.d.s are available in a variety of configurations employing a varying amount of i.c. logic and drive circuits. A block diagram showing the possible sections that can be combined into one package is given in Figure 1. The counter is a high speed synchronous decade counter with full cascading facilities. The latch is simply composed of cross coupled NAND gates. The outputs of the latches are often brought out externally for use when needed. The decoder takes the information from the latch outputs and converts it into the desired signals to produce the display through drivers. The latter are generally of constant current form and do not require external current defining resistors. The display is arranged in one of three forms, seven segment, hexadecimal, or alphanumeric (a 5x7 matrix). The descriptions of the devices are divided into these three display configurations. A list of some available devices and their characteristics is given at the end of the chapter in Table 1.

DESCRIPTION

Seven Segment Displays

Display Only: The simplest devices are merely an array of v.l.e.d.s in the configuration shown in Figure 2, e.g. TIL302/3, etc. as listed in Table 1. These diodes are capable of forming the characters shown in Figure 3 when

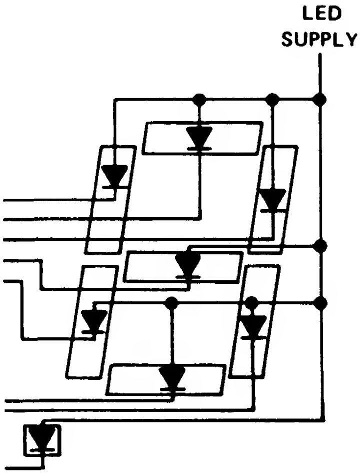


FIGURE 2. V.L.E.D. Array

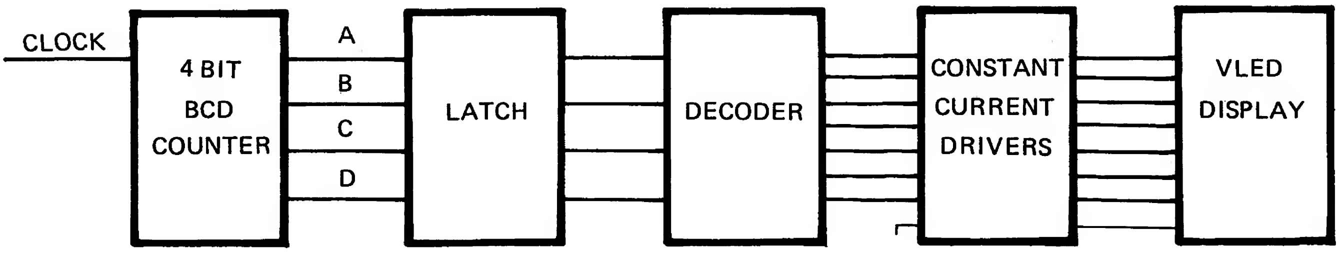


FIGURE 1. Possible Device Sections

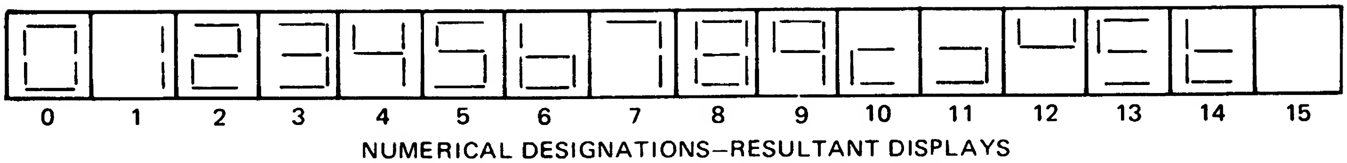


FIGURE 3. Possible 7-Segment Characters

driven by a t.t.l. decoder such as the SN7447A. They can also display certain simple letters such as A C E F etc. and be amber and green as well as the more common red.

Decoder, Driver and Display: A block diagram of such a device e.g. the TIL506, is shown in Figure 4. These accept 4-line b.c.d. input in negative logic and display the decimal number in a 7-segment format. Invalid input codes are automatically blanked as shown in Table 2. A 'high' logic level voltage at the decimal point (d.p.) input turns on the decimal independently of the b.c.d. inputs. The d.p., as well as each segment, is driven by a constant current from the logic 'chip'. Varying the v.l.e.d. supply voltage will not significantly affect the brightness of the display. The brightness may be controlled by pulse width modulation of the b.c.d. inputs, alternating between a valid and invalid code, e.g. all inputs 'low'.

Latch, Decoder, Driver and Displays: The functional diagram of such a device, i.e. the TIL308/9, is shown in Figure 5. This accepts an 8-4-2-1 4-bit code, stores it in latches and displays the stored character. The inputs and outputs, which are t.t.l. compatible, are LATCH DATA INPUTS, LATCH OUTPUTS, LATCH STROBE, BLANKING INPUT, and LED TEST INPUT. The data and decimal point on the LATCH DATA INPUT lines are transferred into the latch flip-flops when LATCH STROBE is 'low'. The data and decimal point data stored in the latches are available at the LATCH OUTPUTS. With the LATCH STROBE 'high' the LATCH DATA INPUT lines can change

Table 2. Truth Table — Recorder, Driver and 7-Segment Display

FUNCTION	DATA INPUTS					DISPLAY
	$\bar{D}$	$\bar{C}$	$\bar{B}$	$\bar{A}$	DP	
0	H	H	H	H	L	0
1	H	H	H	L	H	.1
2	H	H	L	H	L	2
3	H	H	L	L	H	.3
4	H	L	H	H	L	4
5	H	L	H	L	H	.5
6	H	L	L	H	L	6
7	H	L	L	L	H	.7
8	L	H	H	H	L	8
9	L	H	H	L	H	.9
BLANK	L	H	L	H	L	
BLANK	L	H	L	L	H	.
BLANK	L	L	H	H	L	
BLANK	L	L	H	L	H	.
BLANK	L	L	L	H	L	
BLANK	L	L	L	L	H	.

H = high logic level, L = low logic level
DP input has arbitrarily been shown activated (high) on every other line of the table.

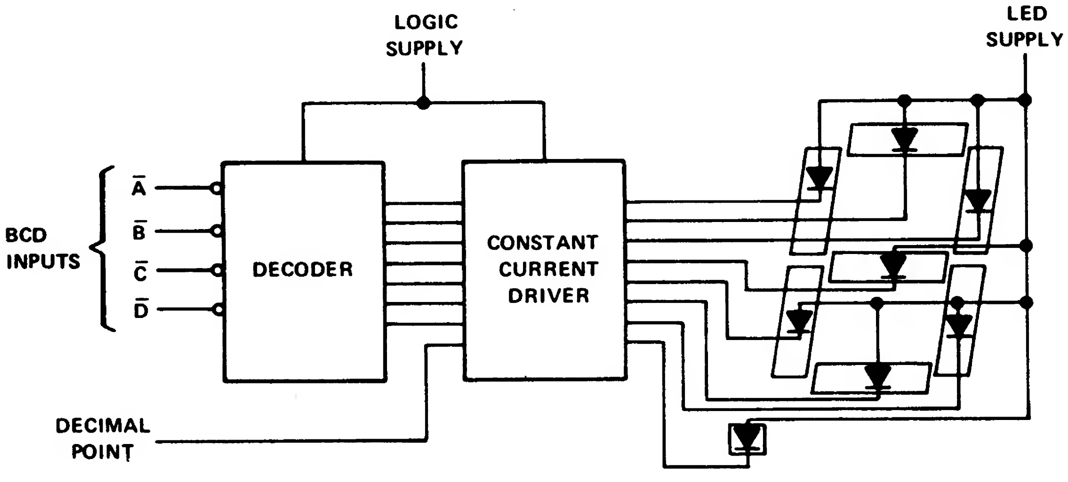


FIGURE 4. Block Diagram of Decoder, Driver and Display Device

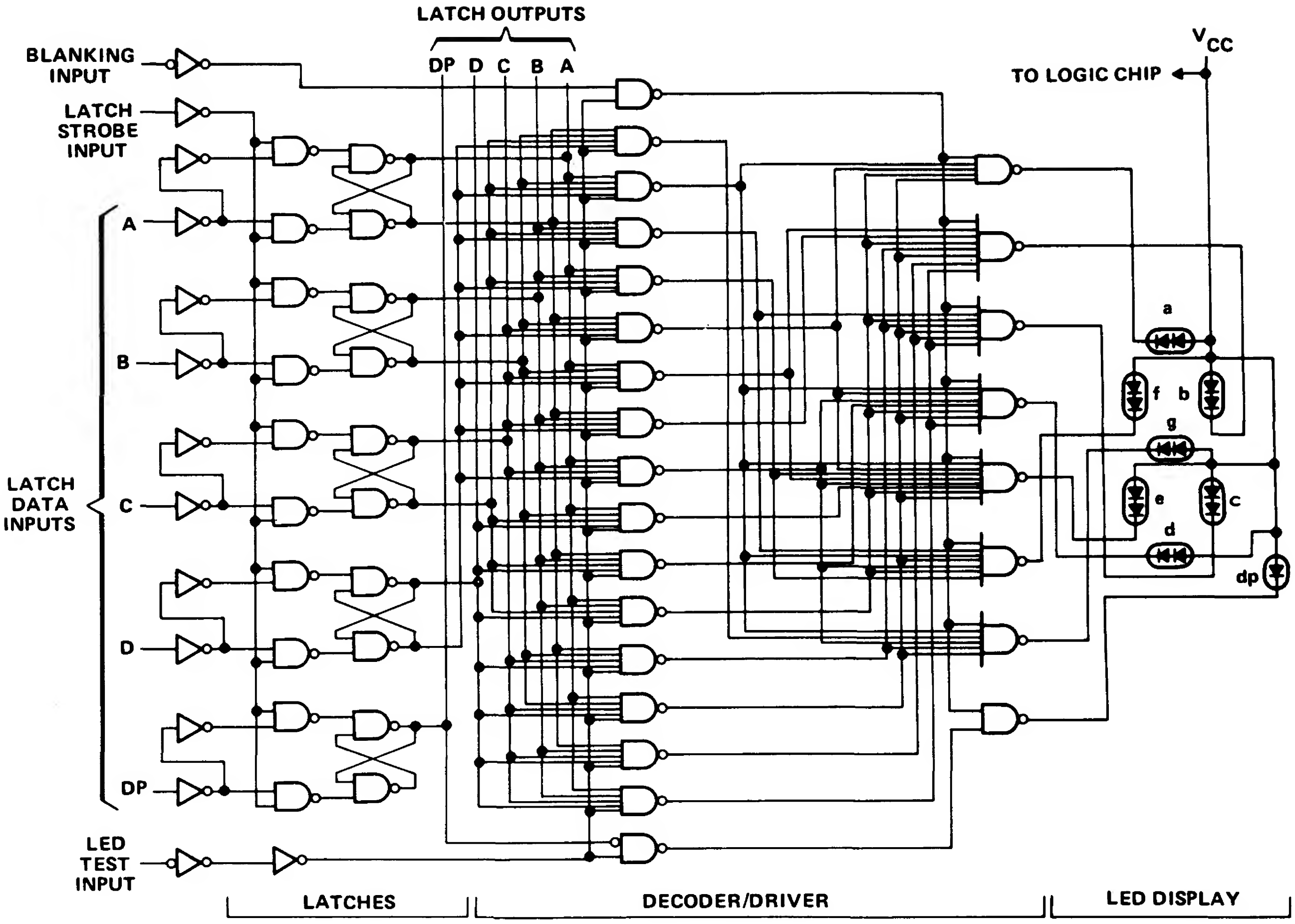


FIGURE 5. Functional Diagram of Latch, Decoder, Driver and Display Device

without effecting the data stored in the latches, the BLANKING INPUT must be 'high' to display the data stored in the latches. When the BLANKING INPUT goes 'low', the decoder drivers are inhibited and l.e.d. display is turned 'off'. The data stored in the latches are not effected by the BLANKING INPUT. A 'low' on the LED TEST INPUT will override all other signals and turn all of the l.e.d.s 'on'. The LED TEST INPUT does not change the status of the latches. The v.l.e.d. driver outputs are designed specifically to maintain a relatively constant 'on' level current of approximately 15mA through the l.e.d. segments and 7mA through the d.p. diode. The 4-bit input is displayed or blanked in accordance with the listing shown in Table 3.

Counter, Latch, Decoder, Driver and Display: Devices which perform all these functions are the TIL306/7 whose functional diagram is shown in Figure 6. The counter is connected as a synchronous counter. This configuration takes advantage of the minimal propogation delay to give maximum speed capability. Inputs to the counter are CLEAR, CLOCK, SERIAL CARRY and PARALLEL CARRY. The counter and its inputs generate an output, MAX COUNT. Additional connections are LATCH STROBE, BLANKING, RIPPLE BLANKING, and DECIMAL POINT INPUTS, RBO NODE and LOGIC OUTPUTS. All inputs and outputs are t.t.l. compatible. A 'low' input to the CLEAR will reset the counter to zero independently of any other input. As long as the input remains 'low' the counter remains at zero. A 'high' is required to allow the counter to count. The CLOCK input is the signal to be counted. With an input the counter will advance from 0 to 9. At a count of 9 the counter automatically resets to 0 with the next pulse. The counter changes state on the positive-going edge of the clock pulse. The clock pulse to the counter is enabled by the SERIAL and PARALLEL CARRY INPUTS. The MAX COUNT output goes 'low' when the counter reaches a count of 9, and then goes 'high' when the counter progresses to 0 on the next clock input. This output can be connected to the CLOCK input of the next decade position for asynchronous operation or to the SERIAL CARRY INPUT of the next decade position for synchronous operation. A 'high' on the SERIAL CARRY INPUT inhibits the counter and forces the MAX COUNT to go 'high' regardless of the state of the counter stages. When the SERIAL and the PARALLEL CARRY INPUTS go 'low',

Table 3. Truth Table – Latch, Decoder, Driver and 7-Segment Display

FUNCTION	LATCH INPUTS						BLANKING INPUT	LED TEST	LATCH OUTPUTS					DISPLAY	
	D	C	B	A	DP	STROBE			Q_D	Q_C	Q_B	Q_A	Q_{DP}	TIL308	TIL309
0	L	L	L	L	L	L	H	H	L	L	L	L	L	0	0
1	L	L	L	H	H	L	H	H	L	L	L	H	H	.1	1.
2	L	L	H	L	L	L	H	H	L	L	H	L	L	2	2
3	L	L	H	H	H	L	H	H	L	L	H	H	H	.3	3.
4	L	H	L	L	L	L	H	H	L	H	L	L	L	4	4
5	L	H	L	H	H	L	H	H	L	H	L	H	H	.5	5.
6	L	H	H	L	L	L	H	H	L	H	H	L	L	6	6
7	L	H	H	H	H	L	H	H	L	H	H	H	H	.7	7.
8	H	L	L	L	L	L	H	H	H	L	L	L	L	8	8
9	H	L	L	H	H	L	H	H	H	L	L	H	H	.9	9.
A	H	L	H	L	L	L	H	H	H	L	H	L	L	A	A
MINUS SIGN	H	L	H	H	H	L	H	H	H	L	H	H	H	.–	–.
C	H	H	L	L	L	L	H	H	H	H	L	L	L	C	C
BLANK	H	H	L	H	H	L	H	H	H	H	L	H	H	.	.
E	H	H	H	L	L	L	H	H	H	H	H	L	L	E	E
F	H	H	H	H	H	L	H	H	H	H	H	H	H	.F	F.
BLANK	X	X	X	X	X	X	L	H	X	X	X	X	X		
LED TEST	X	X	X	X	X	X	X	L	X	X	X	X	X	.8	8.

H = high level, L = low level, X = irrelevant.
DP input has arbitrarily been shown activated (high) on every other line of the table.

the CLOCK is enabled to the counter stages and the MAX COUNT gate is allowed to sense the status of the counter. The logic level of the SERIAL or PARALLEL CARRY INPUTS must not be allowed to change while the CLOCK is 'low' or erroneous counts may result. The PARALLEL CARRY INPUT permits look ahead carry inputs from lower order decade positions. A 'high' input inhibits the clock to the counter stages. The LATCH STROBE INPUT transfers the data in the counter stages to the latch storage to be displayed. With the LATCH STROBE INPUT 'low' the latch flip-flops follow the states of the counter flip-flops. When the LATCH STROBE INPUT goes 'high', the counter data is stored in the latch flip-flops. The counter can continue to count while the previous information is stored in the latches. A 'high' on the DECIMAL POINT INPUT is required to turn 'on' the l.e.d. d.p. display. A 'high' on the BLANKING INPUT inhibits the driver and gates, and blanks the l.e.d. display. For normal operation, the BLANKING INPUT must be 'low'. A 'low' on RIPPLE BLANKING INPUT blanks the display if the latch flip-flops contain a count of zero. This combination also forces the RBO NODE to go 'low'. By connecting the RBO NODE of one decade position to the RIPPLE BLANKING INPUT of the next decade position, zero suppression can be achieved. This is discussed later. The RBO NODE has a resistor 'pull-up' which allows this output to be used as an input. A 'low' level applied to RBO NODE will blank the l.e.d. display independently of any other input. The constant currents driver outputs are the same as those of the TIL308/9. The character format is identical in size and shape except that, because it is driven by a decade counter, only the numbers 0 to 9 are used.

Hexadecimal Displays

These devices can store and display decimal or hexadecimal data. Devices, such as the TIL311 or TIL505 have latch, decoder, constant current driver and display as shown in Figure 7. They accept parallel 8-4-2-1 data on four input lines and display the corresponding decimal or hexadecimal character on a 4 by 7 dot matrix. Figure 8 illustrates the

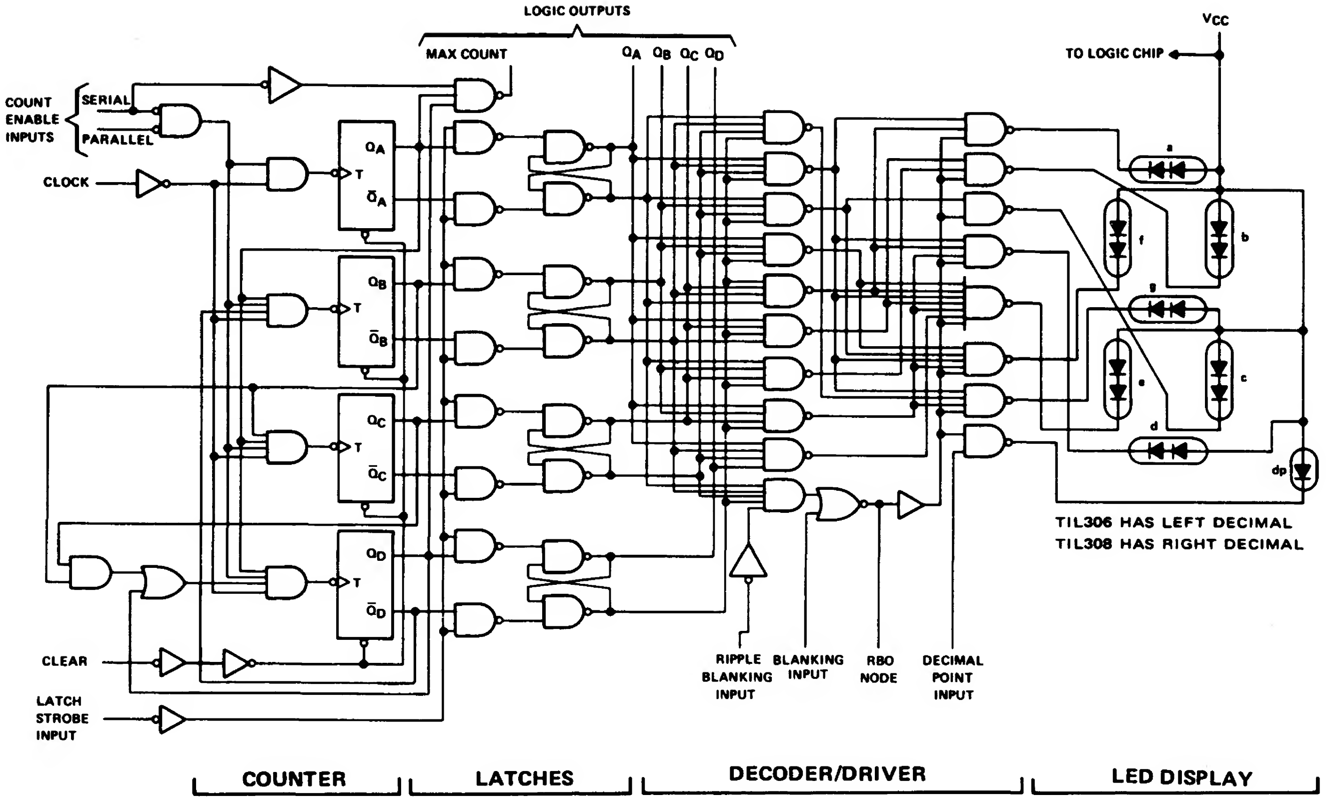

LOGIC OUTPUTS
MAX COUNT
Q_A Q_B Q_C Q_D
Vcc
TO LOGIC CHIP
COUNT ENABLE INPUTS
SERIAL
PARALLEL
CLOCK
Q_A
T
$\bar{Q}_A$
Q_B
$\bar{Q}_B$
Q_C
$\bar{Q}_C$
Q_D
$\bar{Q}_D$
a
b
c
d
e
f
g
dp
TIL306 HAS LEFT DECIMAL
TIL308 HAS RIGHT DECIMAL
CLEAR
LATCH STROBE INPUT
RIPPLE BLANKING INPUT
BLANKING INPUT
RBO NODE
DECIMAL POINT INPUT
COUNTER
LATCHES
DECODER/DRIVER
LED DISPLAY

FIGURE 6. Functional Diagram of Counter Latch, Decoder, Driver and Display Device

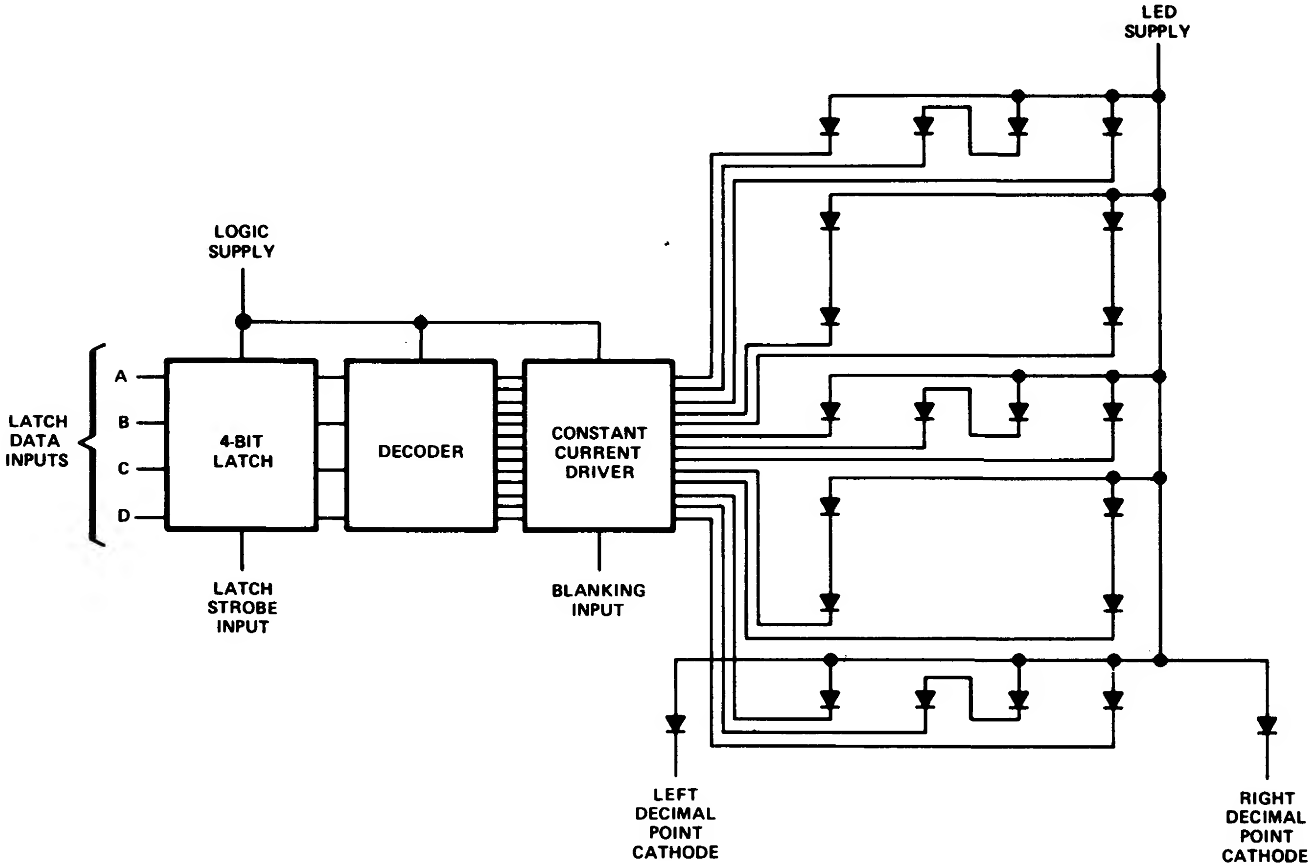

LED SUPPLY
LOGIC SUPPLY
LATCH DATA INPUTS
A
B
C
D
4-BIT LATCH
DECODER
CONSTANT CURRENT DRIVER
LATCH STROBE INPUT
BLANKING INPUT
LEFT DECIMAL POINT CATHODE
RIGHT DECIMAL POINT CATHODE

FIGURE 7. Block Diagram of Hexadecimal Display Device

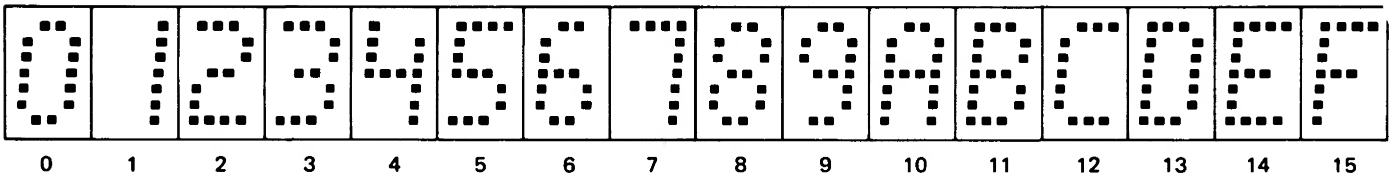


FIGURE 8. Hexadecimal Character Representation

hexadecimal character representation for decimal numbers 0 to 15. The logic levels are again t.t.l. compatible. The v.l.e.d.s contain two decimal points, one to the left and one to the right of the character. When a d.p. is used, an external resistor, or other current limiting mechanism must be connected in series with it. The input data are decoded and the required diodes are turned 'on' via the constant current drivers to display the correct character. The drivers maintain a relatively constant current of approximately 5mA through each of the v.l.e.d.s. The BLANKING INPUT must be 'low' to display the character. When it goes 'high', the character is turned 'off' regardless of the inputs and it does not change the data stored in the latches. The BLANKING INPUT may be pulsed to intensity modulate the display. The apparent brightness of the display is proportional to the duty cycle of the modulating signal, assuming a frequency high enough to avoid visible flicker. For example, at 1kHz a 50% duty cycle would cause an apparent brightness of 50% of the steady state brightness.

Alphanumeric Displays

Display Only: These devices consist a 5x7 matrix of v.l.e.d.s with the anodes commoned in columns and the cathodes commoned in rows as shown for the TIL305/504 in Figure 9. There is also a left hand d.p. included in the packages.

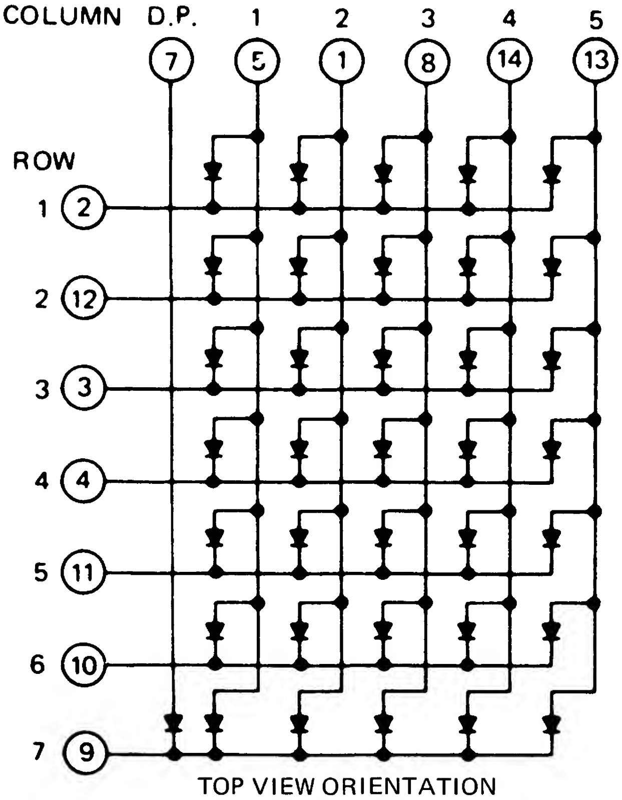


FIGURE 9. V.L.E.D. Matrix for Alphanumeric Display

Latch, Driver and Display: Six D-type flip-flops are included in these devices which can transfer data from a character generator to the five columns of the matrix and the d.p.. Examples of this type of device are the TIL507 and TIL508. Figure 10 shows the functional diagram of the TIL508 and how by reorientating the package a display can be obtained with decimal points of the opposite hand. The TIL507 is similar to the left orientation of the 508 except that it does not have D.P. 1 and it is physically larger. The chips also include six cathode column drivers with series limiting resistors. To operate the display the rows are strobed by sequentially applying a positive voltage to each row input. As each row is strobed the data set up at the column inputs is transferred to the column drivers on the rising edge of each clock pulse. A 'high' column input causes the v.l.e.d. to turn 'on'. After the minimum hold time requirement has been satisfied, the column data inputs may change whether the clock is 'high' or 'low'.

Shift Register, Driver and Display: A device which has these features is the TIL560 whose schematic diagram is shown in Figure 11. This contains three 5x7 matrixes of diodes, two 8-bit shift registers, which allows the use of a single input to enter a row of data, and fifteen internal resistors. The latter are in series with the shift register outputs and are used to control the v.l.e.d. current. Their value is matched to the diode 'chips' to control the light intensity, but the v.l.e.d. peak current cannot exceed 12mA.

APPLICATIONS

3½ Digit Display

The circuit shown in Figure 12 uses three TIL303 v.l.e.d. seven-segment displays and a TIL304 display, which incorporates a positive or negative sign with a number one, to produce a 3½ digit display. The segments are driven by an SN7447A decoder/driver which converts the b.c.d. input from an SN7490A counter into the required digit. The brightness of the segments is controlled by selecting resistors R1 and R2. The d.p. is determined by an external range switch which grounds the line from the desired d.p.. The minus sign is 'hardwired' to always emit light and it is changed to a plus sign by grounding the line to the vertical segments of the sign. The clear function will blank the half digit and reset the other three digits to zero. Following resetting, input pulses will be counted, decoded, and displayed.

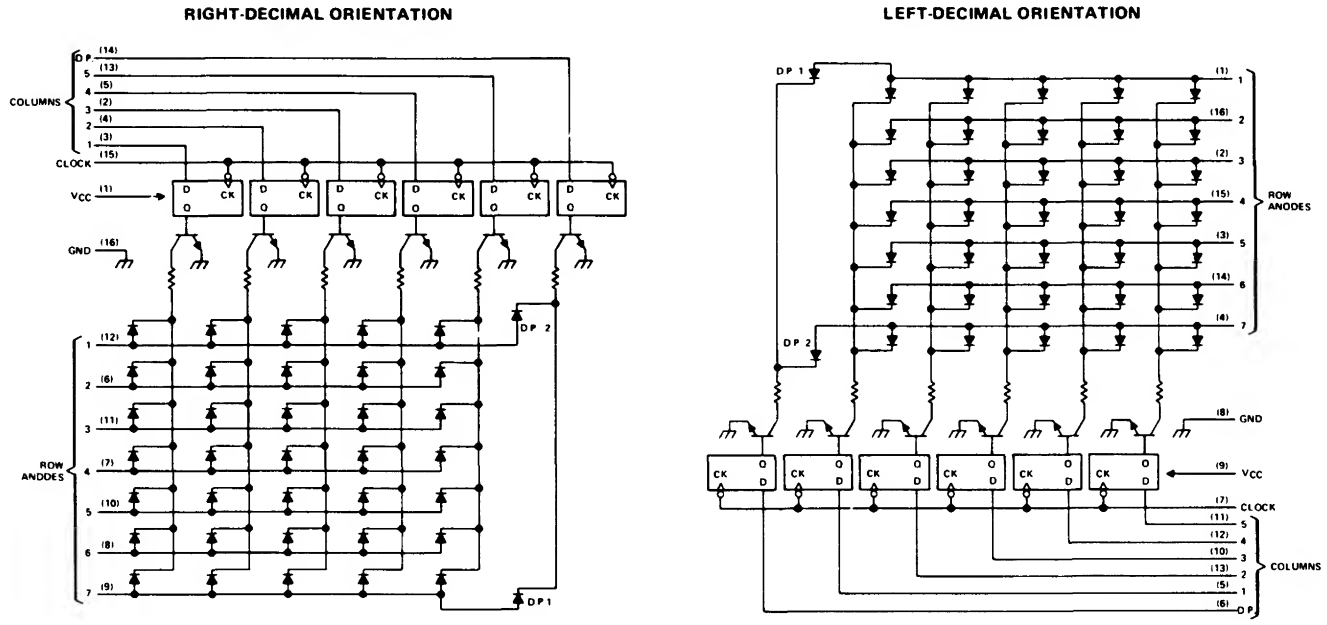

RIGHT-DECIMAL ORIENTATION
LEFT-DECIMAL ORIENTATION
COLUMNS
D.P. (14)
5 (13)
4 (5)
3 (2)
2 (4)
1 (3)
CLOCK (15)
VCC (1)
GND (16)
D
CK
Q
ROW ANODES
1 (12)
2 (6)
3 (11)
4 (7)
5 (10)
6 (8)
7 (9)
DP 2
DP 1
DP 1
(1) 1
(16) 2
(2) 3
(15) 4
(3) 5
(14) 6
(4) 7
ROW ANODES
DP 2
(8) GND
(9) VCC
(7) CLOCK
(11) 5
(12) 4
(10) 3
(13) 2
(5) 1
(6) DP
COLUMNS

FIGURE 10. Functional Diagram of Latch, Driver and Alphanumeric Display Device

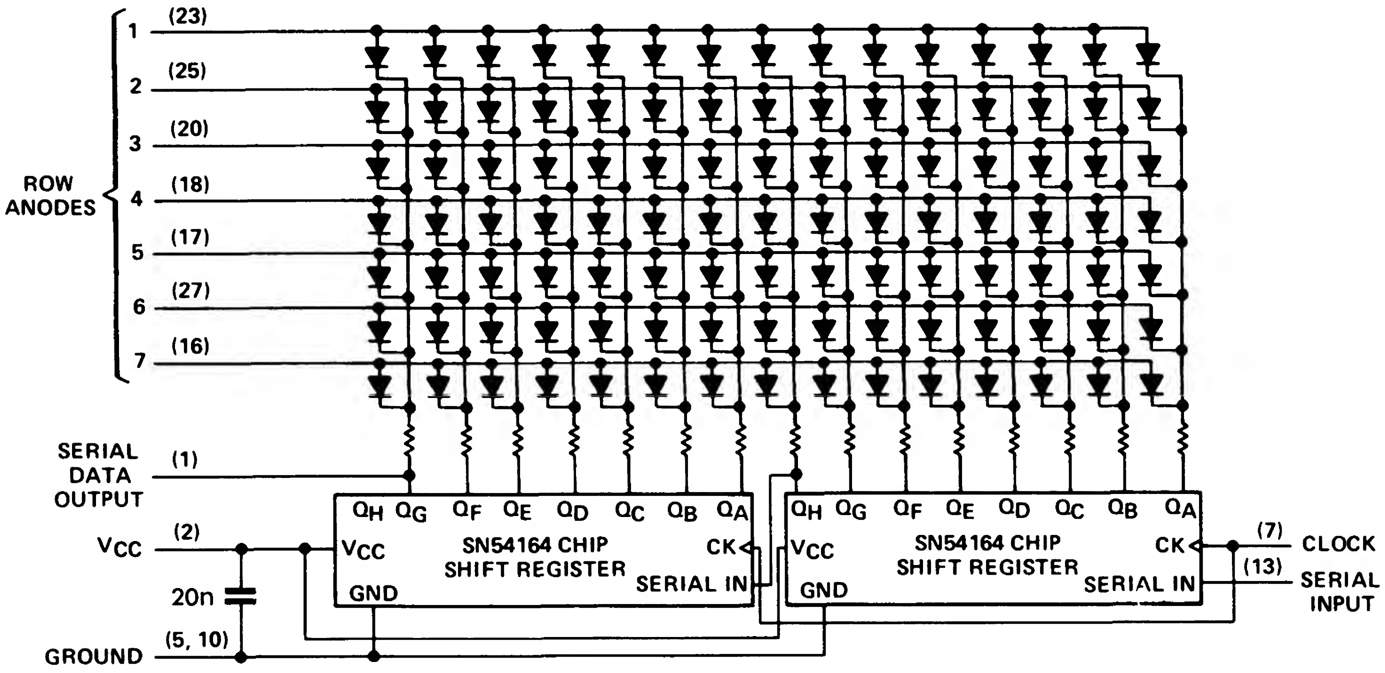
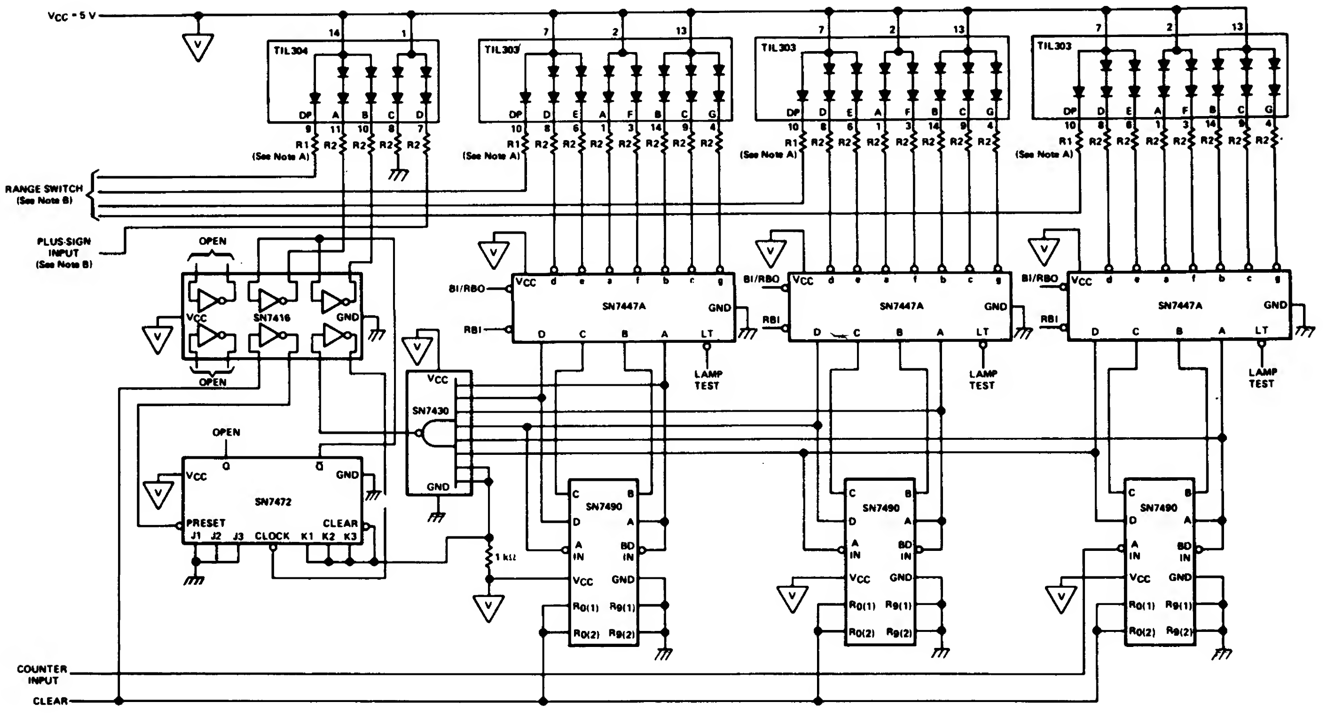

ROW ANODES
1 (23)
2 (25)
3 (20)
4 (18)
5 (17)
6 (27)
7 (16)
SERIAL DATA OUTPUT (1)
VCC (2)
20n
GROUND (5, 10)
QH QG QF QE QD QC QB QA
VCC
SN54164 CHIP SHIFT REGISTER
CK
GND
SERIAL IN
QH QG QF QE QD QC QB QA
VCC
SN54164 CHIP SHIFT REGISTER
CK
GND
SERIAL IN
(7) CLOCK
(13) SERIAL INPUT

FIGURE 11. Schematic Diagram of Shift Register. Driver and Alphanumeric Display Device


VCC = 5 V
TIL304
TIL303
TIL303
TIL303
DP A B C D
DP D E A F B C G
R1 R2
(See Note A)
RANGE SWITCH (See Note B)
PLUS-SIGN INPUT (See Note B)
OPEN
SN7416
VCC
GND
SN7430
SN7447A
BI/RBO
RBI
LT
LAMP TEST
SN7472
PRESET
CLEAR
J1 J2 J3 CLOCK K1 K2 K3
Q
1 kΩ
SN7490
A IN
BD IN
R0(1) R9(1)
R0(2) R9(2)
COUNTER INPUT
CLEAR

NOTES: A. R1 and R2 are selected for desired brightness.
B. Grounding of any of these lines will illuminate the associated function.

▽ ... Vcc

FIGURE 12. 3½ Digit Display Circuit

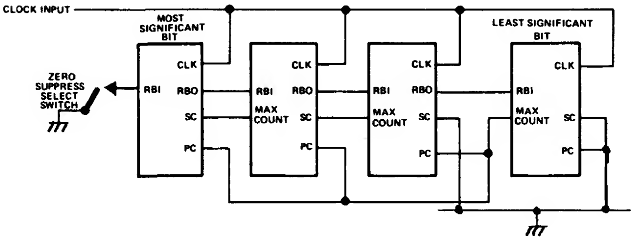

CLOCK INPUT
MOST SIGNIFICANT BIT
LEAST SIGNIFICANT BIT
ZERO SUPPRESS SELECT SWITCH
CLK
RBI
RBO
SC
PC
MAX COUNT

FIGURE 13. Synchronous Count-Mode and High Order Zero Suppression

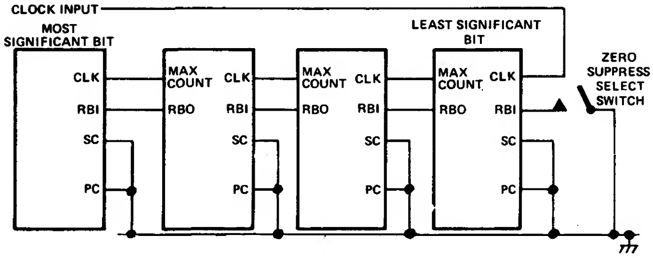

CLOCK INPUT
MOST SIGNIFICANT BIT
LEAST SIGNIFICANT BIT
ZERO SUPPRESS SELECT SWITCH
CLK
RBI
RBO
SC
PC
MAX COUNT

FIGURE 14. Asynchronous Counting Mode and Low Order Zero Suppression

Seven Segment Display/Counters

Figure 13 shows the connections for synchronous counting, with leading zero suppression (ripple blanking) using TIL306 v.l.e.d. seven segment counter/displays. Figure 14 illustrates the connections between similar devices for asynchronous counting and trailing zero suppression. A limiting factor of both these circuits is the fact that the counters in the TIL306 will not count faster than typically 18MHz. (The minimum device specification is 12MHz). The TIL308, however, can be fed from a much faster counter enabling a counter system to work at a much higher frequency.

A b.c.d. counter capable of working a typically 100MHz (minimum specification 80MHz) is shown in Figure 15. It consists of two SN74S112 and one SN74S11 Schottky t.t.l. circuits. The Q outputs of the four flip-flops are fed into one TIL308, resulting in a decade with readout. The following decade position could consist of a TIL306, which is capable of handling the next stage rate. This circuit can be expanded even further by preceeding the Schottky counter with an emitter-coupled logic (e.c.l.) flip-flop stage. This will work at 400MHz toggle rate while using discrete built e.c.l. flip-flops a toggle rate of 800MHz is possible.

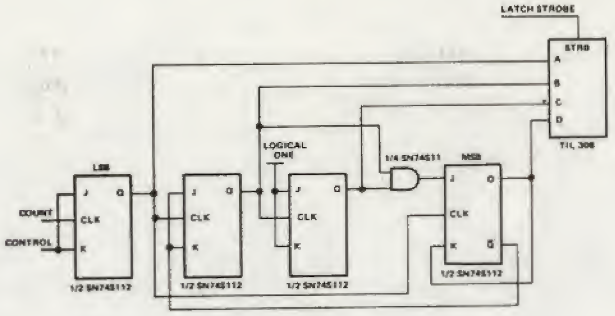

LATCH STROBE
STRB
A
B
C
D
TIL 308
LOGICAL ONE
1/4 SN74S11
MSB
LSB
J
Q
CLK
K
Q̄
COUNT
CONTROL
1/2 SN74S112
1/2 SN74S112
1/2 SN74S112
1/2 SN74S112

FIGURE 15. High Speed Decade Counter

A block diagram of a stage which is capable of counting up to 800MHz is given in Figure 16. Since e.c.l. levels are incompatible with t.t.l. levels, an e.c.l.–t.t.l. converter is necessary. The output of the converter will drive the TIL308 without any interference caused by switching speed problems.

Figure 17 is a block diagram representation of a nine-digit readout, consisting of an e.c.l. decade counter with a TIL308 display and a Schottky t.t.l. decade counter with a TIL308 display, as just described, and seven TIL306 devices.

Figure 18 is a photograph of two counters with identical performance illustrating the difference in the number of components between a conventional counter consisting of SN7490A, SN7475 and SN7447A t.t.l. integrated circuits, resistors, and a display using TIL302 devices, (A); or a counter using TIL306 devices, (B). Both counters are specified to operate up to 15MHz using a six digit readout. The counter using TIL306 devices shows a big empty surface in the middle of the board and considerably fewer connections to the display. The cost savings resulting from using such a counter are obvious.

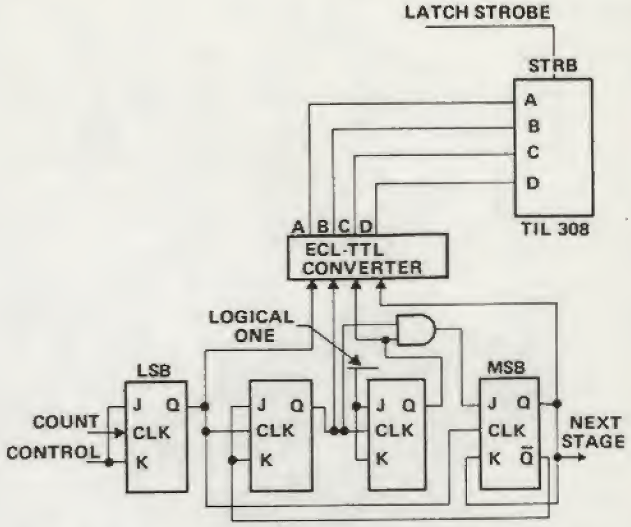

LATCH STROBE
STRB
A
B
C
D
TIL 308
A B C D
ECL-TTL CONVERTER
LOGICAL ONE
LSB
MSB
J Q
CLK
K
K Q̄
COUNT
CONTROL
NEXT STAGE

FIGURE 16. 800MHz Decade Counter Using ECL Logic and a TIL308 Display

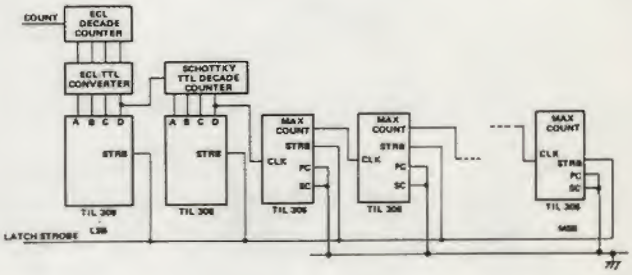

COUNT
ECL DECADE COUNTER
ECL TTL CONVERTER
SCHOTTKY TTL DECADE COUNTER
A B C D
STRB
TIL 308
LSB
MAX COUNT
CLK
PC
SC
TIL 306
MSB
LATCH STROBE

FIGURE 17. Nine Digit Counter

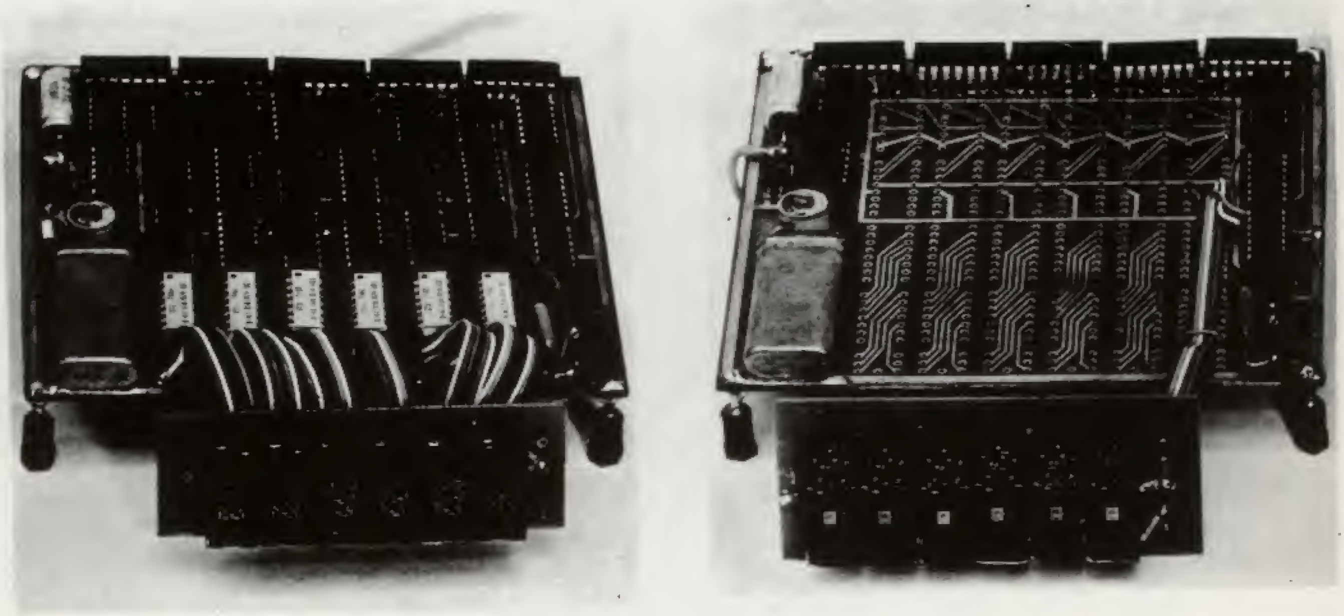


FIGURE 18. Two Counters with Identical Performance

A High Speed Counter

Figure 19 is a photograph of 200MHz counter using seven TIL306 devices and two TIL308 devices. A compact assembly technique reduces the total size. Figure 20 shows all of the basic circuit boards and components used in the counter shown in Figure 19. The upper board is the timebase. The centre board is the control. The bottom board is the counter and the display.

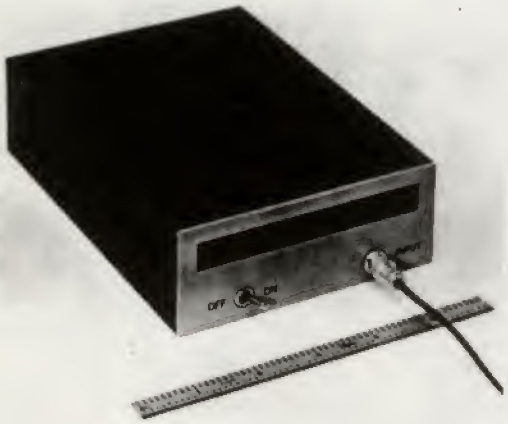


FIGURE 19. A Portable 100MHz Counter

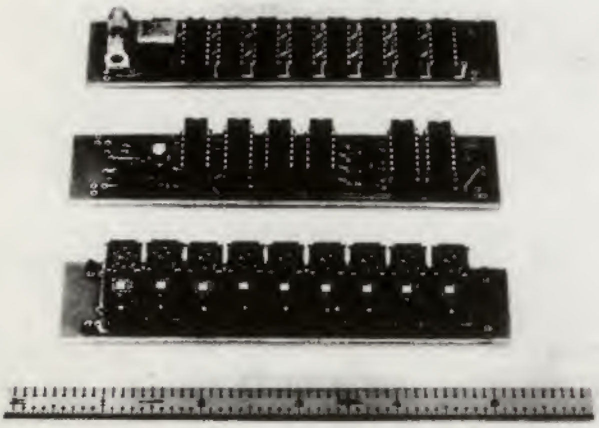


FIGURE 20. Circuit Boards of the Portable Counter

FIGURE 21. Assembly

Figure 21 shows the assembly technique for high density component packing. The total size is 1:2 inches high, 1:2 inches deep and 4.25 inches wide. This counter can be incorporated in a lightweight and portable instrument. Total power dissipation is 9W.

Figure 22 shows a complete schematic of this frequency and time counter incorporating the typically 100MHz stage shown in Figure 15 and seven TIL306 devices. This counter is capable of measuring frequencies up to 100MHz and time with 10 nanosecond resolution. A minimum part count and simplicity are the major objectives. The unit is universal and the counter can be expanded into other functions by adding circuits to the basic building block. The counter has three main functional sections: timebase, control and counter. The top part of the diagram is the timebase. A 10MHz oscillator is formed using two SN74H04 t.t.l. high speed inverters. The output is coupled through a third inverter to isolate the oscillator from the rest of the circuit. Capacitor C1 is a course adjust and capacitor C2 is a fine adjust. C2 should be a variable capacitor that allows fine resolution during adjustment. For more accurate requirements, a separate oscillator in a temperature-controlled oven with an a.g.c. circuit can replace this circuit. The output of the oscillator is fed into a divider chain consisting of eight SN7490A decade dividers. Timing signals from 10MHz to 0·1Hz are generated and switch selectable as the timebase. In the middle of the circuit diagram is the control circuit, which gates the counter and generates the latch strobe and reset signals. The input of flip-flop FF1 is the timebase signal in the frequency measuring mode or the unknown time period in the time measuring mode. With all circuits reset, the $\overline{Q}$ output of flip-flop FF2 holds a high level at the JK inputs of flip-flop FF1. With a pulse coming into the FF1, Q of FF1 changes from a '0' to a '1' on the negative-going edge. This '1' is applied to the first stage of the counter, allowing it to count. Flip-flop FF2 does not change state since it changes only on a negative-going edge. With the next pulse to the clock input of FF1, flip-flop FF1 changes state on the negative-going edge, changing the Q output from logical '1' to logical zero. This negative-going transition sets FF2 and at the same time stops the counter from counting. With FF2 set, $\overline{Q}$ of FF2 is a '0'. A '0' at the JK inputs of FF1 inhibits change with any additional pulses coming into its clock input. The Q output of FF2 is connected to the input of a monostable multivibrator, one half of an SN74123. This multivibrator generates a short positive-going pulse at the Q output. The pulse width is determined by the CR combination R6. C5 and is set in this application to 160ns. The output signal is inverted and applied to the latch strobe inputs of the TIL306 and TIL308 devices. This pulse transfers the data from the counters into the latches to be displayed. The $\overline{Q}$ output of FF2 is connected to the JK inputs of FF1 and also through a resistor to transistor VT1. During counting operation $\overline{Q2}$ is high, turning VT1 'on' and preventing C4 from charging. At the end of the count cycle, the $\overline{Q2}$ is 'low', turning transistor VT1 'off'. The

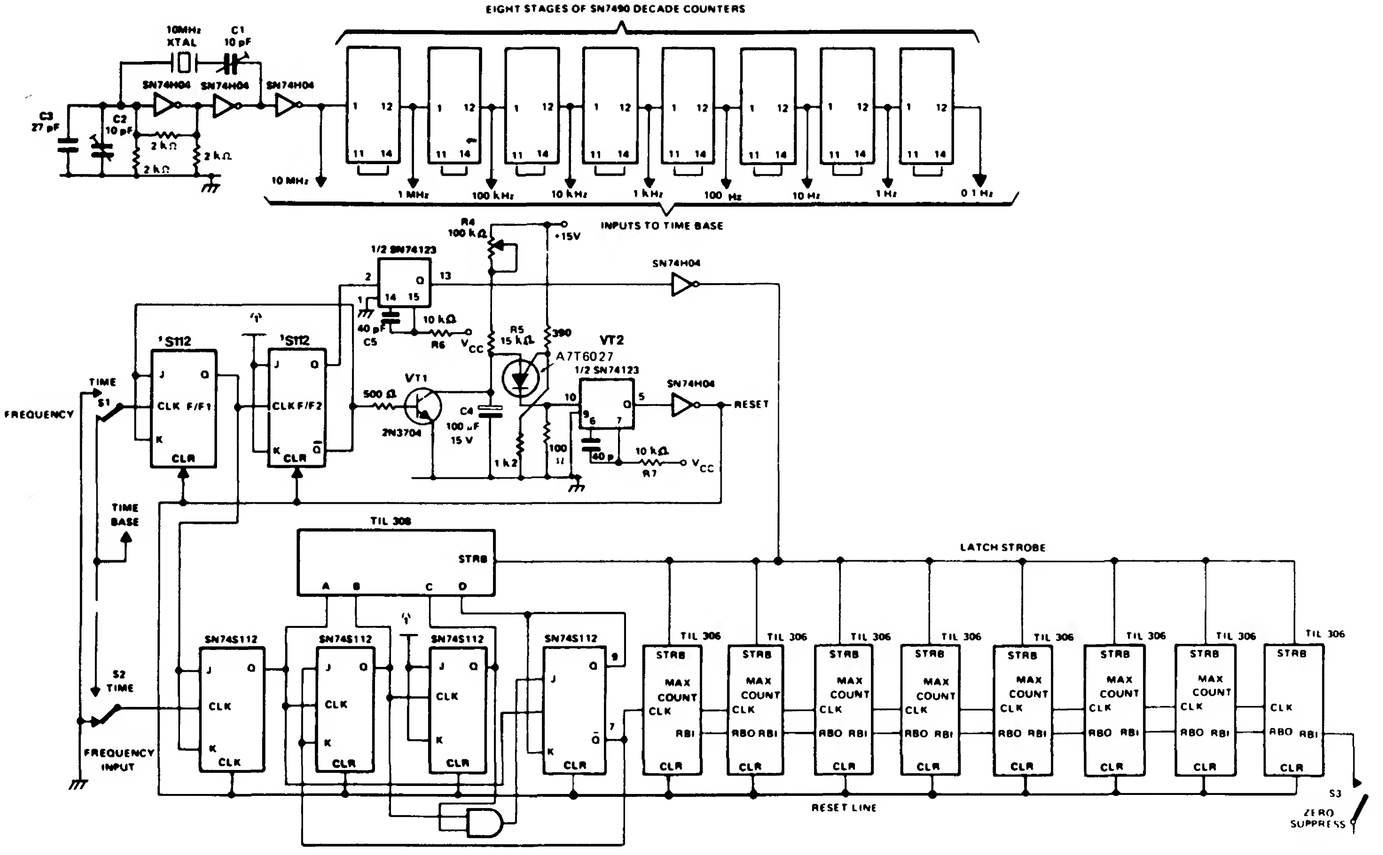

EIGHT STAGES OF SN7490 DECADE COUNTERS
10MHz XTAL
C1 10 pF
C2 10 pF
C3 27 pF
SN74H04
2 kΩ
10 MHz
1 MHz
100 kHz
10 kHz
1 kHz
100 Hz
10 Hz
1 Hz
0.1 Hz
INPUTS TO TIME BASE
R4 100 kΩ
+15V
1/2 SN74123
40 pF C5
10 kΩ R6 VCC
R5 15 kΩ
390
VT2 A7T6027
VT1
500 Ω
2N3704
C4 100 µF 15 V
1 k2
100 Ω
10 kΩ R7 VCC
RESET
'S112
CLK F/F1
CLK F/F2
CLR
TIME
S1
FREQUENCY
TIME BASE
TIL 308
STRB
A B C D
LATCH STROBE
SN74S112
S2 TIME
FREQUENCY INPUT
TIL 306
MAX COUNT
CLK
RBO RBI
RESET LINE
S3
ZERO SUPPRESS

FIGURE 22. Schematic of the Frequency and Time Counter

capacitor C4 begins charging through resistors R4 and R5. Resistor R4 is adjustable and allows a variation in the display time. Resistor R5 prevents the charging current and the current through VT1 from exceeding 1mA when R4 is turned to zero. Once the charge across capacitor C4 reaches the firing potential of the p.u.t. VT2, the p.u.t. generates a positive pulse on its cathode which is coupled into the second monostable multivibrator, the other half of the SN74123. The positive pulse determined by R7. C6, which is 150ns wide, is inverted by an inverter, one sixth of an SN74H04, and applied to the reset input of the TIL306 devices, the four flip-flops of the first counter stage, and the two flip-flops in the control section. With flip-flops FF1 and FF2 reset the JK inputs are reset to a high level by FF2 and the circuit is again ready to handle the incoming signal. The bottom part of the circuit shows the counter section. As described this stage is made up of two SN74S112s one SN74S11, and one TIL308. (An alternative device to use in place of all the Schottky circuits would be the SN74S196). The $\overline{Q}$ output of the fourth flip-flop is connected to the clock input of the first TIL306. The maximum count of the TIL306 is connected to the clock input of the next TIL306. This operation is the asynchronous mode, which is acceptable for counter purposes. The counter is controlled by the two inputs to the first flip-flop of the first decade. The clock input is the unknown frequency in the frequency mode, or the known time pulses from the timebase in the time measuring mode. The JK inputs are connected to the Q output of the control flip-flop. This signal gates the counter. As already explained, a high level to the JK inputs allows the flip-flop to change state on a negative edge of a pulse applied to the clock input. With the JK inputs low, the clock input does not affect the flip-flop. To complete the operation of the counter, the latch strobe and the reset are applied to the circuit as shown. Zero blanking switch S3 allows a choice between suppression or displaying of zeroes to the left of the most significant digit. With the switch closed, a ground is applied to the ripple blanking input of the most significant digit. If this digit is a zero, the display is blanked and the ripple blanking output goes zero. This output is connected to the next digit and the process repeated until all leading zeroes are suppressed. If switch S3 is opened the high order zeroes are displayed. All that is necessary for operation of the counter now is to provide a power supply and a signal to be counted.

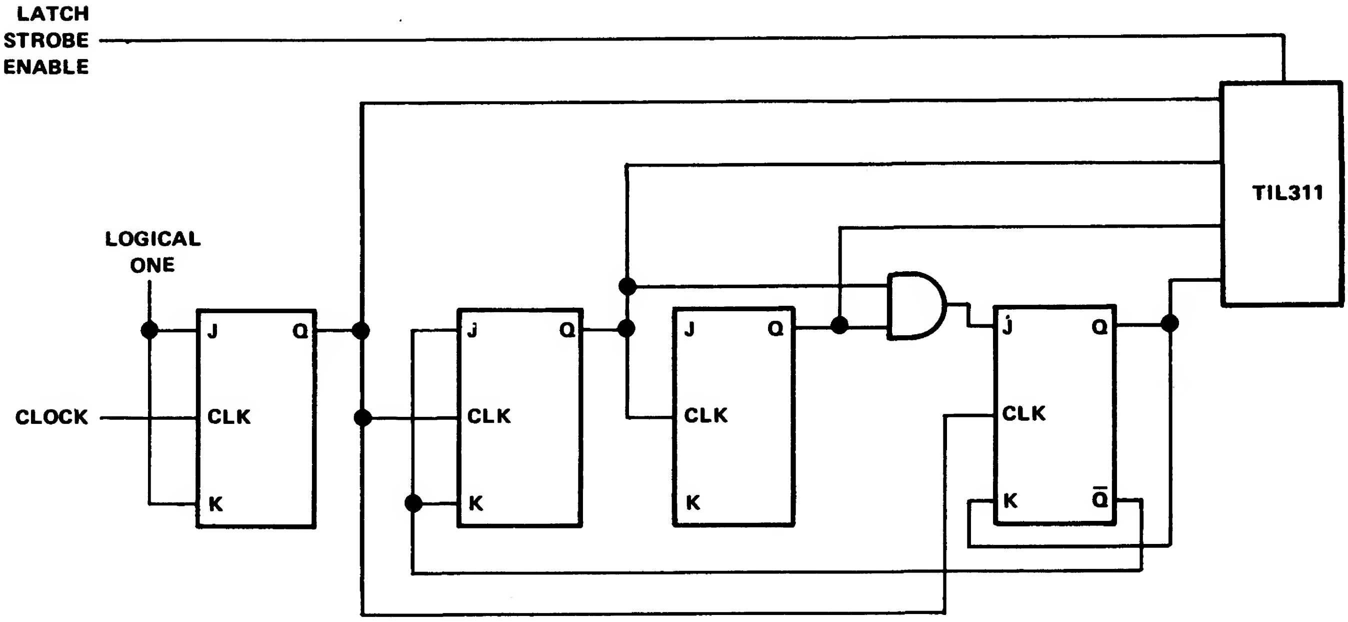


FIGURE 23. Counter Display Using Hexadecimal Device

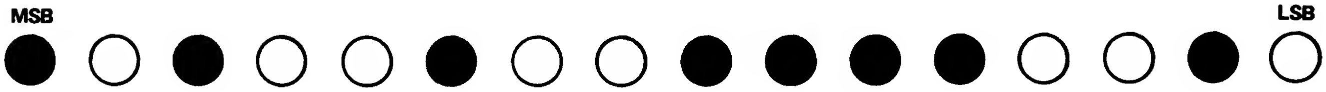


FIGURE 24. Discrete Light Display for a 16-Bit Register

Decimal Counter Display

Figure 23 illustrates the use of the v.l.e.d. hexadecimal display TIL311 as a decimal display. The JK flip-flops are connected as a count-by-ten counter and represent one decade position in a multidecade counter. The four Q outputs of the four flip-flops furnish the data inputs to the TIL311. Normally the LATCH STROBE INPUT will be held 'high' so that the display does not follow the counting. When counting is complete for a given timebase, the LATCH STROBE INPUT is pulsed with a negative going pulse. The new data is then transferred from the decade counter into the latches and displayed. The advantages of using a hexadecimal display are that it gives a better and more pleasing character shape than when using a seven-segment display and there is some redundancy of the diodes so that a single diode failure does not impair the display.

Hexadecimal Indicator

If the register information on, for instance, computer control and service panels is to be displayed, one method could be as shown in Figure 24 using discrete lights. The length of such a display can easily lead to errors in interpretation of the data. Figure 25 illustrates the use of the TIL311 hexadecimal display to give the same data in the same 16-bit register. The 16 register positions are divided into four 4-bit groups. The four bits in each group provide the inputs to each of four TIL311 displays. The resulting four hexadecimal character display provides a more concise interpretation of the register data.

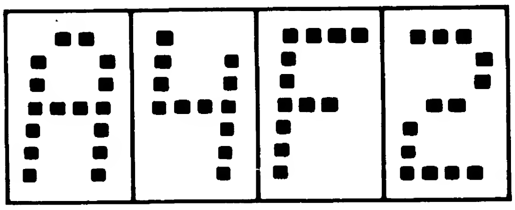


FIGURE 25. Hexadecimal Display for a 16-Bit Register

Table 1. Characteristics of Available Devices

DEVICE	TYPE OF CHARACTER(S)	CHARACTER HEIGHT (INCHES)	COLOR OF DISPLAY	PACKAGE	REMARKS
TIL302 TIL303	7-segment	0.270	Red	14-lead dual-in-line plastic	TIL302—left decimal. TIL303—right decimal.
TIL304	Polarity and overflow unit	0.270	Red	14-lead dual-in-line plastic	Right decimal.
TIL305	5 X 7 alphanumeric	0.300	Red	14-lead dual-in-line plastic	Left decimal.
TIL306 TIL307 TIL308 TIL309	7-segment	0.270	Red	16-lead dual-in-line plastic	Logic in TIL306 and TIL307 includes decade counter, latch, current source driver, and decoder. Logic in TIL308 and TIL309 is same except decade counter not included. TIL306 and TIL308—left decimal. TIL307 and TIL309—right decimal.
TIL311	Hexadecimal	0.270	Red	14-lead dual-in-line plastic	Logic includes latch, decoder, and driver. Left and right decimals.
TIL312 TIL313	7-segment	0.300	Red	14-lead dual-in-line plastic	TIL312 has common anode, right and left decimals. TIL313 has common cathode, right decimal only.
TIL314 TIL315	7-segment	0.300	Green	14-lead dual-in-line plastic	TIL314 has common anode, right and left decimals. TIL315 has common cathode, right decimal only.
TIL316 TIL317	7-segment	0.300	Amber	14-lead dual-in-line plastic	TIL316 has common anode, right and left decimals. TIL317 has common cathode, right decimal only.
TIL321 TIL322	7-segment	0.500	Red	10-lead dual-in-line plastic	Right decimal. TIL321 is common-anode, TIL322 is common-cathode.
TIL323 TIL324	7-segment	0.500	Green	10-lead dual-in-line plastic	Right decimal. TIL323 is common-anode, TIL324 is common-cathode.
TIL325 TIL326	7-segment	0.500	Amber	10-lead dual-in-line plastic	Right decimal. TIL325 is common-anode, TIL326 is common-cathode.
TIL327	Polarity and overflow unit	0.300	Red	14-lead dual-in-line plastic	Left decimal.
TIL328	Polarity and overflow unit	0.300	Green	14-lead dual-in-line plastic	Left decimal.
TIL329	Polarity and overflow unit	0.300	Amber	14-lead dual-in-line plastic	Left decimal.
TIL330	Polarity and overflow unit	0.500	Red	10-lead dual-in-line plastic	Right decimal.
TIL331	Polarity and overflow unit	0.500	Green	10-lead dual-in-line plastic	Right decimal.
TIL332	Polarity and overflow unit	0.500	Amber	10-lead dual-in-line plastic	Right decimal.
TIL361	7-segment	0.500	Red		2-digit display, molded in plastic, mounted on 9-tab printed-circuit board.
TIL362	7-segment	0.500	Green		Same as TIL361 except for color.
TIL363	7-segment	0.500	Amber		Same as TIL361 except for color

(Continued)

DEVICE	TYPE OF CHARACTER(S)	CHARACTER HEIGHT (INCHES)	COLOR OF DISPLAY	PACKAGE	REMARKS
TIL364	7-segment	0.500	Red		4-digit 12-hour clock display with alarm and PM indicators, molded in plastic, mounted on 16-tab printed-circuit board.
TIL365	7-segment	0.500	Green		Same as TIL364 except for color.
TIL366	7-segment	0.500	Amber		Same as TIL364 except for color.
TIL367	7-segment	0.500	Red		Same as TIL364 except without alarm indicator.
TIL368	7-segment	0.500	Green		Same as TIL365 except without alarm indicator.
TIL369	7-segment	0.500	Amber		Same as TIL366 except without alarm indicator.
TIL370	7-segment	0.500	Red		4-digit 24-hour clock display with alarm indicator molded in plastic, mounted on 16-tab printed-circuit board.
TIL371	7-segment	0.500	Green		Same as TIL370 except for color.
TIL372	7-segment	0.500	Amber		Same as TIL370 except for color.
TIL373	7-segment	0.500	Red		Same as TIL370 except without alarm indicator.
TIL374	7-segment	0.500	Green		Same as TIL371 except without alarm indicator.
TIL375	7-segment	0.500	Amber		Same as TIL372 except without alarm indicator.
TIL501	7-segment	0.270	Red	14-lead hermetically sealed dual-in-line	Electrically and mechanically interchangeable with TIL302.
TIL502	7-segment	0.270	Red	14-lead hermetically sealed dual-in-line	Electrically interchangeable with TIL302.
TIL503	7-segment	0.270	Red	14-lead hermetically sealed dual-in-line	Electrically interchangeable with TIL303.
TIL504	5 X 7 alphanumeric	0.300	Red	14-lead hermetically sealed dual-in-line	Electrically interchangeable with TIL305.
TIL505	hexadecimal	0.300	Red	14-lead hermetically sealed dual-in-line	Electrically interchangeable with TIL311.
TIL506	7-segment	0.300	Red	8-lead hermetically sealed	Internal TTL MSI chip with decoder and driver. Left Decimal.
TIL507	5 X 7 alphanumeric	0.300	Red	16-lead hermetically sealed dual-in-line	Integral D-type flip-flop column drivers and series limiting resistors. Left decimal.
TIL508	5 X 7 alphanumeric	0.240	Red	16-lead hermetically sealed dual-in-line	Integral D-type flip-flop column drivers and series limiting resistors. Left and right decimals.
TIL560	5 X 7 alphanumeric	0.500	Red	28-lead hermetically sealed dual-in-line	Three 5 X 7 alphanumeric characters. Logic includes two SN54164 8-bit shift-register chips.

REFERENCE

1. *Semiconductor Circuit Design,* Volume II, Texas Instruments Limited, April 1973, pp 200-201.

ACKNOWLEDGEMENTS

The application circuits are taken from reports by Bert Kehren and Bruce E. Aldridge. Modifications for some of the circuits were provided by David Wilkins.

XVI INTEGRATED INJECTION LOGIC

by
John Read

Integrated Injection Logic (i.i.l. or i^2.l.) has emerged from the laboratory and is appearing in new integrated circuit products[1]. One such product, a microprocessor, is discussed in detail in an earlier chapter. This microprocessor and other i.i.l. designs such as watch circuits, are now in production[2]. Processing for i.i.l. requires only minor variations from bipolar processes already existing for fabrication of either linear i.c.s or Schottky i.c.s. The basic logic gate, however, which is key to i.i.l.'s success, is very different from t.t.l. and is much more like direct-coupled-transistor logic (d.c.t.l.). The size of the basic logic gate is considerably smaller than t.t.l. (see Table 1) while it is almost as fast and consumes considerably less power. With i.i.l. over 2,000 logic gates can be made in a single chip which will operate at a higher frequency than presently available l.s.i. technologies. A further advantage of i.i.l. is that, where nanosecond speeds are not needed, even lower power gates can be used, down to tens of nanowatts per gate, giving a true micropower logic capability.

A wide range of applications is envisaged for i.i.l. from consumer devices such as watches, clocks and circuits for radio and television, in computer applications where the ultimate in speed is not required, to telecommunications equipment where high complexity, low voltage and low power are important. The full extent of the applications introduced by i.i.l. will depend on developments now under way to improve speeds while keeping the present l.s.i. packing density.[3,4]

Table 1. Comparison of TTL and IIL

Parameter	Units	TTL	$\mathrm{I}^2\mathrm{L}$
Gate area	square thou	50	5
Packing density	Gates mm^2	20	120-200
Gate delay	ns/gate	10	25-250
Power dissipation	µW/gate	10,000	0·006-70
Supply voltage	V	3-7	1-7
Logic swing	V	3·5	0.7
Current per/gate	mA	2	10^{-3}-1

EVOLUTION OF THE I.I.L. GATE

The gate has evolved from the d.c.t.l. gate shown in Figure 1. D.c.t.l. had severe problems in small-scale-integration (s.s.i.) systems due to current 'hogging' caused by mismatch of transistor V_{BE}s and was not used extensively. With the matching of V_{BE}s now obtainable across an l.s.i. chip, even across a wafer of i.c.s, such a gate design can be used although operating temperature differences on a chip can still cause problems. However, for straightforward d.c.t.l. as in Figure 1, the load resistor has to be isolated from the transistors forming the switching elements and these in turn have to be isolated from those of each other gate. This isolation diffusion takes up significant area and limits the functional density achievable. Considerable area savings can be made when it is realised that all emitters in the circuit are common and that the transistor bases driven from one d.c.t.l. output are also common sharing the previous load resistor for base drive current. By using an inverted transistor, as shown in Figure 2, one can combine these transistors with common emitters

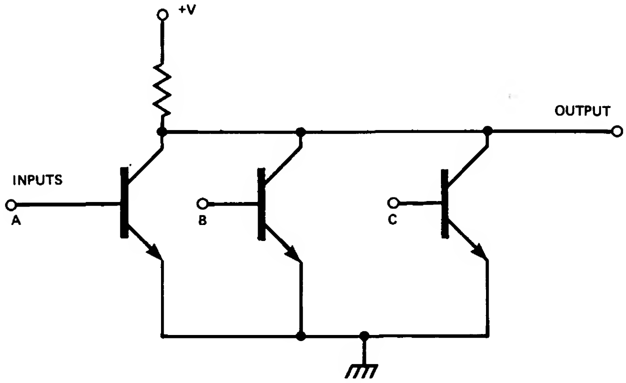


FIGURE 1. D.C.T.L. Gate

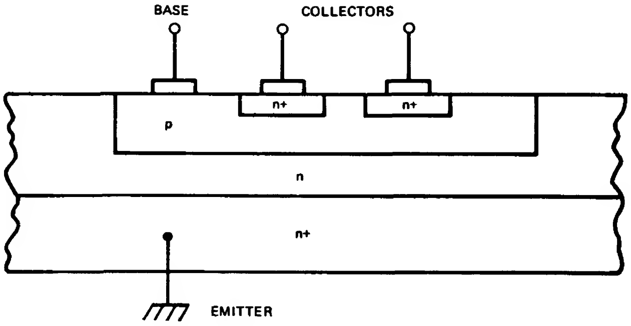


FIGURE 2. Inverted Multi Collector Transistor

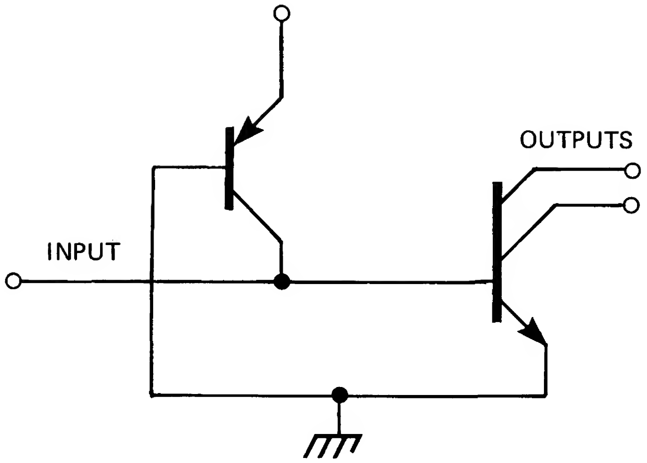


FIGURE 3. Schematic For I.I. L. Gate Structure

and bases into a single multicollector structure and achieve significant increase in functional density. Replacing the load resistor with a lateral pnp current source gives the circuit shown in Figure 3, and removes the need for any of the area-consuming isolation diffusion required in conventional bipolar processes. The new structure is shown in Figure 4. In practice an n+ guard-ring is required to minimise cross-talk between adjacent gates. Because this guard-ring can be very close, or even touch the base of the multicollector transistor, the logic packing density is not compromised.

With the input of the i.i.l. gate of Figure 3 'high' or floating corresponding to the previous gates being 'off', the multicollector transistor is biased 'on' by the pnp current source. Its isolated outputs are then capable of 'sinking' the currents from the current sources at the inputs of the gates to which they are connected. The outputs of all gates are open collectors.

FABRICATION

Non Isolated Process

In Figure 4 the n+ substrate serves as the structural base for fabrication and also as a common ground plane to interconnect all the grounded emitter transistor gates. This eliminates the need for any surface metalisation for ground interconnections. The thin n-type epitaxial layer is both the grounded emitter region of the vertical npn switch and the grounded base region of the lateral pnp. The p-type 'base' diffusion forms the base of the npn, which is also the collector of the pnp, and the emitter of the lateral pnp, known in i.i.l. as the injector. The second diffusion completes the i.i.l. gate by providing the multiple-collector n+ regions of the vertical npn and the guard-ring minimising crosstalk between adjacent gates. Fabrication proceeds by etching the contact holes and then deposition of metallisation followed by etching to define the interconnection pattern.

It is important to note that the lateral pnp is fully integrated into the gate structure and does not exist as a separate component. Further, a single lateral pnp can be used as a current injector for many gates as long as symmetry is maintained so that all gates operate at similar injector current levels.

A number of i.i.l. fabrication techniques are under consideration. The one described is the most common and was used to build the microprocessor described earlier. It is called the non-isolated i.i.l. process because no p-diffusion isolation is required.

Comparison With Isolated Process

With the non-isolated i.i.l. structure, shown in Figure 4, very complex digital i.c.s can be produced; an example, as mentioned, being the microprocessor which has more than

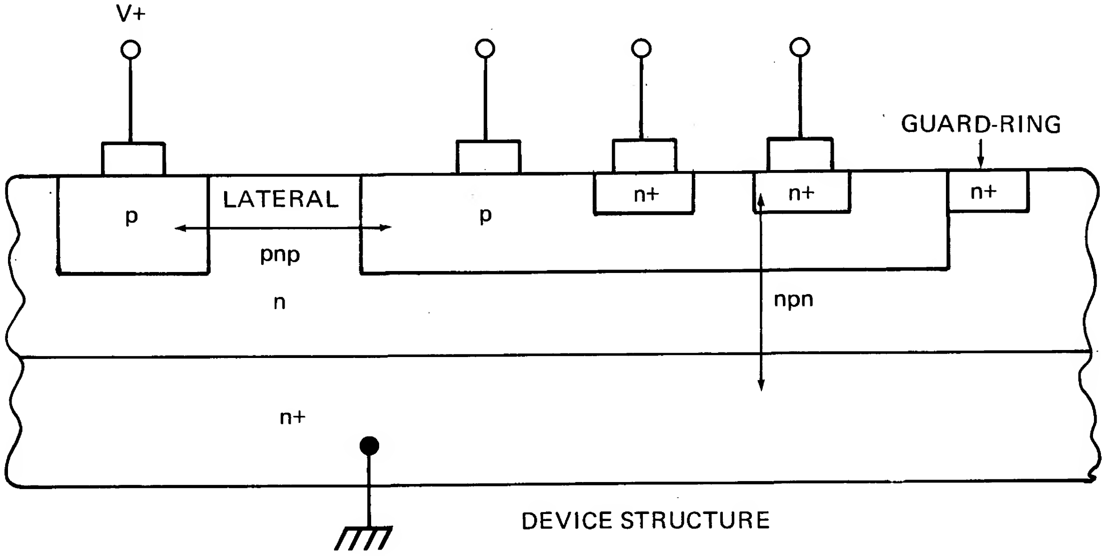
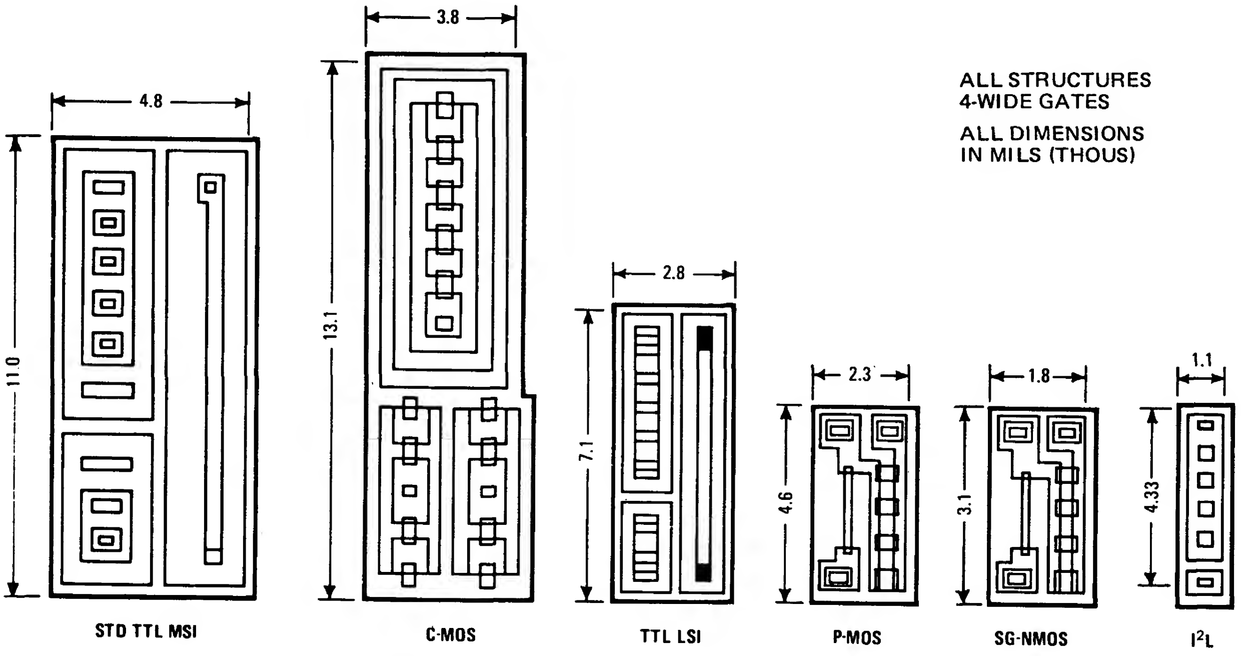


FIGURE 4. I.I.L. Gate Structure

1450 gates. Comparison of the basic gate area with other technologies such as c.m.o.s and t.t.l. shows a tenfold increase in component density. For practical designs due to interconnection area, bonding pads and scribe lines, the area saving may be only a factor of 3 to 4 times. This density combined with nanosecond speeds and microwatt power dissipation makes non-isolated i.i.l. the key candidate for the next generation of digital circuits. However, the processing steps required for i.i.l. are so closely similar to processes used in the manufacture of other non gold-doped products, linear circuits and Schottky t.t.l., that i.i.l. circuit techniques and gates can be combined with these conventional p-n junction-isolated processes to build even more versatile devices. With a linear process the density of isolated i.i.l. can be combined with circuit functions such as operational amplifiers, oscillators, regulators and l.e.d. drivers to make single chip circuits for watches, calculators and a variety of other consumer and industrial products. The combination of isolated i.i.l. with Schottky designs provides higher speed, denser devices than would otherwise be achievable. Examples here are 256 bit r.a.m.s such as the SN74S201 and '301. The process chosen therefore depends on the product requirements. For high-speed, low power, high-density logic the non-isolated, simple four mask process is ideal. For combining logic with analogue circuitry or with ultra high speed t.t.l. a six mask isolated process is used.

Comparison with Other Technologies

The advantages of i.i.l. are shown clearly in Figure 5. The first comparison made is of area, and the unit used for this is a '4-wide' gate, i.e. a four input NAND/NOR gate. (In most technologies a gate has isolated inputs with a single output, but with i.i.l. it has a single input and isolated outputs. Thus a whole gate unit must be used as a basis of comparison). As can be seen i.i.l. is the most economical in area. The process technology comparison shows that i.i.l. is simpler than all other approaches except p-m.o.s., which requires the same number of mask steps, but needs one less diffusion step. Compared with i.i.l., the latest important production m.o.s. process, n-channel depletion load, requires an additional mask step. Although the latter uses one less diffusion than i.i.l., it does require two ion implantations. Compared with t.t.l. and c.m.o.s., the i.i.l. process is extremely simple and the area required is about a factor of ten times less at the basic gate level. Its closest bipolar competitor, collector diffusion isolation (c.d.i.),



GATE AREA (SQ MILS)	52.8	49.8	19.9	10.6	5.6	4.8
NUMBER OF COMPONENTS	3	3	3	2	2	1
MASK STEPS	7	6	7	4	7	4
NUMBER OF DIFFUSIONS	4	3	4	1	3	2

FIGURE 5. Comparison of Different Technologies

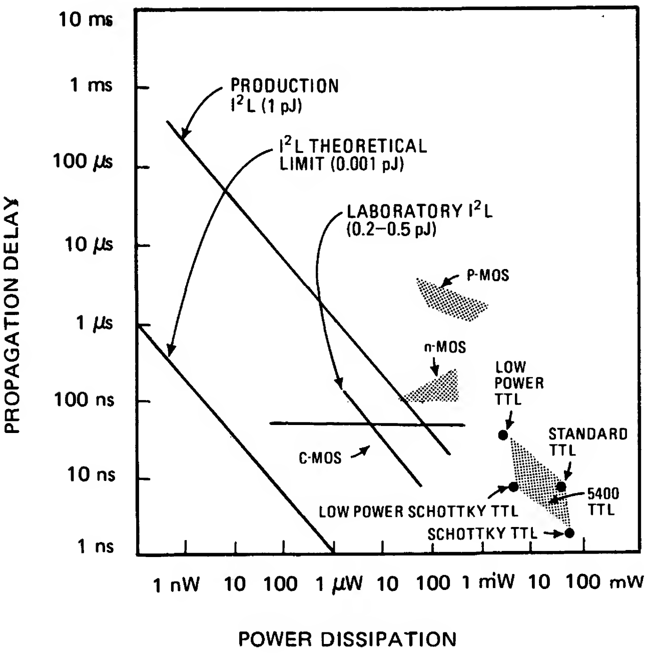


FIGURE 6. Speed-Power Comparison of I.C. Technologies

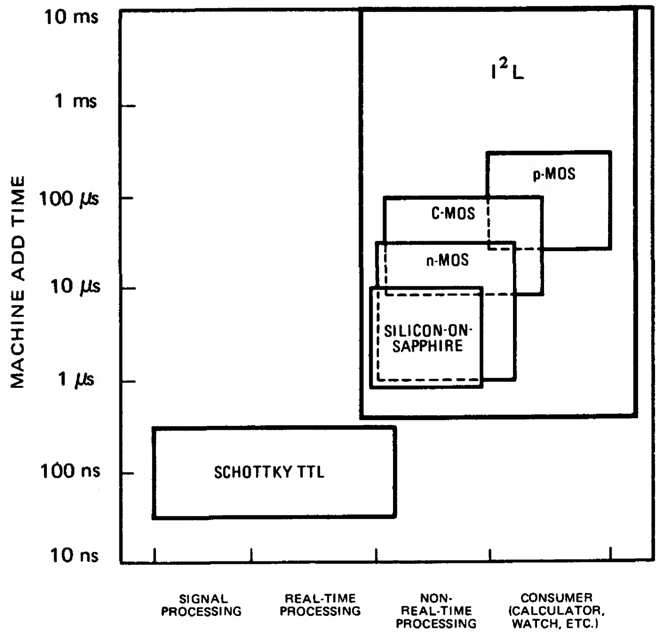


FIGURE 7. Applications Spectrum

although a simple process, takes up considerably more silicon area–similar in fact to that required by the latest forms of t.t.l. l.s.i.

Speed-power comparisons (see Figure 6) show still further advantages for i.i.l. gates–they have the lowest speed-power product of any technology in use today. Non-optimised i.i.l. test bars have operated with 50ns propagation delays with 100nW of power per gate. Optimisation of layout and process can give speeds down below 20ns and with the introduction of new processes currently in development better than 5ns can probably be achieved for very little increase in gate area.

An advantage of i.i.l. is that it can operate over a wide speed range, milliseconds to nanoseconds, and this speed is controlled by the injector current level. In practice this can be used in two ways. First in designs where the total injector current can be controlled by the user with resistors external to the chip he can make a direct trade-off between operating speed and power. Secondly, at the chip design level, the injector currents of gates where short propagation delay are not required can be lower than those needed for high speed. With an isolated process 'on-chip' current regulators can be designed to minimise the total power required by a device. Because of the wide speed range available with i.i.l. by controlling injector current levels this technology is competitive in a wide range of applications. Figure 7 shows where i.i.l. fits into the application spectrum, i.e. it can handle the 50ns speed required for some main frame controller systems to calculator tasks requiring only millisecond add times. Second. generation i.i.l. will significantly extend this capability into higher performance applications.

DESIGN

Digital Circuits

The i.i.l. npn transistor is normally biased 'on' ('low' output) by the lateral pnp transistor injector which is connected between the base of the npn and an external current source. Switching is accomplished by the steering of this injector current. A low input voltage of less than one V_{BE}–approximately 700mV–pulls current from the injector through the 'on' ('low') output of the driving gate. This robs the following gate of its base drive which will turn 'off' with its open-collector output rising to a 'high' logic level, unless held 'low' by another collector with which it is wire-OR ed, as shown in Figure 8. Since the logic functions are achieved by wire-ORing the isolated collector outputs from different gates, a 'high' input logic level is achieved only when inputs of all preceding gates are 'low'. When this happens the injector forward-biases the npn into the 'on' state and produces an output low level equal to one $V_{CE(sat)}$ above ground. For an i.i.l. transistor with high inverse gain this is typically 5-10mV. Internal i.i.l. logic swings are nearly 700mV–from $V_{CE(sat)}$ of only a few mV to a V_{BE} of 700mV.

Figure 9 shows how i.i.l. gates are interconnected to make a D-type flip-flop (bistable multivibrator). Figure 9(a) shows how this circuit is made with standard NAND gates while 9(b) shows how the same circuit is implemented in i.i.l. The injector is shown on only one gate, but all six gates have injectors. The injectors of the other gates are left off the circuit schematic for convenience. In fact, one common injector rail is used, as can be seen in the layout shown in

Figure 9(c). A D-type flip-flop as shown in Figure 9(c) covers only an area of 18·4 square thou. when constructed in i.i.l.. In t.t.l. or c.m.o.s. a similar function would use from 120 to 200 square thou.. Other logic functions are performed in i.i.l. with the same economy of area.

Input/Output Buffers

It is not generally practical to bring i.i.l. gate inputs or outputs direct to the package pins because the gates operate at low current levels with only 700mV signal swing, which does not match with other logic i.c.s. To achieve good noise immunity and high output drive capacity buffers are therefore included to interface with t.t.l. or l.e.d.s, synchronous motors, etc. as demanded by the application. With the non-isolated process, as used for the microprocessor, the most useful interfaces are resistor transistor logic (r.t.l.) inputs modified for t.t.l. compatability, and open-collector outputs–see Figure 10. The i.i.l. input and output characteristics are shown in Figure 11. As

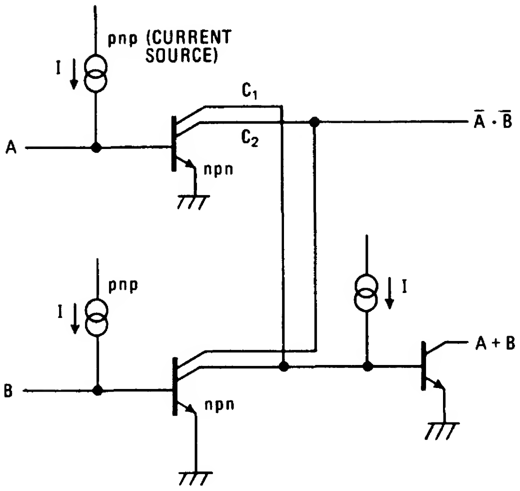
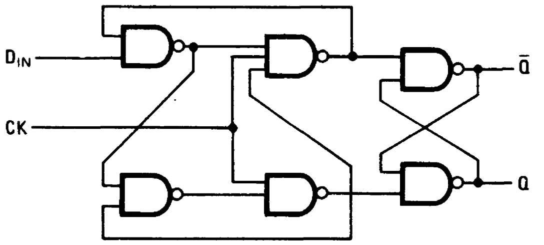
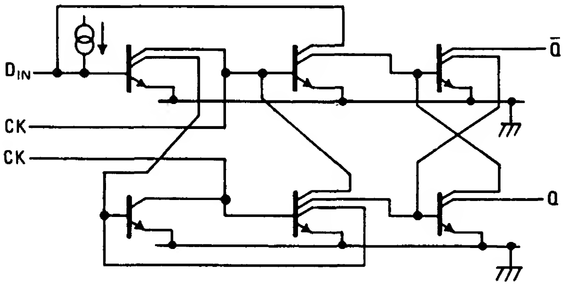


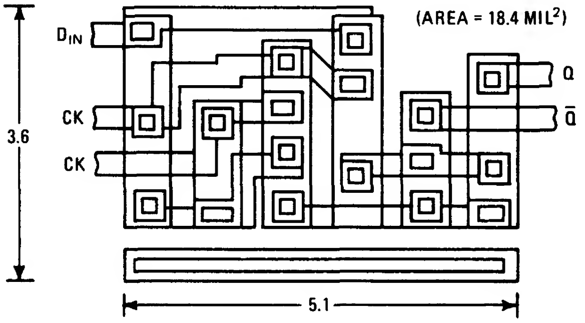
FIGURE 8. Logic with I.I.L.



(a) D-TYPE FLIP FLOP USING STANDARD GATES

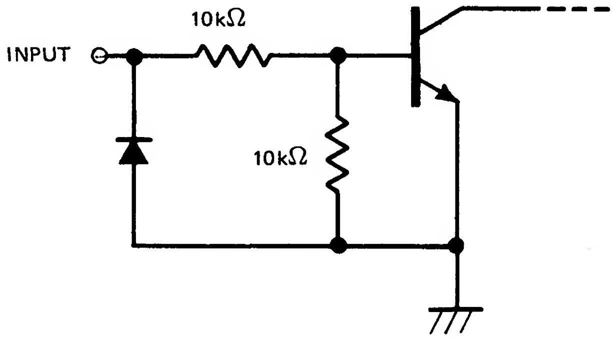


(b) D-TYPE FLIP FLOP USING I.I.L. GATES

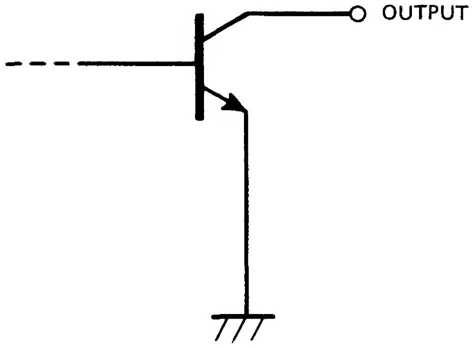


(c) I.I.L. LAYOUT

FIGURE 9. Construction of a D-Type 'Flip-Flop'

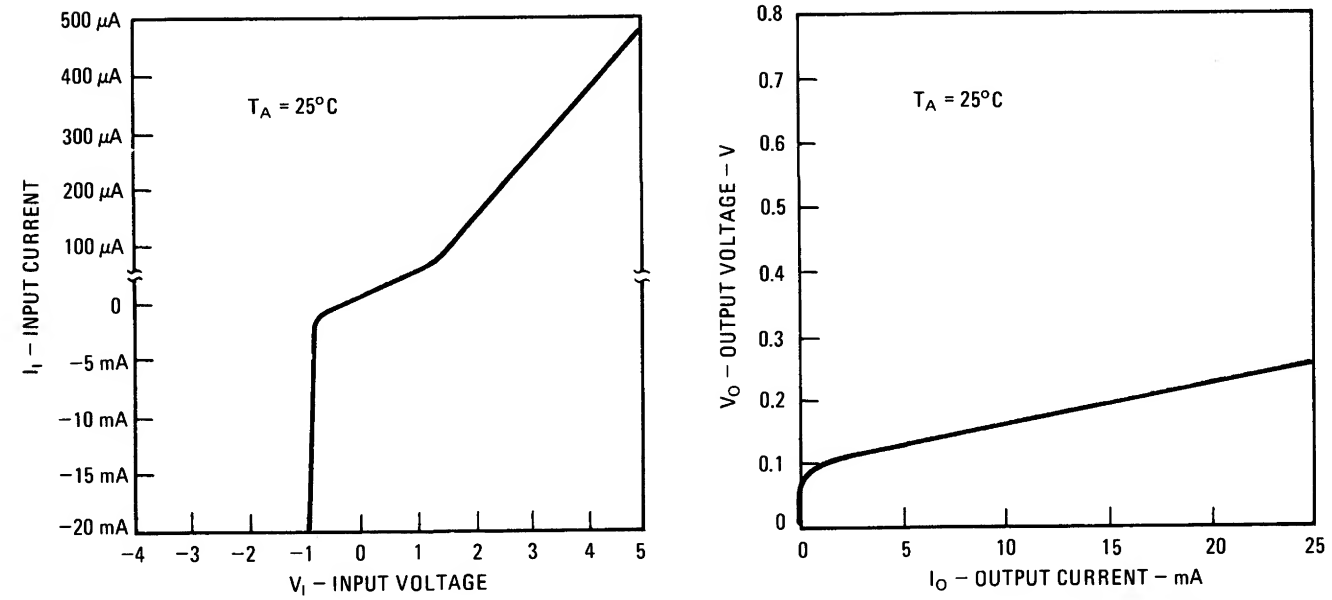


(a) INPUT BUFFER



(b) OPEN COLLECTOR OUTPUT

FIGURE 10. T.T.L. Compatible Interface Circuits for I.I.L.



(a). INPUT CURRENT vs INPUT VOLTAGE

(b) OUTPUT VOLTAGE vs OUTPUT CURRENT

FIGURE 11. I.I.L. Input and Output Characteristics

stated, with an isolated process it is possible to design the t.t.l. interface circuits as illustrated in Figures 12 and 13. The input buffer is extremely compact, particularly because the multi-emitter input transistor only occupies the area of one isolated transistor. A t.t.l. compatible output buffer is somewhat more complex. For the circuit shown in Figure 13, current amplification stages are required to provide the necessary current 'switching' capability, since the internal gates themselves are operating at very low current levels.

Other output buffer configurations may be used depending on the voltage and current requirements at the outputs. In particular, if stand-off voltages of more than about 7V are required it is generally necessary to use a lateral pnp at the output as these devices have considerably higher break-down voltage typically in the range of 30 to 40 volts. Output current sink capability has to be sacrificed as the current gains of the lateral pnps are low and peak gain occurs at relatively low current levels–i.e. a few mA maximum.

POWER SUPPLIES

From the power supply terminals an i.i.l. gate looks like a silicon diode–the injector diode. For circuits made with the non-isolated process the total current required is the sum of all the injector currents. Thus any supply capable of sourcing the required current at a voltage of 800mV or greater will be satisfactory. For some applications this will be a dry cell battery–i.i.l. is an ideal technology for circuits to operate where a single dry cell can be used. In most cases the supply required will be dictated by other circuit components, l.e.d.s, t.t.l. etc. In such cases a dropping resistor will be required and its value can be simply calculated. Where the isolated process is used, 'on-chip' regulation can be designed such that a chip can be driven directly from, say, t.t.l. supplies eliminating the need for an external resistor. Use of 'on-chip' supply regulation also gives the chip designer flexibility to run parts of a circuit at different injector current levels as dictated by the speed requirements of the particular logic functions. Alternatively all injectors would have to be run at the same level as that required by the fastest gate in the system, in which case a significant percentage of the power could be wasted. This may not be generally important because of the

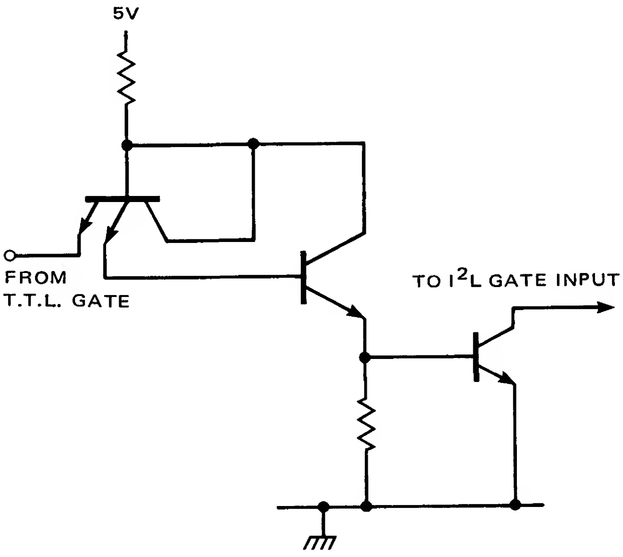


FIGURE 12. T.T.L. Input Buffer for I.I.L. Circuit

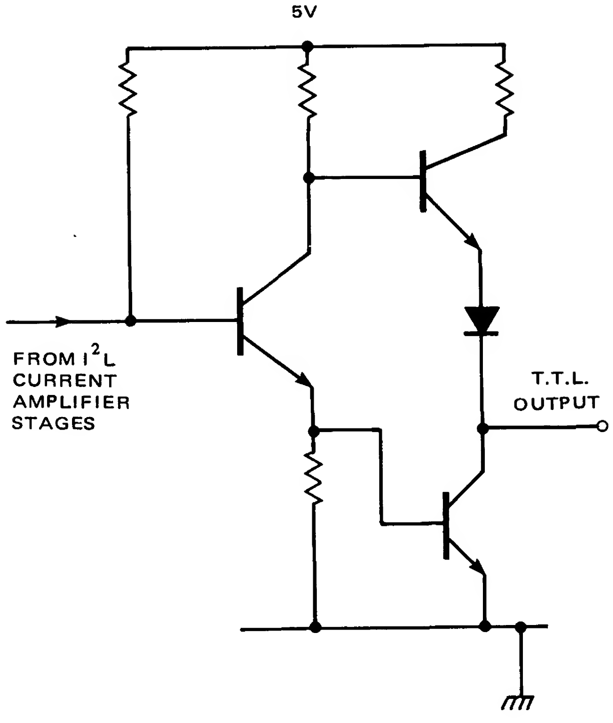


FIGURE 13. T.T.L. Output Buffer for I.I.L. Circuit

extremely low power per gate required, but in battery powered applications it could be critical. The cost of this feature is the added processing complexity required for the isolated process but is justified where parts of a single circuit have significantly different speed requirements. For example a clock divider may require initial divide stages to operate at frequencies of several MHz, taking 100μA or so per stage; whilst the lower order stages would run at a few hundred Hz, which would only require currents of the order of nA.

APPLICATIONS

Integrated Injection Logic can be applied to a wide range of products now made in m.o.s., c.m.o.s. and even t.t.l. Its first applications however, will be to products where the unique advantages of i.i.l. can be utilised–low voltage operation, high speed at low power or where a mixture of digital and linear circuitry on one chip are needed. The microprocessor, for example, is an application where the speed of i.i.l. gives a significant advantage over m.o.s. devices now available. Consumer products such as watches and clocks, where operation from one or two dry cells at low power is a key advantage, may also be expected to be early applications.

The technology will also be important in many places where c.m.o.s. and low-power t.t.l. are now being used. Its speed-power characteristics compare favourably with each and greater functional density per unit silicon area can be achieved leading to lower costs. The full extent to which this technology and derivatives of it will be used will probably depend on current development work. Increased speed may be achieved with ion-implanted devices or Schottky clamps–many variations are presently being studied. If standard t.t.l. speeds or better can be achieved with i.i.l. packing density then a major advance in bipolar integrated circuits will shortly occur.

REFERENCES

1. C.M. Hart, A. Slob and H.E.J. Wulms; 'Bipolar L.S.I. takes new direction with integrated injection logic', *Electronics*, October 3rd 1974. Vol. 47. No. 20, pp.111-118.

2. R. L. Horton, J. Englade, J. McGee; 'I^2 L takes bipolar integration a significant step forward', *Electronics*, February 6th 1975, Vol. 48. No. 3, pp.83-90.

3 Peltier, A. W.; 'A New Approach to Bipolar LSI:C^3 L.' *1975 IEEE International Solid-State Circuits Conference Abstracts* pp 168-169.

4 Berger, H. H. and Wiedman, S. K., 'Schottky Transistor Logic.' *1975 IEEE ISSCC Abstracts* pp 172-173.

Index

- Accumulator, 125, 131–137, 162–165
- Acquisition system, digital data, 162–165
- Addition and subtraction, 173
- Address:
  - bus, 107–115
  - multiplexer, 163–165
  - register, 117, 126–129
- Algorithm:
  - development flowchart, 120
  - for binary division, 137
  - for binary multiplication, 133
- Alphanumeric displays, 191, 196–197
- Amplifier:
  - audio, use of, 97
  - function control/selection, 87–89
  - operational, use of, 92
- Analysis:
  - of waveforms, 32–33
  - transient, 33–34
- Architecture, microcomputer, 104, 116–117
- Arithmetic:
  - instruction, 126
  - logic unit (a.l.u.), 103–116, 117, 125–127, 128–132
  - operations, 170–176
  - shifting, 131–134
- Astable multivibrator, 43–44
- Audio amplifier:
  - function control/selection, 87–89
  - use of, 97
- Avalanche rectifiers, series operation, 15

- Bandpass filter, 92
- Base current:
  - control of, 29
  - measurement, 30
- Binary and decimal rate multiplier:
  - arithmetic operations, 170–176
  - cascading, 170
  - device implementation, 168–170
  - mathematical operations, 176–180
  - principles, 167–182
- Binary-coded decimal addition subroutine, 121
- Binary:
  - division, 136–137, 171–172
  - multiplication, 133–135, 171–172
- Biphase circuit, 1–2
- Bistable multivibrator, 58, 61, 209
- Bounce eleminator circuit, 45
- Bridge:
  - centre-tapped circuit, 2, 14
  - circuit, 2, 14
  - design, three phase, 16–22
  - voltage doubler, 3
- Buffer memory, 148–149
- Burst firing, 91

- Capacitor input filter, 4–11
- Cascading:
  - microprocessors, 109
  - priority encoders, 184–185
  - rate multipliers, 170
  - switching mode sections, 65–67
- Centre-tap:
  - transformer circuit, 1–2, 8
  - bridge circuit, 2, 14
- Character generator, 142–144
- Characteristics:
  - high voltage switching transistors, 23–24
  - i^2l input and output, 209–210
  - programmable unijunction transistors, 35–39
- Check bit generator, 141
- Checking information, 140–142
- Choke input filter, 11–12
- Chopper power supplies, shunt, 50–51, 51–55, 65, 68–71
- Clock generation, 159–160
- Cockcroft-Walton circuit, 3–4
- Code, Hamming, 140–142
- Combined function generation, 145
- Comparator, 66, 139–140, 164–165, 187–188
- Computer, micro:
  - concepts of, 103
  - one-chip, 116–123
  - Schottky t.t.l., 125–137
  - 16 bit system, 114–115
- Conductivity modulation, 23, 28
- Construction:
  - high voltage switching transistors, 23–24
  - programmable unijunction transistors, 35
  - visible light emitting diodes, 191
- Control:
  - base current, 29
  - channel, 82, 88–90
  - chopper supply, 52–53
  - heating element, 84–86
  - high current supply, 61–62
  - instructions, 126
  - light/fan, 86
  - logic, 135
  - program, 110
  - psychedelic lights, 91–100
  - r.o.m., 114–115, 125–130, 136
  - switching mode power supply, 73–74
  - u.a.r.t., 155–156
- Controller, terminal, 122–123
- Conversion, digital to analogue, 186–188

- Converter:
  - /inverter systems, 47–64
  - isolated multiple output, 51–55
  - shunt switching, 25V, 50–51
  - shunt switching, 220V, 65
  - sinewave, 56
  - single saturating transformer, 55–56
  - two transformer, 66
  - −12V (from 5V), 160–162
  - 30V, 120W, 48–49
- Counter:
  - asynchronous, 198
  - decade, 198–199
  - decimal display, 202
  - high speed, 200–201
  - in keyboard encoder, 185–186
  - nine digit, 199
  - synchronous, 198
  - with v.l.e.d.s, 191–204
- Critical inductance, 11
- Crystal oscillator, 159–160, 200–201
- Current:
  - fault, 18–22
  - high supply, 60–63

- Darlington transistor, use of, 59–60, 62
- Data:
  - digital acquisition system, 162–165
  - flow, double precision shift, 110–112
  - input and output, 118
  - maps, r.a.m., 120–122
  - memory, 103, 117, 126, 130
  - multiplexer, 164–165
  - register, 107–109, 117
- Decoder, v.l.e.d., 191–194
- Decoding, instruction, 110–112
- Delay circuits, 45, 201
- Design:
  - i^2l, 208–210
  - switching mode power supply, 68–77
  - three phase bridge, 16–22
- Detector, zero crossing, 45–46, 91
- Diametric connection, 13
- Digital:
  - data acquisition system, 162–165
  - processing techniques, 107–211
  - to analogue converters, 186–188
- Direct-coupled-transistor logic (d.c.t.l.), 205
- Display:
  - alphanumeric, 191, 196–197
  - decimal counter, 202
  - diode (light emitting), 80–81, 85, 87
  - hexadecimal, 191, 194–196, 202–204
  - seven segment, 122–123, 191–194, 196–201
- Dissipation:
  - circuit total loss method, 31–33
  - substitution method, 31
  - transistor, 68–71
- Division, 136–137, 171–172
- Double precision shift data flow, 110–112
- Double star circuit, 13
- Doubler, voltage, 2–3, 8–9, 14
- Driver:
  - stage, 67, 72–73
  - v.l.e.d., 191–194, 196
- Driving:
  - microprocessor, 113
  - one chip microcomputer, 118

- Efficiency, 19–22
- Element, heating, control of, 84–86
- Emitting, visible light, 80–81, 85, 87, 191–204
- Encoder:
  - keyboard, 185–186
  - priority, 183–186
- Error:
  - amplifier stage, 53, 66
  - checking and correcting, 141–142
- Expansion, encoder, 184–185

- Fabrication, i^2l, 206–208
- Factor, power, 19–22
- Fan control, 86
- Fault current, 18–22
- Field effect transistor, use of, 79–81
- Filter:
  - bandpass, 92
  - capacitor input, 4–11
  - choke input, 11–12
  - circuits, 92–93
  - highpass, rumble, 88–89, 92
  - lowpass, scratch, 88–89, 92
  - selection circuits, 87–89
- Firing, burst, 91
- Flags, 131, 154–155
- Flip-Flop, 58, 61, 209
- Flowchart:
  - algorithm development, 120
  - machine instruction, 120, 121
  - u.a.r.t., 157
- Fluorescent lamp inverter, 47
- Frequency:
  - counter, 200–201
  - ratio discriminator, 176
- Full wave rectifier, 1–22
- Function generators:
  - rate multiplier, 174–180
  - triangular, precision, 188–189

- Gates, 60–61, 205–210
- Generator:
  - character, 142–144
  - check bit, 141
  - combined function, 145
  - non integer roots, 174
  - pulse, 39–44
  - p.n.g., use of, 187–188
  - sine and cosine, 177
  - square roots, 173–174
  - triangular function, 188–189
  - vector, 178–180

- Half wave rectifier, 1, 6–10, 13
- Half waving, of triac, 86
- Hamming code, 140–142
- Heating element control, 84–86

Hexadecimal displays, 191, 194–196, 202–204
High current (40A) supply, 60–63
High voltage:
  rectifiers, 14–22
  stacks, 15–22
  switching transistors, 23–34
  supply (14kV), 55–56
High speed counter, 200–201

Indicator, hexadecimal, 202
Inductance, critical, 11
Infinite reactance theory, 16–18
Information checking, 140–142
Input:
  characteristics, i^2l, 209–210
  data, 118
  equivalent, 113
  filter, capacitor and choke, 4–12
Instruction:
  arithmetic, 126
  control, 126
  decoding, 110–112
  machine flow, 121
  macro-, 104, 106
  memory, 125, 128–129, 136
  set, 118–119
  sequencing, 112–113
Integrated circuit:
  channel select, 82
  control, 73–74
Integrated injection logic (i^2l, or i.i.l.):
  application, 107–115, 211
  design, 208–210
  fabrication, 206–208
  gate evolution, 205–206
  power supplies, 113, 210–211
Integration, 176–177
Interconnection, psychedelic lights, 94–98
Interference, suppression, radio frequency, 89
Inverter:
  /converter systems, 47–64
  fluorescent lamp (13W), 47
  push-pull, driver, 57–64
  push-pull, self oscillating, 55–56
  single-ended, driver, 50–55
  single-ended, self oscillating, 47–49
  50Hz, 12-240V, 300W, 57–60
Isolated process, i^2l, 206–208

Keyboard encoders, 185–186

Lamp dimming, 98–99
Light:
  control, 79–86
  emitting diodes, 80–81, 85, 87
  /fan control, 86
  psychedelic, control, 91–100
Line output circuit, 25–27, 30–34
Locator, reference mark, 147–151
Logic array, programmable, 104–105
Logic unit, arithmetic (a.l.u.), 103–106, 117, 125–127, 128–132
Lowpass filter, 88–89, 92
Low power transistor-transistor logic, use of, 60–62
Low voltage wiring system, 81, 83–84

Machine instruction flowchart, 120–121
Macroinstruction, 104, 106
Mathematical operations, 176–180
Measurement:
  parameter, 29
  procedure, 30–31
  system, 29–30
Memory:
  buffer, 148–149
  data, 103, 117, 126, 130
  instruction, 125, 128–129, 136
  program, 103, 117
  programmable read only (p.r.o.m.), 103, 139–145
  random access (r.a.m.), 103–116, 120–122, 148–151
  read only (r.o.m.), 114–115, 125–130, 136
Microcomputer:
  concepts, 103
  one chip, 116–123
  Schottky, t.t.l., 125–137
  16 bit system, 114–115
Microprocessor:
  application, 103–123
  fast, 125–131
  types, 104–106
  4 bit slice element, 107–113
Microprogramming, 104–105
Modulation, conductivity, 23, 28
Modulator, pulse width, 52–53
Monostable multivibrator, 45, 59–61
Multiple-collector transistor, 205–206
Multiplexer:
  address, 163–165
  data, 164–165
  flag, 130
  keyboard encoder, 185–186
Multiplication, 133–135, 171–172
Multiplier:
  binary and decimal rate, 167–182
  voltage, 2–5
Multivibrator:
  astable, 43–44
  bistable, 58, 61, 209
  monostable, 45, 59–61

Nine digit counter, 199
Non integer roots, 174
Non isolated i^2l process, 206–208
Numeric displays, 191–204

Operational amplifier, use of, 92
Operations:
  arithmetic, 171–176
  mathematical, 176–182
Optically coupled isolators, 66, 86
Oscillator:
  crystal, 159–160, 200–201
  discrete, 52
  i.c., 52–53, 66–67
  internal microcomputer connection, 118
  low I_P, high I_V, 43
  relaxation, 39–44, 50–51, 58, 61
  temperature compensated, 43
  voltage controlled, 46

Output:
  characteristics, i^2l, 209–210
  equivalent, 113
  data, 118
  transistor, 68–71
Overload protection, 61, 63

Parameter:
  definition p.u.t., 39
  measurement, 29
Peak point current/voltage, 35–39
Peripheral circuits, 183–189
Pick up voltage, 79, 83, 85
Power:
  control, 1–100
  control/touch switch, 79–90
  factor, 19–22
  supply, mains, 9–11, 63, 65, 94
  supply, switching mode, 48–49, 55–56, 60–63, 65–77
Priority encoders, 183–186
Printed circuit board, 95–96
Process, i^2l, 206–208
Processing techniques, digital, 101–211
Processor, micro-, 103–123
Programmable:
  logic array (p.l.a.), 104–105
  sequence timer, 139–140
Programmable read only memory (p.r.o.m.), use of, 114–115, 125–130, 136
Programmable unijunction transistor (p.u.t.):
  applications, 39–46, 50–51, 58, 61, 201
  characteristics, 35–39
  construction, 35
  definition of parameters, 39
Program memory, 103, 117
Protection, 20, 22, 61, 63
Psychedelic lights,
  control, 91–100
  filters, 92–93
  interconnections, 94–98
  zero voltage switching, 91, 94–96
Pulse:
  generator, 39–44, 50–51, 58, 61, 201
  width comparator, 61
  width modulator, 52–54
Pseudo-random number generator, use of, 187–188
Push-pull inverter/converters, 55–56, 57–64

Quadrupler, voltage, 3–4

Radio frequency interference suppression, 99
Random access memory (r.a.m.), 103–116, 120–122, 148–151
Rate multiplier:
  arithmetic operations, 171–176
  cascading, 170
  device implementation, 168–170
  mathematical operations, 176–182
  principles, 167–168
Ratio, frequency, 176
Ratings, transistor, 27–28
Read only memory (r.o.m.), 114–115, 125–130, 136
Reed relay, 80–81, 84–86
Receiver section of u.a.r.t., 154–155
Rectifier:
  avalanche, serial operation, 15
  full wave, 1–22
  half wave, 1, 6–10, 13
  high voltage, 14–22
  parallel operation, 15
  single phase, 1–12
  stacks, 15, 22
  three phase, 13–22
  use of, 1–22, 47–63
Reference mark locator, 147–151
Relay, reed, 80–81, 84–86
Relaxation oscillator, 39–44, 50–51, 58, 61
Register:
  address, 117, 126–129
  data, 107–109, 117
  working, 130–131
  16 bit display, 202
Ripple blanking, 198
Rotating vector generation, 178–180
Rumble filter, 88–89, 92

Saturating transformer converter, 55–56
Schottky chip set microcomputer, 106, 125–137
Scratch filter, 88–89, 92
Selector, 164–165
Sequence timer, programmable, 139–140
Set, instruction, 118–119, 126–129
Seven segment displays, 122–123, 191–194, 106–20
Shifting, arithmetic, 131–134
Sine and cosine generation, 177
Sinewave converter, 56
Software, 104, 126
Speed-power product, 208
Square rooting, 173–174
Subtraction, 173
Suppression, r.f.i., 99
Switchbounce eliminator circuit, 45
Switching mode power supplies:
  cascaded, 65–67
  single device, 68–77
Switching, zero voltage, 45–46, 91
Synchronous counter, 198
System timing generation, 139–140

Temperature compensated oscillator, 43
Terminal controller, 122–123
Three phase:
  bridge design, 16–22
  power system, 14–22
Thyristor, use of, 44, 48–49, 54–55, 80–81, 94–95, 99
Time counter, 200–201
Timer, 44–45, 139–140
Touch switch power control:
  i.c., 82–90
  using f.e.t., 79–81
  using i.c., 82–90
Transformer:
  converter, saturating, 55–56
  converter, two-, 66
  design, 72–73, 76–77

Transient analysis, 33–34

Transistor, high voltage switching:
  application, 25–34, 48–49, 62, 65–70
  construction, 23–24
  Darlington, 59–60, 62
  effect of parameters, 24–25

Transmitter section of u.a.r.t., 154–155
Triac, use of, 81, 84–86, 91, 94–96, 98–100
Triangular function generation, 188–189
Tripler, voltage, 3
Two's complement, 117

Unijunction transistor, programmable (p.u.t.), 35–46, 50–51, 58, 201

Universal asynchronous receiver/transmitter (u.a.r.t.)
  applications, 122, 126, 162–165
  control section, 155–156
  operation, 154–159
  receiver section, 154–155
  timing, 156–159
  transmission modes, 162
  transmitter section, 154–155

Vector generation, 178–180
Video digitiser circuit, 148
Visible light emitting diode, (v.l.e.d.), use of, 80–81, 85, 87, 191–204
V.l.e.d. display:
  applications, 196–202
  construction, 191
  description, 191–196
  types/characteristics, 203–204
Voltage:
  controlled oscillator, 46
  doubler, 2–3, 8–9, 14
  multiplier, 2–5
  n-stage multiplier, 3–4
  pick up, 79, 83, 85
  quadrupler, 3–4
  reference stage, 53, 66
  wiring system, low-, 81, 83–84
  zero switching, 45–46, 91

Waveform, analysis, 32–33

Zero crossing switching, 45–46, 91
Zero suppression (ripple blanking), 198

SEMICONDUCTOR CIRCUIT DESIGN

Volume I

SECTION 1. POWER CONTROL WITH TRIACS, THYRISTORS, AND UNIJUNCTION TRANSISTORS

Chapter I Triacs – Theory and General Applications
Chapter II Triacs with Resistive and Inductive Loads
Chapter III Solid State Switching Using Triacs and Thyristors
Chapter IV Burst Firing Techniques Using Triacs
Chapter V Thyristor Reversible D.C. Supply
Chapter VI Unijunction Transistors Theory, Operation and Circuits

SECTION 2. POWER TRANSISTOR APPLICATIONS

Chapter VII Switching Mode Power Supplies
Chapter VIII Monochrome TV Switching Regulator and Line Driver
Chapter IX Chopper Power Supplies using BUY69/70 High Voltage Power Transistors
Chapter X Inverters

SECTION 3. AUDIO CIRCUITS

Chapter XI A High Fidelity Preamplifier
Chapter XII Power Amplifiers
Chapter XIII Super Silect Transistors in Audio Amplifiers

SECTION 4. USING TTL INTEGRATED CIRCUITS

Chapter XIV TTL Counters and Registers
Chapter XV Numerous TTL Applications
Chapter XVI Use of TTL Integrated Circuits in Industrial Noise Environments
Index

SEMICONDUCTOR CIRCUIT DESIGN

Volume II

SECTION 1. DIGITAL INTEGRATED CIRCUITS

Chapter I Introduction to TTL
Chapter II Schottky TTL
Chapter III Schmitt Triggers
Chapter IV Threshold Detector
Chapter V Synchronous Counters
Chapter VI Reversible Counters
Chapter VII Programmable Synchronous Frequency Divider
Chapter VIII Data Selectors
Chapter IX Decoders/Demultiplexers
Chapter X Simple Binary to BCD & BCD to Binary Converters
Chapter XI Fast BCD to Binary & Binary to BCD Converters
Chapter XII Fast Multipliers

SECTION 2. OPERATIONAL AMPLIFIERS

Chapter XIII Introduction to Operational Amplifiers
Chapter XIV Applications of Operational Amplifiers
Chapter XV Logarithmic and Exponential Amplifiers
Chapter XVI A Stereo Amplifier

SECTION 3. OPTOELECTRONICS

Chapter XVII Introduction to Optoelectronics
Chapter XVIII Applications of Optoelectronics
Index

SEMICONDUCTOR CIRCUIT DESIGN

Volume III

SECTION 1. MOS INTEGRATED CIRCUITS

Chapter I	Process Technologies
Chapter II	MOS in Terminals
Chapter III	The Random Access Memory
Chapter IV	Arithmetic Processor
Chapter V	Interfacing MOS Devices

SECTION 2. SPECIAL PURPOSE BIPOLAR INTEGRATED CIRCUITS

Chapter VI	Line Drivers and Receivers
Chapter VII	(Programmable) Read-Only Memories
Chapter VIII	Zero Crossing Detector and Pulse Generator
Chapter IX	A Double Balanced Mixer
Chapter X	An Audio Power Amplifier

SECTION 3. FIELD EFFECT TRANSISTORS

Chapter XI	Theory and Operation
Chapter XII	RF Applications
Chapter XIII	High Input Impedance Circuits
Chapter XIV	Switching or 'Chopping' Circuits

SECTION 4. RADIO FREQUENCY POWER APPLICATIONS

Chapter XV	RF Power Transistors
Chapter XVI	Tuned Amplifier Design
Chapter XVII	Low Voltage Single Sideband Amplifiers
Chapter XVIII	Frequency Multipliers

TEXAS INSTRUMENTS
LIMITED
MANTON LANE · BEDFORD · ENGLAND

Semiconductor Circuit Design

Vol. IV

Texas
Instruments
Limited